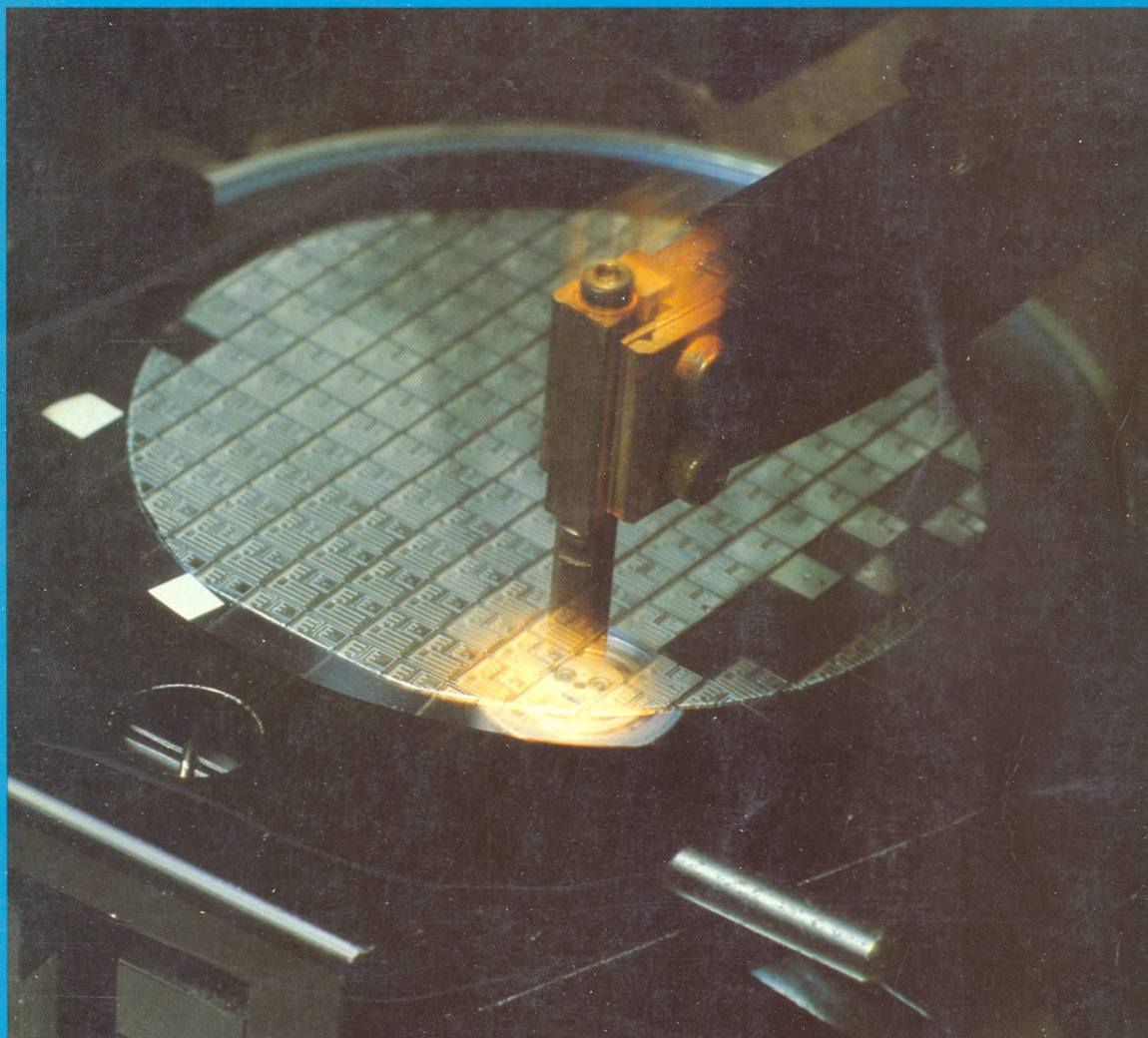




MOTOROLA Semiconductors



SWITCHMODE AND TMOS POWER TRANSISTORS

1983-84

Supplied by: ADVANCED SEMICONDUCTOR DEVICES (PTY) LTD.
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SWITCHMODE AND TMOS POWER TRANSISTORS 1983/84

Motorola, the world's largest power transistor supplier, offers devices for almost every Switchmode or power application. From our range of 5 Switchmode technologies and 9 standard packages, we have selected the most popular power transistors for new cost effective designs.

In case you did not find a satisfactory device, please contact your Motorola distributor or sales office for information. We also manufacture hundreds of special and standard products, that are not listed in this book.

Our large facility in Toulouse – France is supplying the European market with innovative and unique products designed to meet your requirements.

A companion booklet, called "Switchmode Selector Guide", including thyristors, SCRs, ICs and optocouplers, can be obtained for free from your Motorola distributor or sales office.

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BDY94	BUS45P*
BDY96	BUS47
BDY97	BUS47
BU126	BUS45P*
BU126A	BUS45P*
BU326	BUS45P*
BU326A	BUS45P*
BU326S	BUS45P*
BU426	BUS45P*
BU426E	BUS45P
BUS11	BUS46P*
BUS12	BUS47
BUS12A	BUS47A
BUS13	BUS48
BUS13A	BUS48A
BUS14	BUS98
BUS14A	BUS98A
BUV46	BUS45P
BUV47	BUS47P
BUV47A	BUS47AP
BUV47B	BUS47P
BUV48	BUS48P
BUV48A	BUS48AP
BUW25	BUS45P*
BUW26	BUS46P*
BUW34	BUS47
BUW35	BUS47
BUW36	BUS47A
BUW44	BUS48
BUW45	BUS48
BUW46	BUS48A
BUW71	BUS45P*
BUW72	BUS46P*
BUX46	BUS45P*
BUX47	BUS47
BUX47A	BUS47A
BUX48	BUS48
BUX48A	BUS48A
BUX80	BUS47
BUX81	BUS47A
BUX82	BUS46P*
BUX84	BUS45P*
BUX97	BUS45P*

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BUX97A	BUS45P*
BUX97B	BUS45P*
BUX98	BUS98
BUX98A	BUS98A
BUY69A	BUS47A
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MJE13006	BUS46P
MJE13007	BUS46P
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SVT400-3	BUS46P*
SVT400-5	BUS47
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SVT450-5	BUS47
SVT7520	BUS46P*
SVT7521	BUS46P*
SVT7522	BUS46P*
SVT7523	BUS46P*
SVT7524	BUS46P*
SVT7525	BUS46P*
SVT7530	BUS47
SVT7531	BUS47
SVT7532	BUS47
SVT7533	BUS47
SVT7534	BUS47
SVT7535	BUS47
SVT7536	BUS47
SVT7540	BUS47
SVT7541	BUS47
SVT7542	BUS47
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* Different package

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SVT7545	BUS48
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SVT7551	BUS48
SVT7552	BUS48
SVT7553	BUS48
SVT7554	BUS48
SVT7555	BUS48
SVT7561	BUS48
SVT7562	BUS48
SVT7563	BUS48
SVT7564	BUS48
SVTR7543	BUS47
TIP53	BUS46P*
TIP54	BUS46P*
TIP57A	BUS47P
TIP58A	BUS47P
TIP75A	BUS45P
TIP75B	BUS45P
TIP75C	BUS45P
TIP560	BUS47
TIP561	BUS47
TIP562	BUS48
TIP563	BUS48
TIP575A	BUS48
TIP575B	BUS48
TIP575C	BUS48
TIPL751	BUS46P*
TIPL752	BUS47
TIPL752A	BUS47A
TIPL753	BUS47
TIPL753A	BUS47A
TIPL755	BUS48
TIPL755A	BUS48A
TIPL762	BUS47P
TIPL762A	BUS47AP
TIPL763	BUS47P
TIPL763A	BUS47AP
TIPL765	BUS48P
TIPL765A	BUS48AP
2N6306	BUS47
2N6307	BUS47
2N6308	BUS47
2N6542	BUS46P*
2N6543	BUS46P*

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2N6544	BUS47
2N6545	BUS47
2N6546	BUS48
2N6547	BUS48
2N6579	BUS47
2N6580	BUS47
2N6581	BUS47
2N6582	BUS47
2N6583	BUS47
2N6584	BUS47
2N6671	BUS47
2N6672	BUS47
2N6673	BUS47
2N6674	BUS48
2N6675	BUS48

* Different package

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BUZ10A	MTP14N05
BUZ20	MTP12N10
BUZ23	MTM12N10
BUZ30	MTP7N20
BUZ32	MTP12N20
BUZ33	MTM7N20
BUZ35	MTM12N20
BUZ40	MTP2N50
BUZ41	MTP5N50
BUZ41A	MTP5N50
BUZ42	MTP4N50
BUZ43	MTM2N50
BUZ44	MTM7N50
BUZ44A	MTM5N50
BUZ45	MTM10N50
BUZ45A	MTM7N50
BUZ46	MTM4N50
BUZ53	MTM4N100
BUZ60	MTP7N40
BUZ63	MTM7N40
BUZ64	MTM15N40
BUZ83	MTM4N85
BUZ84	MTM5N85
IRF100	MTM12N06
IRF101	MTM12N06
IRF120	MTM10N10
IRF121	MTM10N08
IRF122	MTM10N10
IRF123	MTM10N08
IRF130	MTM12N10
IRF131	MTM12N08
IRF132	MTM12N10
IRF133	MTM12N06
IRF151	MTM35N06
IRF152	MTM25N10
IRF153	MTM25N06
IRF220	MTM7N20
IRF221	MTM7N15
IRF222	MTM5N20
IRF223	MTM7N15
IRF230	MTM8N20
IRF231	MTM8N15
IRF232	MTM7N20
IRF233	MTM7N15
IRF300	MTM5N40
IRF301	MTM5N35
IRF305	MTM5N40
IRF306	MTM5N35
IRF320	MTM5N40

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IRF321	MTM5N35
IRF322	MTM5N40
IRF323	MTM5N35
IRF330	MTM7N40
IRF331	MTM7N35
IRF332	MTM5N40
IRF333	MTM5N35
IRF350	MTM15N40
IRF351	MTM15N35
IRF352	MTM15N40
IRF353	MTM15N35
IRF420	MTM4N50
IRF421	MTM4N45
IRF422	MTM2N50
IRF423	MTM2N45
IRF430	MTM5N50
IRF431	MTM5N45
IRF432	MTM4N50
IRF433	MTM4N45
IRF450	MTM15N50
IRF451	MTM15N45
IRF452	MTM15N50
IRF453	MTM15N45
IRF520	MTP10N10
IRF521	MTP10N08
IRF522	MTP5N20
IRF523	MTP10N08
IRF530	MTP12N10
IRF531	MTP12N08
IRF532	MTP12N10
IRF533	MTP12N06
IRF620	MTP8N20
IRF621	MTP7N15
IRF622	MTP564
IRF623	MTP3N15
IRF630	MTP12N20
IRF631	MTP10N15
IRF632	MTP7N20
IRF633	MTP8N15
IRF710	MTP3N40
IRF711	MTP3N35
IRF712	MTP3N40
IRF713	MTP3N35
IRF720	MTP5N40
IRF721	MTP5N35
IRF722	MTP5N40
IRF723	MTP5N35
IRF730	MTP7N40
IRF731	MTP7N35
IRF732	MTP5N40

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IRF733	MTP5N35
IRF820	MTP4N50
IRF821	MTP4N45
IRF822	MTP2N50
IRF823	MTP2N45
IRF830	MTP5N50
IRF831	MTP5N45
IRF832	MTP4N50
IRF833	MTP4N45
IRF9130	MTM815
IRF9131	MTM814
IRF9132	MTM815
IRF9133	MTM814
IRF9530	MTP815
IRF9531	MTP814
IRF9532	MTP815
IRF9533	MTP814
IVN5200HND	MTM12N06
IVN5200HNE	MTM12N06
IVN5200HNF	MTM12N06
IVN5200KND	MTM12N06
IVN5200KNE	MTM12N06
IVN5200KNF	MTM12N06
IVN5201CND	MTP12N06
IVN5201CNE	MTP12N06
IVN5201CNF	MTP12N06
IVN5201HND	MTM12N06
IVN5201HNE	MTM12N06
IVN5201HNF	MTM12N06
IVN5201KND	MTM12N06
IVN5201KNE	MTM12N06
IVN5201KNF	MTM12N06
IVN6000CNR	MTP5N35
IVN6000CNS	MTP5N40
IVN6000CNT	MTP4N50
IVN6000KNR	MTM5N35
IVN6000KNS	MTM5N40
IVN6000KNT	MTM4N45
MTM474	MTM4N45
MTM475	MTM4N50
MTM564	MTM5N35
MTM565	MTM5N40
MTP1034	MTP10N12
MTP1035	MTP10N15
MTP1224	MTP12N06
MTP1225	MTP12N10
VN64GA	MTM12N06
VN4000A	MTM5N40
VN4001A	MTM5N40
VNO330N1	MTM5N35

Industry Part Number Motorola Replacement

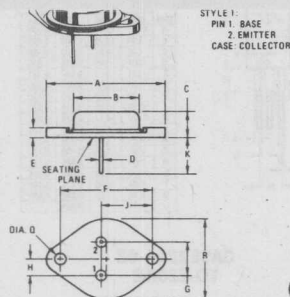
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VNO335A1	MTM5N35
VNO335B1	MTM5N35
VNO335C1	MTM5N35
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VNO335N5	MTP5N35
VNO340A1	MTM5N40
VNO340B1	MTM5N40
VNO340C1	MTM5N40
VNO340N1	MTM5N40
VNO340N5	MTP5N40
VNO345A1	MTM4N45
VNO345B1	MTM4N45
VNO345C1	MTM4N45
VNO345N1	MTM4N45
VNO345N5	MTP474
VNO350A1	MTM4N50
VNO350B1	MTM4N50
VNO350C1	MTM4N50
ZVNO345L	MTP4N45
ZVNO345M	MTM4N50
ZVNO435M	MTM8N35
ZVNO440M	MTM7N40
ZVNO405M	MTM4N50
ZVN1204L	MTP12N06
ZVN1204M	MTM12N06
ZVN1206L	MTP12N06
ZVN1206M	MTM12N06
ZVN1208L	MTP12N10
ZVN1208M	MTM12N10
ZVN1209L	MTP12N10
ZVN1209M	MTM10N10
ZVN1210L	MTP8N10
ZVN1210M	MTM8N10
ZVN1214L	MTP7N15
ZVN1214M	MTM7N15
ZVP0345L	MTP2P45
ZVP0345	MTM2P45

Mechanical Outlines

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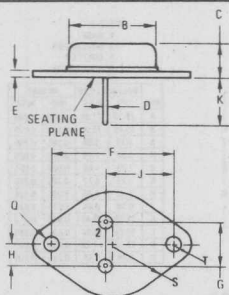
The packaging availability for each device is indicated on the tables. The dimensions for the packages are given in this section.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	28.27	—	1.150
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
I	16.64	17.15	0.655	0.675
J	11.18	12.19	0.440	0.480
K	3.84	4.09	0.151	0.161
L	—	28.67	—	1.090

Collector connected to case

Case 11-01
(TO-204) (Type)



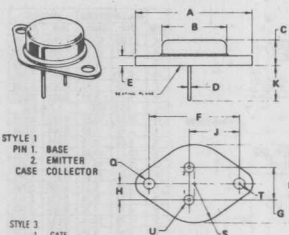
STYLE 1
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.27	5.72	0.205	0.225
I	16.64	17.15	0.655	0.675
J	7.92	—	0.312	—
K	—	13.34	—	0.525
L	—	4.78	—	0.188

CASE 1-03 (TO3)

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	38.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
I	16.64	17.15	0.655	0.675
J	11.18	12.19	0.440	0.480
K	3.84	4.19	0.150	0.165
L	—	28.67	—	1.090
M	2.54	3.05	0.100	0.120



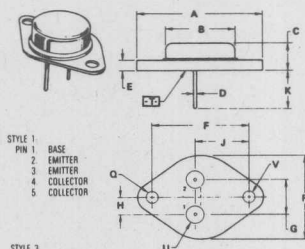
STYLE 1
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

STYLE 3
1. GATE
2. SOURCE
CASE-DRAIN

Case 1-04
TO-204AA (Type)

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS
2. [T] IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
 $\phi \pm 0.13 (0.005) \text{ T V } \phi$
FOR LEADS
 $\phi \pm 0.13 (0.005) \text{ T V } \phi \text{ } \phi$
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5-1973

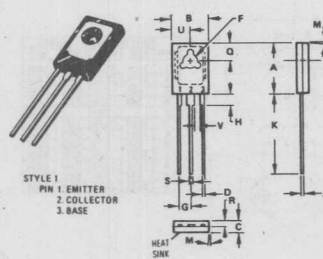
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	28.67	—	1.090
N	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165



STYLE 1
PIN 1. BASE
2. EMITTER
3. EMITTER
4. COLLECTOR
5. COLLECTOR

STYLE 3
PIN 1. GATE
2. SOURCE
CASE-DRAIN

Case 1-05
TO-204AA (Type)



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 5
1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

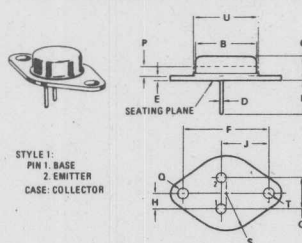
CASE 77-04
TO-126

NOTES:
2. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. TO DIM "A" "B" "W" AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.69	0.425	0.460
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.68	0.020	0.026
E	2.62	3.18	0.115	0.125
F	2.21	2.46	0.087	0.097
G	1.27	2.41	0.050	0.095
H	0.38	0.84	0.015	0.033
I	15.11	16.64	0.595	0.655
J	—	30 TYP	—	30 TYP
K	3.76	4.61	0.148	0.180
L	1.14	1.40	0.045	0.055
M	0.64	0.89	0.025	0.035
N	3.68	3.94	0.145	0.155
V	1.82	—	0.040	—

All JEDEC Dimensions and Notes Apply

CASE 80-02
TO-66

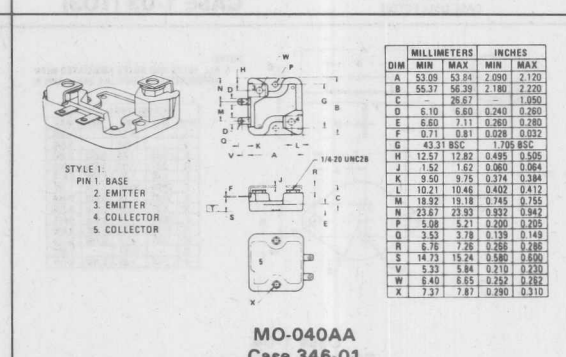
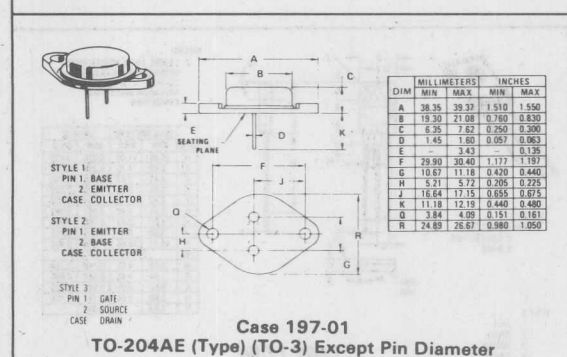
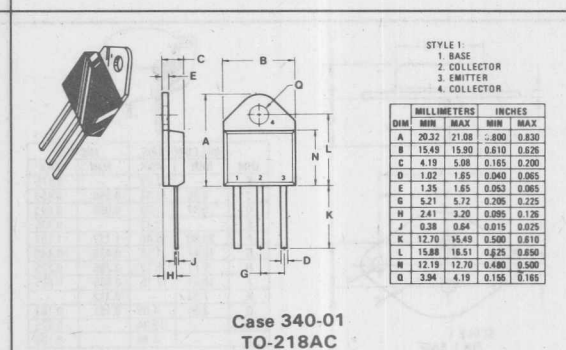
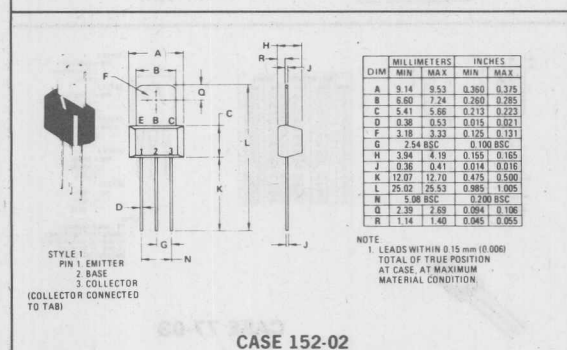
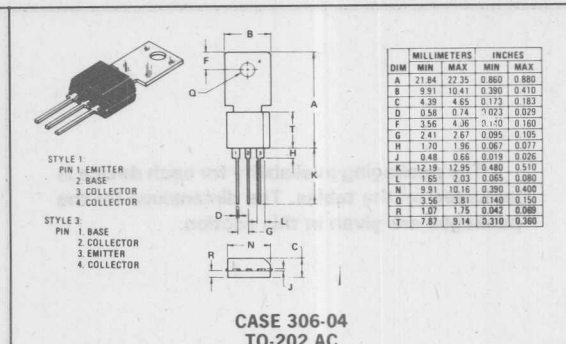
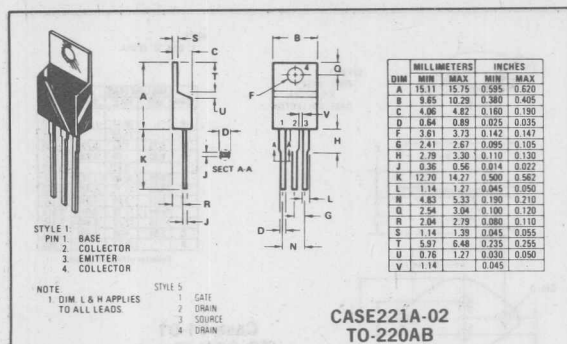


STYLE 1
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	11.84	12.70	0.470	0.500
B	8.35	8.64	0.330	0.340
C	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.23	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
L	—	1.27	—	0.050
M	3.81	4.06	0.150	0.160
N	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

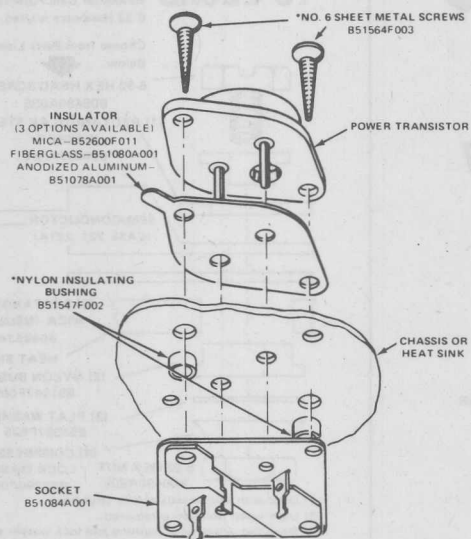
2

OUTLINE DIMENSIONS (continued)



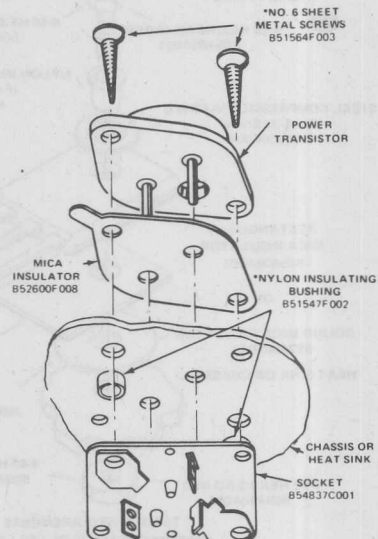
MOUNTING HARDWARE

TO-204AA (Type)



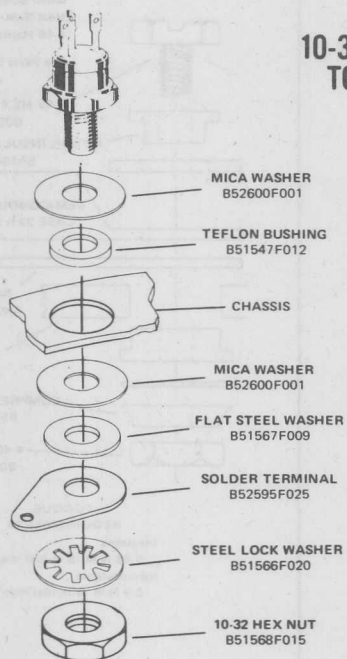
* Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

TO-66

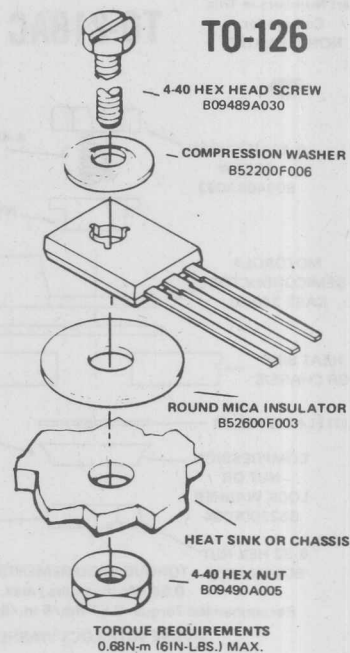


* Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

10-32 STUD TO-59

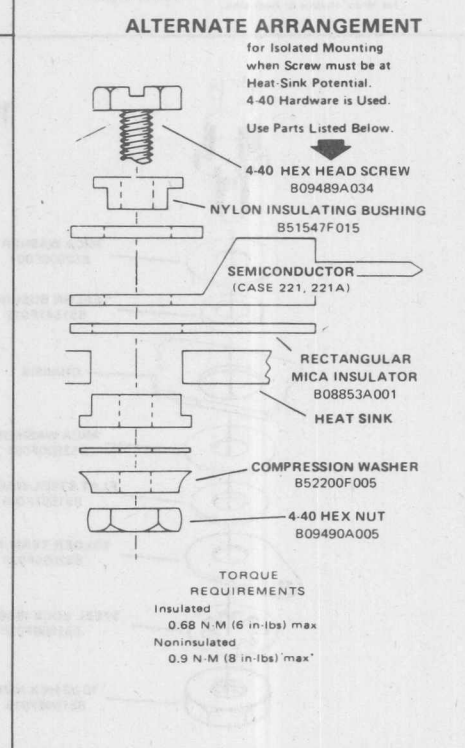
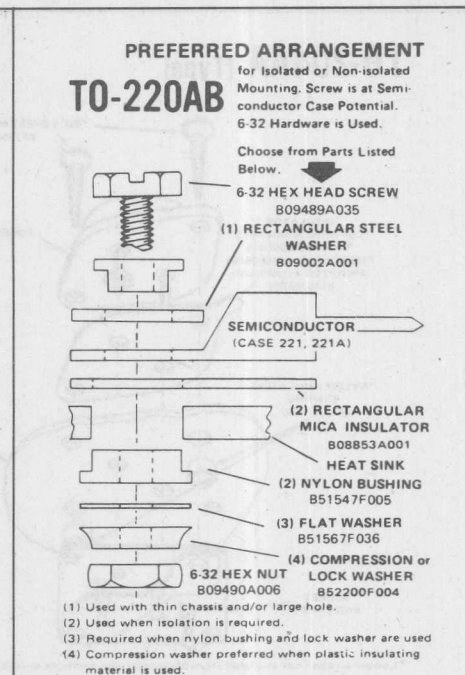
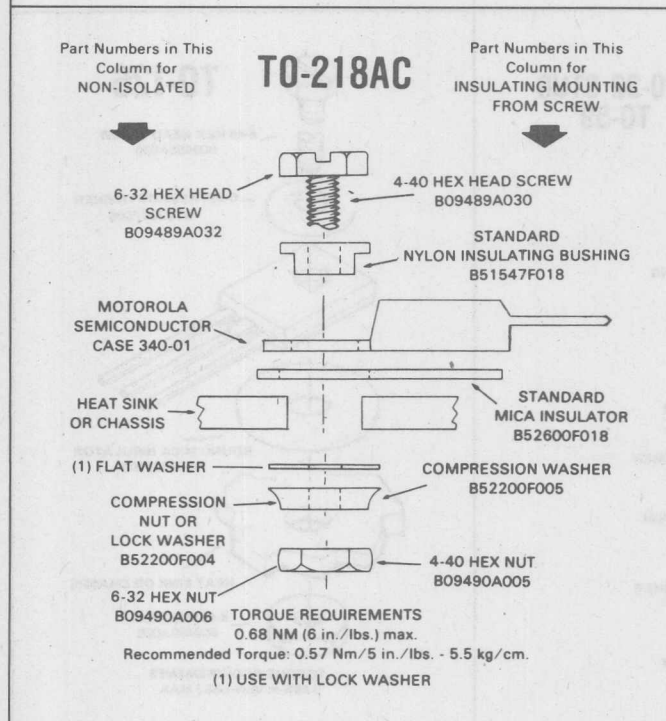
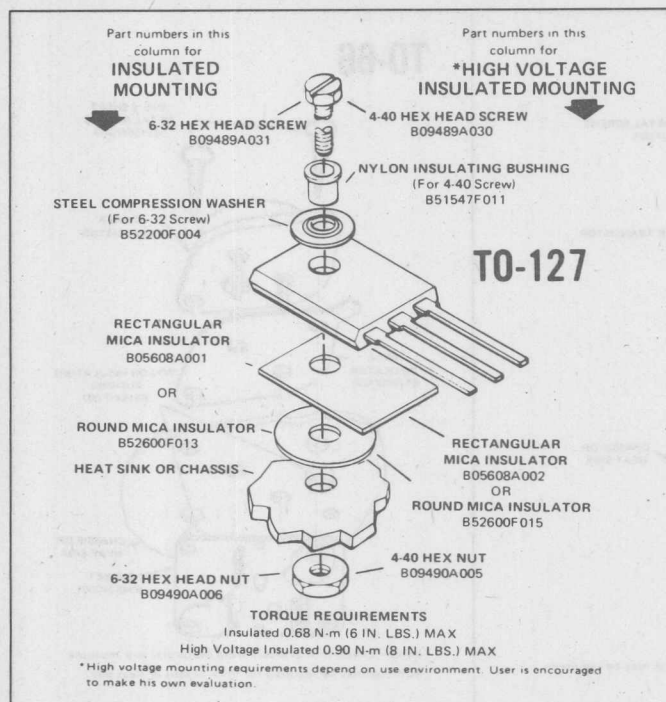


TO-126



TORQUE REQUIREMENTS
0.68N-m (6IN-LBS.) MAX.

MOUNTING HARDWARE (continued)



Data Sheets

3

**SWITCHMODE^Δ SERIES
NPN SILICON POWER TRANSISTOR**

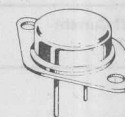
...designed for high speed, high voltage, high power applications.

- Low saturation: $V_{CE(sat)}$ max. = 1.0 V @ $I_C = 10$ A
- Very fast switching times:
 t_F typ. = 50 nS @ $I_C = 5$ A

10 AMPERES

**NPN SILICON
POWER
METAL TRANSISTOR**

**60 - 100 VOLTS
40 WATTS @ $T_c = 75^\circ\text{C}$**



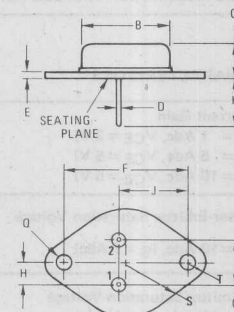
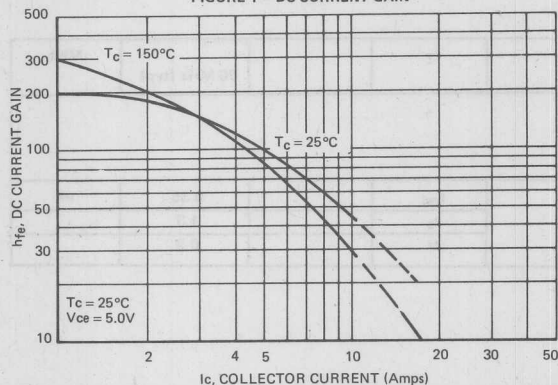
MAXIMUM RATINGS

Rating	Symbol	BDY90	BDY91	BDY92	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	100	80	60	Vdc
Collector-Base Voltage	V_{CEO}	120	100	80	Vdc
Collector-Emitter Voltage	V_{CEV}	120	100	80	Vdc
Emitter Base Voltage	V_{EB}		6		Vdc
Collector Current-Continuous	I_C		10		Adc
Peak	I_{CM}		15		
Base Current-Continuous	I_B		2		Adc
Peak	I_{BM}		3		
Total Power Dissipation @ $T_c = 75^\circ\text{C}$ Derate above 25°C	P_D		40		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}		- 65 to 175		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.5	$^\circ\text{C/W}$

FIGURE 1 - DC CURRENT GAIN



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
----------------	--------	------	------	------

OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 30\text{ mA}$, $I_B = 0$)	BDY90 BDY91 BDY92	$V_{CE(sus)}$	100 80 60	Vdc
Collector Cutoff Current at Reverse Biases: ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ V}$), ($T_C = 150^\circ\text{C}$)		I_{CEX}		mAdc
Emitter-Cutoff Current ($V_{EB} = 6\text{ V}$)		I_{EBO}	0.1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 6	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 7	

ON CHARACTERISTICS¹

DC Current Gain ($I_C = 1\text{ Adc}$, $V_{CE} = 2\text{ V}$) ($I_C = 5\text{ Adc}$, $V_{CE} = 5\text{ V}$) ($I_C = 10\text{ Adc}$, $V_{CE} = 5\text{ V}$)		h_{FE}	35 30 20	120	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1\text{ Adc}$)	BDY90, BDY91 BDY92	$V_{CE(sat)}$	1.5 1.0		Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1\text{ Adc}$)		$V_{BE(sat)}$	1.5		Vdc

DYNAMIC CHARACTERISTICS

Current Gain - Bandwidth Product ($f = 10\text{ MHz}$, $I_C = 0.5\text{ A}$, $V_{CE} = 5\text{ V}$)	f_T		70 MHz (typ)	MHz
--	-------	--	--------------	-----

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	(I _C = 5 A, V _{CC} = 30 V) (I _{B1} = - I _{B2} = 0.5 A)	t_{on}	0.35	μs
Storage Time		t_s	1.3	
Fall Time		t_f	0.2	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%

FIGURE 1 - DC CURRENT GAIN

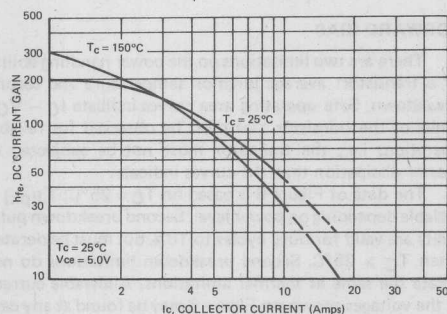


FIGURE 2 - COLLECTOR SATURATION REGION

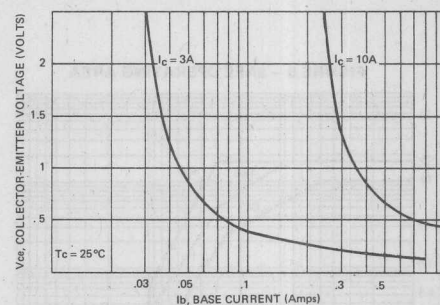


FIGURE 3 - COLLECTOR-EMITTER SATURATION VOLTAGE

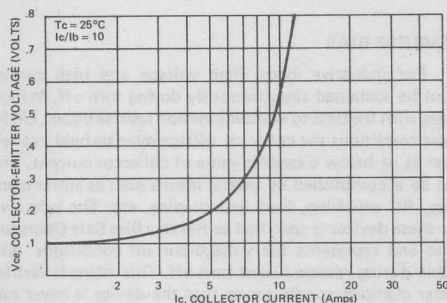


FIGURE 4 - BASE-EMITTER VOLTAGE

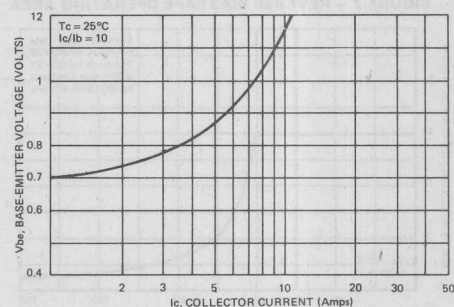
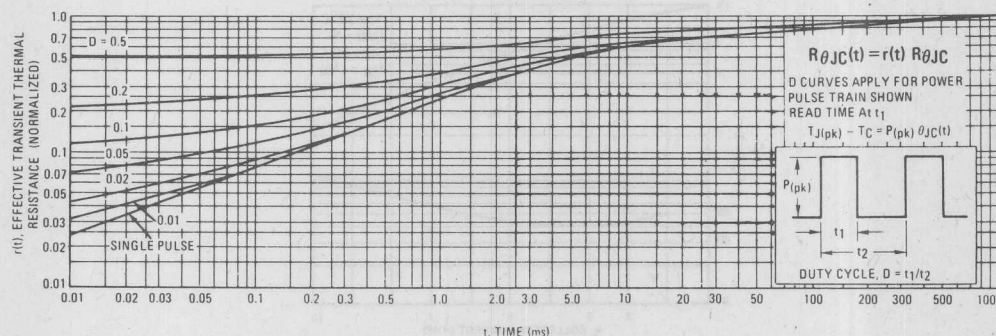


FIGURE 5 - THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 6 and 7 are specified for these devices under the test conditions shown.

FIGURE 6 - SAFE OPERATING AREA

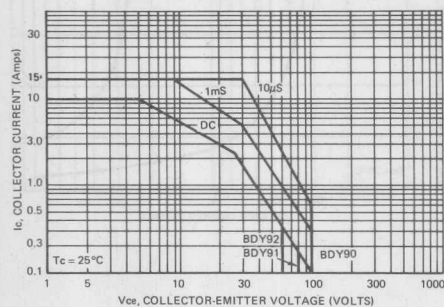


FIGURE 7 - REVERSE BIAS SAFE OPERATING AREA

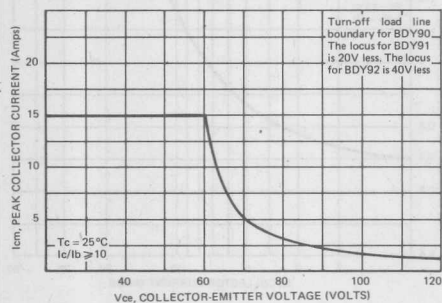
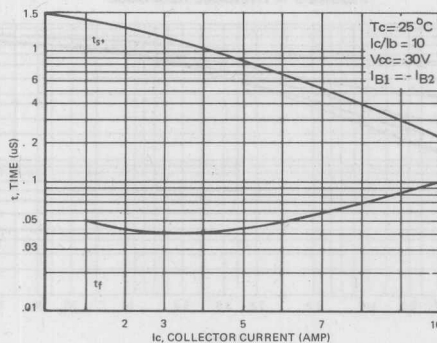


FIGURE 8 - TURN-OFF TIME vs IC



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure gives the RBSOA characteristics.

**MOTOROLA**

BD135, -6, -10, -16
BD137, -6, -10, -16
BD139, -6, -10, -16

**PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR**

... designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- Available in HFE groups -6, -10, -16
- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
- BD 135, 137, 139 are complementary with BD 136, 138, 140

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 135	45	Vdc
		BD 137	60	
		BD 139	80	
Collector-Base Voltage	V_{CBO}	BD 135	45	Vdc
		BD 137	60	
		BD 139	80	
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$	P_D		1.25	Watts
			10	mW/°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D		12.5	Watt
			100	mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

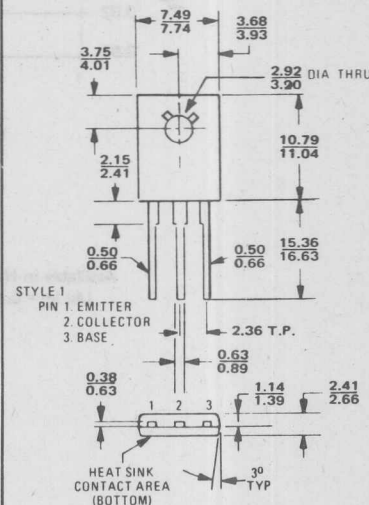
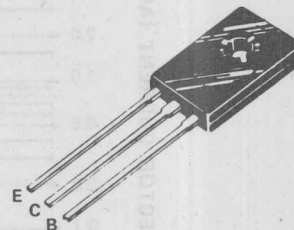
Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.03$ Adc, $I_B = 0$)	V_{CEO}^*	BD 135	45	—	Vdc
		BD 137	60	—	
		BD 139	80	—	
Collector Cutoff Current ($V_{CB} = 30$ Vdc, $I_E = 0$) ($V_{CB} = 30$ Vdc, $I_E = 0$, $T_C = 125^\circ\text{C}$)	I_{CBO}		—	0.1	μAdc
			—	10	
			—	—	
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	10	μAdc
DC Current Gain ($I_C = 0.005$ A, $V_{CE} = 2$ V) ($I_C = 0.15$ A, $V_{CE} = 2$ V) ($I_C = 0.5$ A, $V_{CE} = 2$ V)	h_{FE}^*		25	—	—
			40	250	
			25	—	
Collector-Emitter Saturation Voltage* ($I_C = 0.5$ Adc, $I_B = 0.05$ Adc)	$V_{CE(sat)}^*$		—	0.5	Vdc
Base-Emitter On Voltage* ($I_C = 0.5$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}^*$		—	1	Vdc

* Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$

**1.5 AMPERE
POWER TRANSISTOR**

NPN SILICON

**45, 60, 80 VOLTS
10 WATTS**



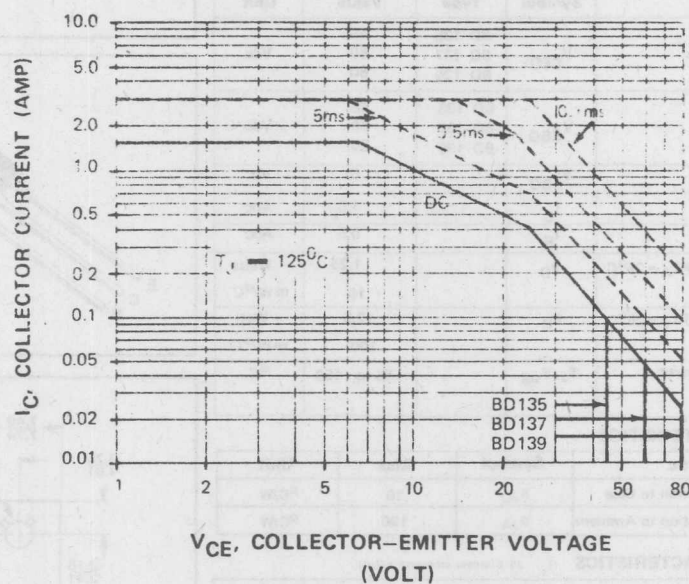
When mounting the device, torque not to exceed 0.07 m·kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
All dimensions in millimeters

CASE 77-04



FIGURE 1 — ACTIVE REGION SAFE OPERATING AREA



Available in HFE groups

(At $I_C = 0.15\text{ A}$, $V_{CE} = 2\text{ V}$) HFE group:

	Min.	Max.
-6	40	100
-10	63	160
-16	100	250

**MOTOROLA**

BD136, -6, -10, -16
BD138, -6, -10, -16
BD140, -6, -10, -16

**PLASTIC MEDIUM POWER
SILICON PNP TRANSISTOR**

... designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- Available in HFE groups -6, -10, -16
- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
- BD 136, 138, 140 are complementary with BD 135, 137, 139

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 136	45	Vdc
		BD 138	60	
		BD 140	80	
Collector-Base Voltage	V_{CBO}	BD 136	45	Vdc
		BD 138	60	
		BD 140	80	
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D		1.25	Watts
			10	mW/°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D		12.5	Watt
			100	mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

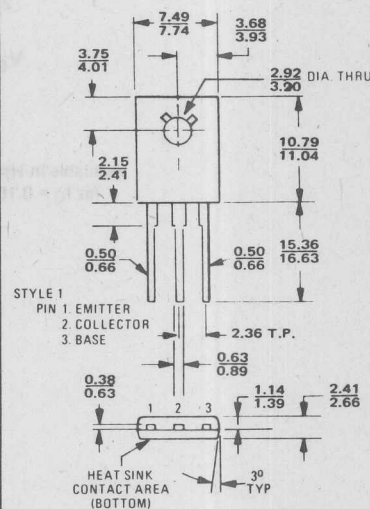
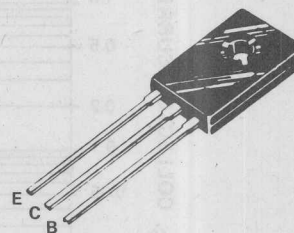
Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.03$ Adc, $I_B = 0$)	V_{CEO}^*	BD 136	45	—	Vdc
		BD 138	60	—	
		BD 140	80	—	
Collector Cutoff Current ($V_{CB} = 30$ Vdc, $I_E = 0$) ($V_{CB} = 30$ Vdc, $I_E = 0$, $T_C = 125^\circ\text{C}$)	I_{CBO}		—	0.1	μAdc
			—	10	
			—	—	
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	10	μAdc
DC Current Gain ($I_C = 0.005$ A, $V_{CE} = 2$ V) ($I_C = 0.15$ A, $V_{CE} = 2$ V) ($I_C = 0.5$ A, $V_{CE} = 2$ V)	h_{FE}^*		25	—	—
			40	250	
			25	—	
Collector-Emitter Saturation Voltage* ($I_C = 0.5$ Adc, $I_B = 0.05$ Adc)	$V_{CE(sat)}^*$		—	0.5	Vdc
Base-Emitter On Voltage* ($I_C = 0.5$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}^*$		—	1	Vdc

* Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$.

**1.5 AMPERE
POWER TRANSISTOR**

PNP SILICON

**45, 60, 80 VOLTS
10 WATTS**

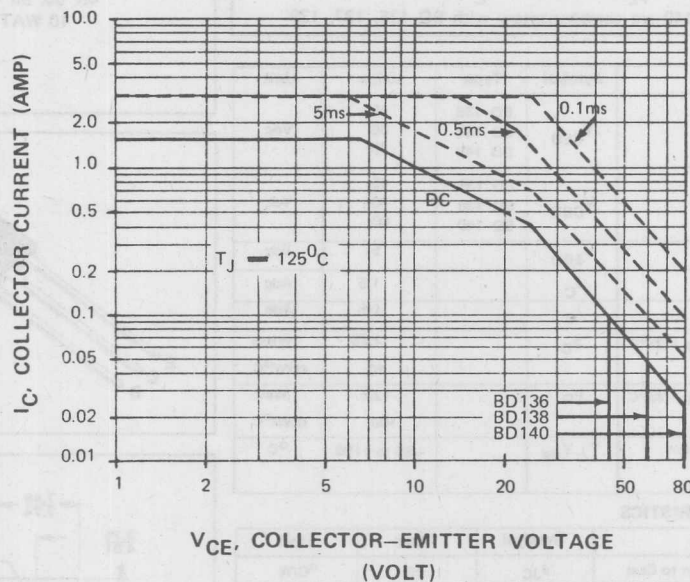


When mounting the device, torque not to exceed 0.07 m·kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
All dimensions in millimeters

CASE 77-04

FIGURE 1 — ACTIVE REGION SAFE OPERATING AREA



Available in HFE groups

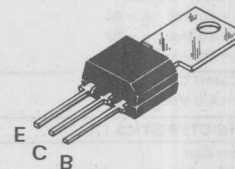
(at I_C = 0.15 A, V_{CE} 2 V) HFE group:

	Min.	Max.
-6	40	100
-10	63	160
-16	100	250

**MOTOROLA****BD385
BD387
BD389****NPN SILICON ANNULAR*
AMPLIFIER TRANSISTORS**

... designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage –
 $BV_{CEO} = 100 \text{ Vdc (Min.) @ } I_C = 1.0 \text{ mAdc} - \text{BD389}$
- Duowatt Package – 2 Watts Free Air Dissipation @ $T_A = 25^\circ\text{C}$
- Complements to PNP BD386, BD388, BD390

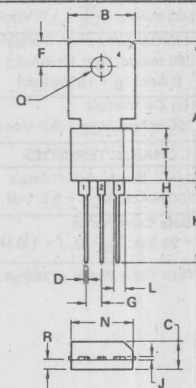
DUOWATT**NPN SILICON
AMPLIFIER TRANSISTORS****MAXIMUM RATINGS**

Rating	Symbol	BD385	BD387	BD389	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
Emitter-Base Voltage	V_{EBO}	5.0			Vdc
Collector Current – Continuous – Peak (1)	I_C	1.0			Adc
Base Current	I_B	100			mAdc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0			Watts
		16			mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10			Watts
		80			mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			$^\circ\text{C}$
Solder Temperature, 1/16" from Case for 10 Seconds	–	260			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$

(1) $\leq 10 \text{ ms}, \leq 50\% \text{ Duty Cycle}$



STYLE 2
PIN
1. EMITTER
2. COLLECTOR
3. BASE
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

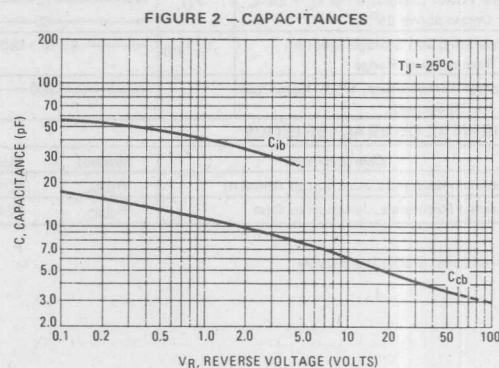
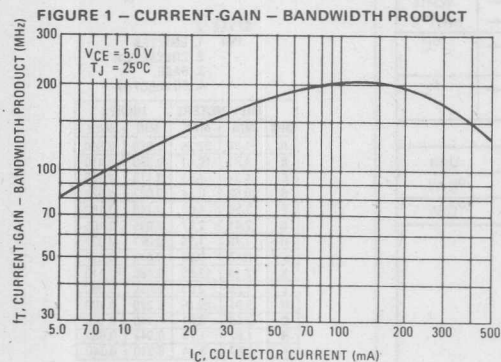
CASE 306-04

*ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 1.0\text{ mA}$, $I_B = 0$)	BV_{CEO}	60	—	Vdc
BD385		80	—	
BD387		100	—	
BD389				
Collector-Base Breakdown Voltage ($I_C = 100\text{ }\mu\text{A}$, $I_E = 0$)	BV_{CBO}	60	—	Vdc
BD385		80	—	
BD387		100	—	
BD389				
Emitter-Base Breakdown Voltage ($I_E = 100\text{ }\mu\text{A}$, $I_C = 0$)	BV_{EBO}	5.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 40\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	100	nAdc
BD385		—	100	
BD387		—	100	
BD389		—	100	
Emitter Cutoff Current ($V_{EB} = 4.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	100	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 10\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	60	—	—
($I_C = 50\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$)		80	300	
($I_C = 250\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$)		60	—	
($I_C = 500\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$)		25	—	
Collector-Emitter Saturation Voltage ($I_C = 250\text{ mA}$, $I_B = 10\text{ mA}$)	$V_{CE(sat)}$	—	0.5	Vdc
($I_C = 1.0\text{ A}$, $I_B = 100\text{ mA}$)		—	1.0	
Base-Emitter On Voltage ($I_C = 250\text{ mA}$, $V_{CE} = 5.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product ($I_C = 100\text{ mA}$, $V_{CE} = 5.0\text{ Vdc}$, $f = 20\text{ MHz}$)	f_T	75	350	MHz
Collector-Base Capacitance ($V_{CB} = 20\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	C_{cb}	—	18	pF

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

FIGURE 3 – DC CURRENT GAIN

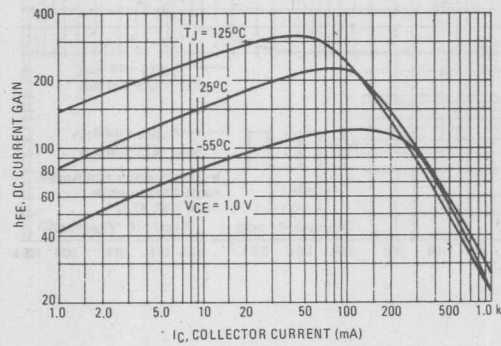


FIGURE 4 – "ON" VOLTAGE

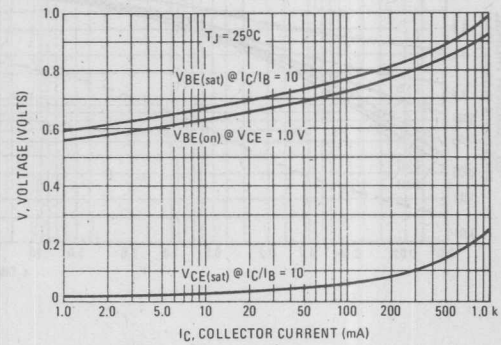


FIGURE 5 – COLLECTOR SATURATION REGION

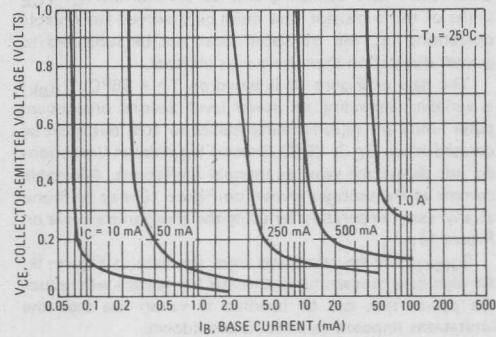


FIGURE 6 – TEMPERATURE COEFFICIENTS

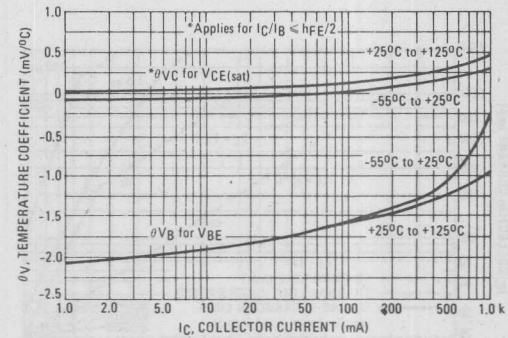


FIGURE 7 – COLLECTOR CHARACTERISTICS

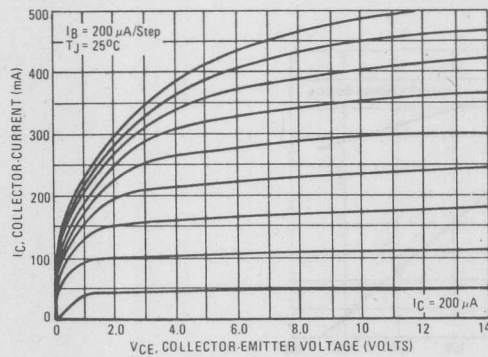
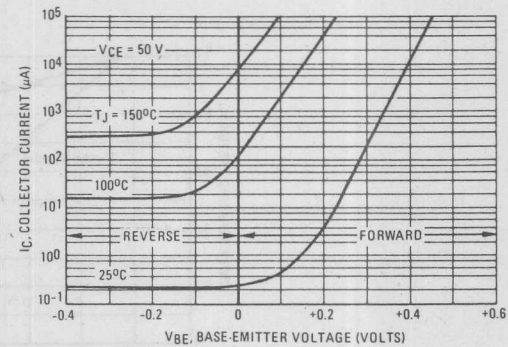


FIGURE 8 – COLLECTOR CUTOFF REGION



TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – THERMAL RESPONSE

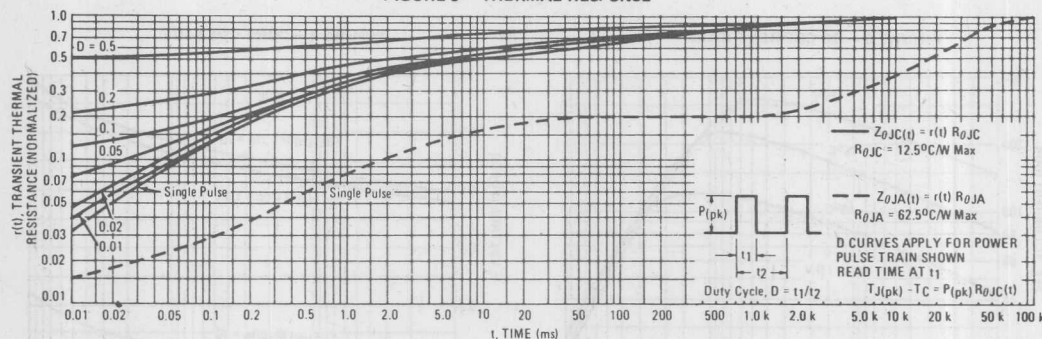
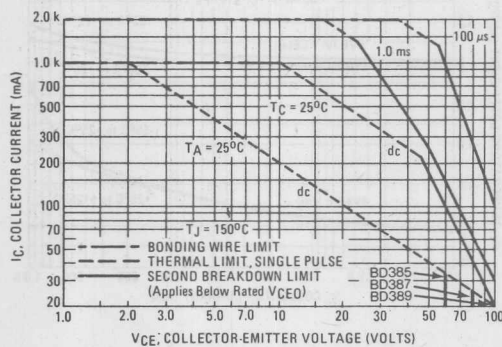


FIGURE 10 – ACTIVE-REGION SAFE-OPERATING AREA

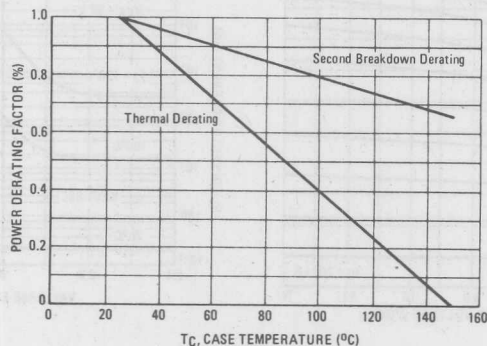


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^{\circ}\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^{\circ}\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING





MOTOROLA

BD386

BD388

BD390

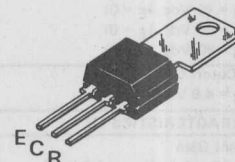
PNP SILICON ANNULAR AMPLIFIER TRANSISTORS

... designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage – $BV_{CEO} = 100 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc}$ – BD390
- Duowatt Package – 2 Watts Free Air Dissipation @ $T_A = 25^\circ\text{C}$
- Complements to NPN BD385/BD387/BD389

DUOWATT

PNP SILICON AMPLIFIER TRANSISTORS

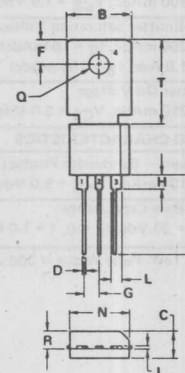


MAXIMUM RATINGS

Rating	Symbol	BD386	BD388	BD390	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
Emitter-Base Voltage	V_{EBO}	5.0			Vdc
Collector Current – Continuous Peak	I_C	1.0			Adc
Base Current	I_B	100			mAdc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0			Watts
		16			mW/°C
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10			Watts
		80			mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			°C
Solder Temperature, 1/16" from Case for 10 Seconds	–	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 2
PIN 1. EMITTER
2. COLLECTOR
3. BASE
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

*ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS *				
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}$, $I_B = 0$)	BV_{CEO}	60 80 100	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100 \mu\text{Adc}$, $I_E = 0$)	BV_{CBO}	60 80 100	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{Adc}$, $I_C = 0$)	BV_{EBO}	5.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	— — —	100 100 100	nAdc
Emitter Cutoff Current ($V_{EB} = 4.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	100	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 10 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 50 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 250 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$)	h_{FE}	60 80 60 25	— 300 — —	
Collector-Emitter Saturation Voltage ($I_C = 250 \text{ mAdc}$, $I_B = 10 \text{ mAdc}$) ($I_C = 1.0 \text{ Adc}$, $I_B = 100 \text{ mAdc}$)	$V_{CE(sat)}$	— —	0.5 1.0	Vdc
Base-Emitter On Voltage ($I_C = 250 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product ($I_C = 100 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 20 \text{ MHz}$)	f_T	75	350	MHz
Collector-Base Capacitance ($V_{CB} = 20 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	C_{cb}		18	pF

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

TYPICAL CHARACTERISTICS

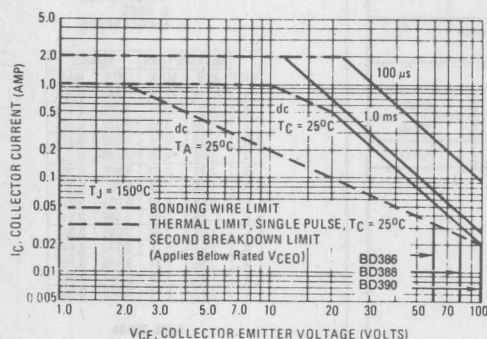


FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

TYPICAL CHARACTERISTICS (continued)

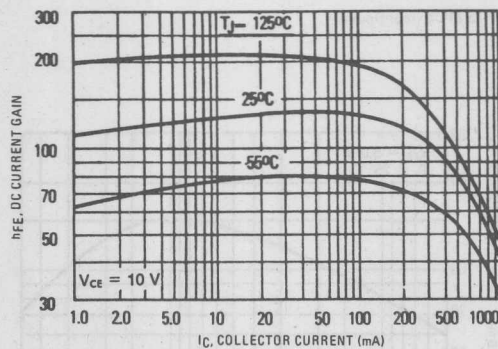


FIGURE 2 – DC CURRENT GAIN

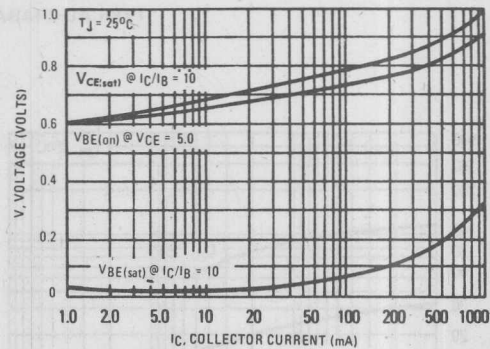


FIGURE 3 – "ON" VOLTAGES

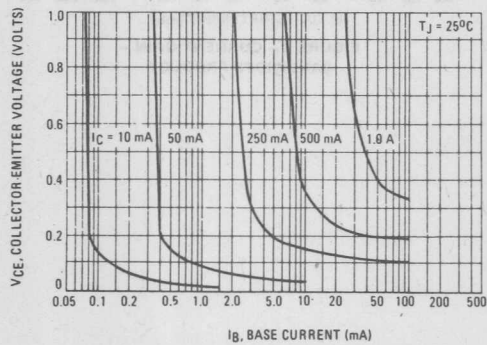


FIGURE 4 – COLLECTOR SATURATION REGION

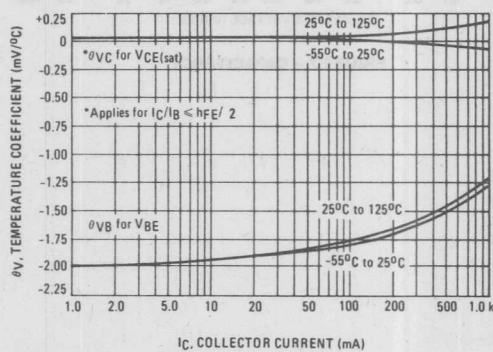


FIGURE 5 – TEMPERATURE COEFFICIENTS

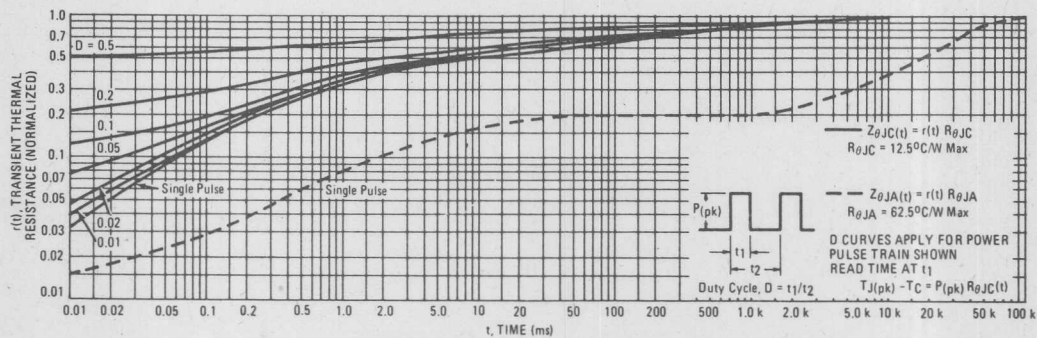


FIGURE 6 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

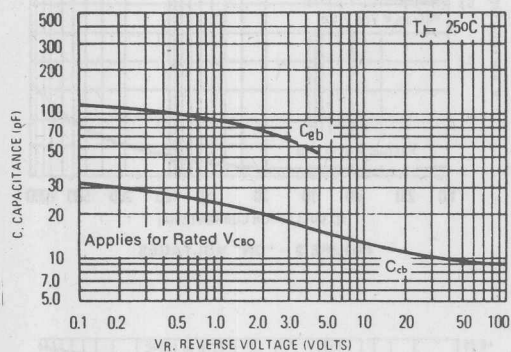


FIGURE 7 – CAPACITANCE

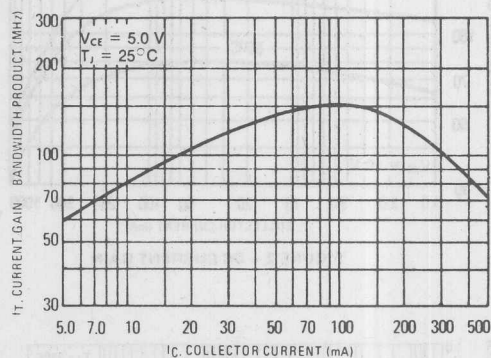
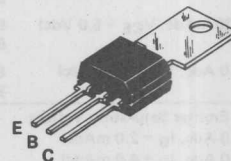


FIGURE 8 – CURRENT GAIN –
BANDWIDTH PRODUCT

**MOTOROLA****BD411****BD412****NPN SILICON DARLINGTON
AMPLIFIER TRANSISTORS**

... designed for amplifier and driver applications where high gain is an essential requirement, low power lamp and relay drivers and power drivers for high-current applications such as voltage regulators.

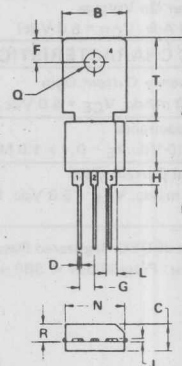
- High DC Current Gain —
 $h_{FE} = 25,000$ (Min) @ $I_C = 200$ mAdc — BD 411
 $= 15,000$ (Min) @ $I_C = 500$ mAdc — BD 411
- Collector-Emitter Breakdown Voltage —
 $BV_{CES} = 40$ Vdc (Min) @ $I_C = 100$ μ Adc
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 1.5$ Vdc (Max) @ $I_C = 1.0$ Adc
- Duowatt Package —
2 Watts Free Air Dissipation @ $T_A = 25^\circ\text{C}$
- Complements to PNP BD 413/414

**NPN SILICON
DARLINGTON AMPLIFIER
TRANSISTORS****MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
*Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
*Collector-Base Voltage	V_{CBO}	50	Vdc
*Emitter-Base Voltage	V_{EBO}	12	Vdc
*Collector Current — Continuous	I_C	2.0	Adc
*Base Current — Continuous	I_B	100	mAdc
*Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0 16	Watts mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/ $^\circ\text{C}$
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
*Solder Temperature, 1/16" from Case for 10 Seconds	—	260	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$



STYLE 1
PIN 1 EMITTER
2 BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 — DC CURRENT GAIN

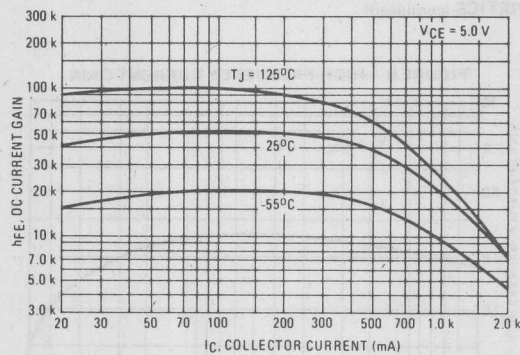


FIGURE 3 — "ON" VOLTAGES

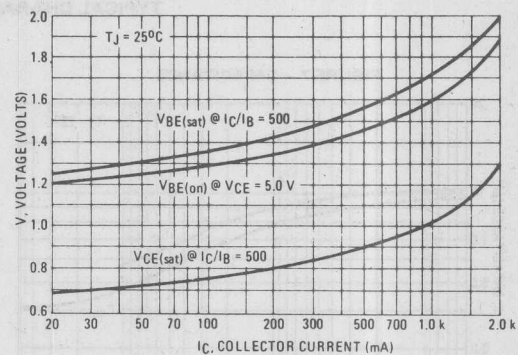


FIGURE 4 — COLLECTOR SATURATION REGION

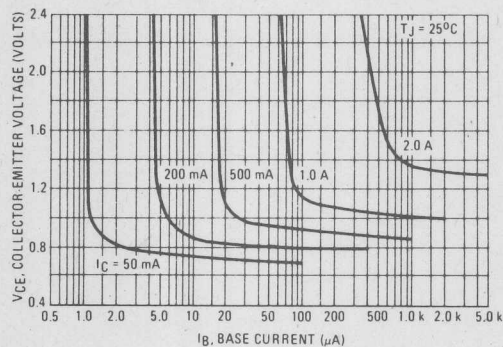


FIGURE 5 — TEMPERATURE COEFFICIENT

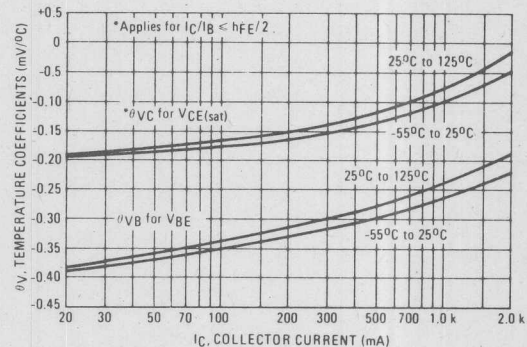
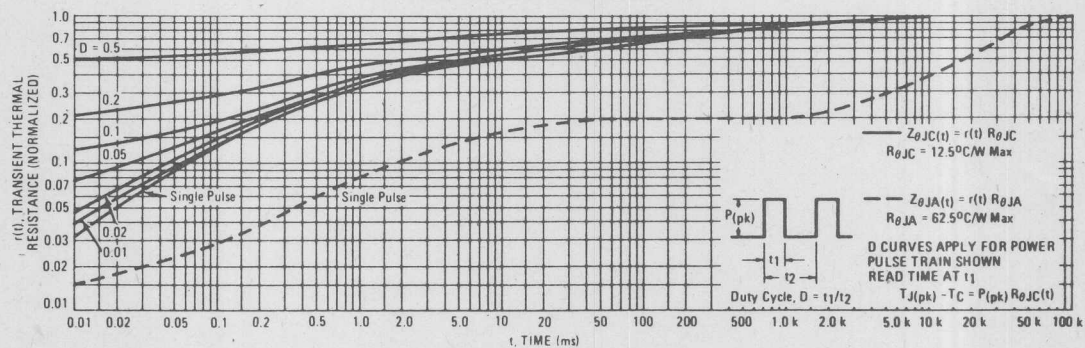


FIGURE 6 — THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 — CAPACITANCE

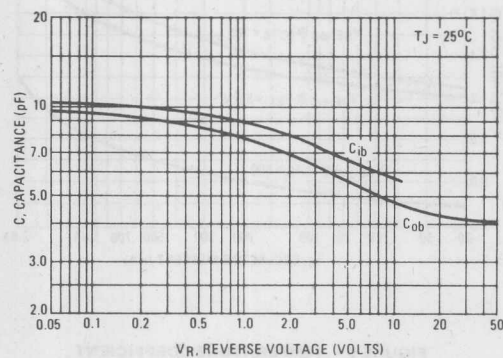
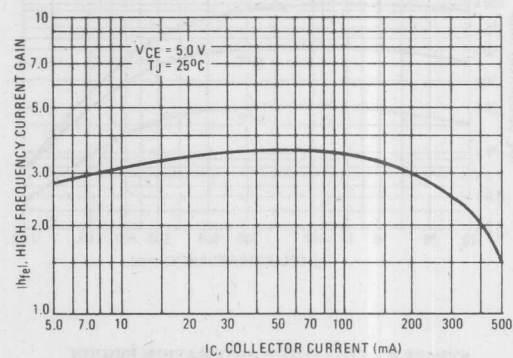


FIGURE 8 — HIGH-FREQUENCY CURRENT GAIN





MOTOROLA

NPN	PNP
BD775	BD776
BD777	BD778
BD779	BD780

PLASTIC DARLINGTON COMPLEMENTARY SILICON ANNULAR[◇] POWER TRANSISTORS

... designed for general purpose amplifier and high-speed switching applications such as hammer drivers for desk calculators.

- High DC Current Gain
 $h_{FE} = 1400$ (Typ) @ $I_C = 2.0$ Adc
- Collector-Emitter Sustaining Voltage — @ 10 mAdc
 V_{CEO} (sus) = 45 Vdc (Min) — BD775, 776
= 60 Vdc (Min) — BD777, 778
= 80 Vdc (Min) — BD779, 780
- Reverse Voltage Protection Diode
- Monolithic Construction with Built-in Base-Emitter output Resistor
- Thermopad II[△] Construction with Hard Solder for High Reliability.

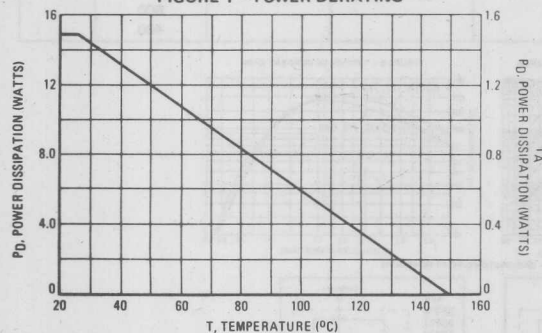
MAXIMUM RATINGS

Rating	Symbol	BD775 BD776	BD777 BD778	BD779 BD780	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous Peak	I_C		4.0 6.0		Adc
Base Current	I_B		100		mAdc
Total Device Dissipation $T_C = 25^\circ\text{C}$ — Derate above 25°C	P_D		15 0.12		Watts W/°C
Operating and Storage junction Temperature Range	T_J, T_{stg} T_J, T_{stg}		— 65 to +150		°C

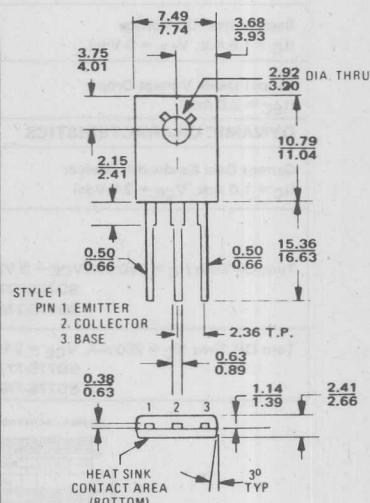
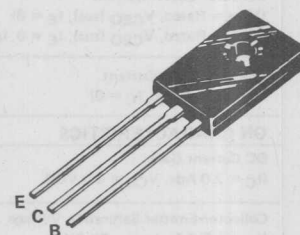
THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W
Thermal Resistance, junction to Ambient	$R_{\theta JA}$	83.3	°C/W

FIGURE 1 — POWER DERATING



DARLINGTON 4-AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 45, 60, 80 VOLTS 15 WATTS



When mounting the device, torque not to exceed 0.07 m·kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
All dimensions in millimeters

CASE 77-04

◇ Annular Semiconductors Patented by Motorola Inc.
△ Trademark of Motorola Inc.

NPN • BD775, BD777, BD779
PNP • BD776, BD778, BD780

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
OFF CHARACTERISTICS				
Collector-Emitter Collector-Emitter Sustaining Voltage (1) ($I_O = 10\text{ mAdc}$, $I_B = 0$) BD775, BD776 BD777, BD778 BD779, BD780	V_{CEO} (sus)	45 60 80		Vdc
Collector Cutoff Current ($V_{CE} = 20\text{ Vdc}$, $I_B = 0$) BD775, BD776 ($V_{CE} = 30\text{ Vdc}$, $I_B = 0$) BD777, BD778 ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) BD779, BD780	I_{CEO}		100 100 100	μAdc
Collector Cutoff Current ($V_{CB} = \text{Rated}$, V_{CEO} (sus), $I_E = 0$) ($V_{CB} = \text{Rated}$, V_{CEO} (sus), $I_E = 0$, $I_C = 100^\circ\text{C}$)	I_{CBO}		1.0 100	μAdc
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}		1.0	μAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 2.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$)	H_{FE}	750		
Collector-Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 6\text{ mAdc}$)	$V_{CE}(\text{Sat})$		1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 6\text{ mAdc}$)	$V_{BE}(\text{Sat})$		2.5	Vdc
Base-Emitter On Voltage ($I_C = 1.5\text{ Adc}$, $V_{CE} = 3\text{ Vdc}$)	$V_{BE}(\text{On})$		2.3	Vdc
Output Diode Voltage Drop ($I_{EC} = 2.0\text{ Adc}$)	V_{EC}		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain Bandwidth Product ($I_C = 1.0\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$)	f_T	20		MHz
Turn-On Time ($I_C = 250\text{ mA/VCE} = 2\text{ V}$) BD775-777-779 BD776-778-780	SYMBOL		TYP.	UNIT
	t_{on}	25	250 250 150	ns
Turn Off Time ($I_C = 250\text{ mA}$, $V_{CE} = 2\text{ V}$) BD775-777-779 BD776-778-780	t_{off}		600 400	ns

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA

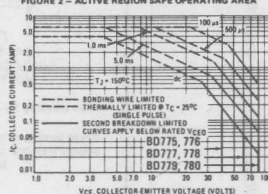


FIGURE 3 - TYPICAL DC CURRENT GAIN

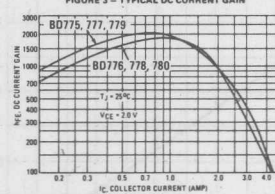
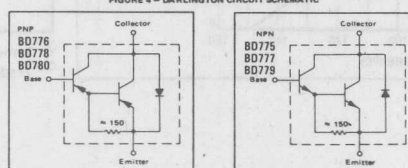


FIGURE 4 - DARLINGTON CIRCUIT SCHEMATIC





MOTOROLA

NPN

BD 785

BD 787

PNP

BD 786

BD 788

COMPLEMENTARY PLASTIC SILICON ANNULAR POWER TRANSISTORS

... designed for low power audio amplifier and low current, high-speed switching applications.

- Low Collector-Emitter Sustaining Voltage –
V_{CEO} (sus) 45 Vdc (Min) – BD785, BD786
60 Vdc (Min) – BD787, BD788
- High Current-Gain – Bandwidth Product –
f_T = 50 MHz (Min) @ I_C = 100 mAdc
- DC Current Gain Specified at 0.2, 1.0, 2.0 and 4.0 Adc
- Collector-Emitter Saturation Voltage Specified at 0.5, 1.0, 2.0 and 4.0 Adc

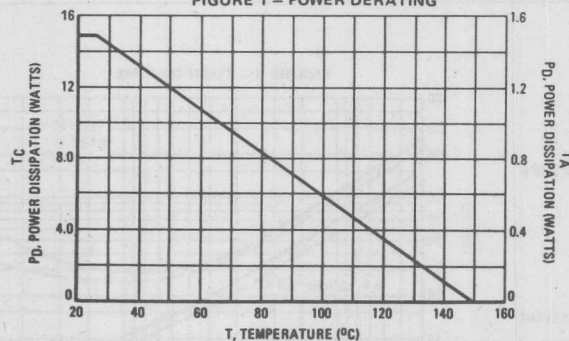
*MAXIMUM RATINGS

Rating	Symbol	BD785 BD786	BD787 BD788	Unit
Collector-Emitter Voltage	V _{CEO}	45	60	Vdc
Collector-Base Voltage	V _{CBO}	60	80	Vdc
Emitter-Base Voltage	V _{EBO}	6.0		Vdc
Collector Current – Continuous	I _C	4.0		Adc
– Peak		8.0		Adc
Base Current	I _B	1.0		Adc
Total Power Dissipation @ T _C = 25°C	P _D	15		Watts
Derate Above 25°C		0.12		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150		°C

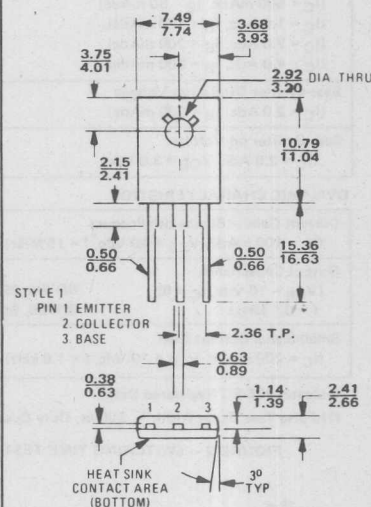
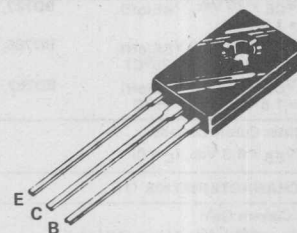
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	8.34	°C/W

FIGURE 1 – POWER DERATING



4 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 45, 60VOLTS 15 WATTS



When mounting the device, torque not to exceed 0.07 m·kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
All dimensions in millimeters

CASE 77-04

NPN • BD785, BD787
PNP • BD786, BD788

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 10 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	45 60	— —	Vdc
Collector Cutoff Current ($V_{CE} = 20 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	100 100	μAdc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$)	I_{CEX}	—	1.0	μAdc
($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$)		—	1.0	
($V_{CE} = 30 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$)		—	0.1	mAdc
($V_{CE} = 40 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$)		—	0.1	
Emitter Cutoff Current ($V_{EB} = 6.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	μAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 200 \text{ mAdc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	40 25 20 5.0	250 — — —	—
Collector-Emitter Saturation Voltage ($I_C = 500 \text{ mAdc}$, $I_B = 50 \text{ mAdc}$) ($I_C = 1.0 \text{ Adc}$, $I_B = 100 \text{ mAdc}$) ($I_C = 2.0 \text{ Adc}$, $I_B = 200 \text{ mAdc}$) ($I_C = 4.0 \text{ Adc}$, $I_B = 800 \text{ mAdc}$)	$V_{CE(sat)}$	— — — —	0.4 0.6 0.8 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 2.0 \text{ Adc}$, $I_B = 200 \text{ mAdc}$)	$V_{BE(sat)}$	—	2.0	Vdc
Base-Emitter on Voltage ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.8	Vdc

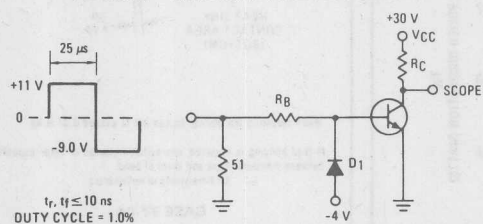
DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product ($I_C = 100 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 10 \text{ MHz}$)	f_T	50	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_C = 0$) $f = 0.1 \text{ MHz}$	C_{ob}	— —	50 70	pF
Small-Signal Current Gain ($I_C = 200 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	10	—	—

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$

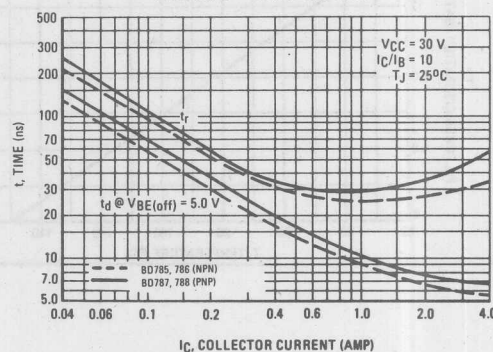
FIGURE 2 — SWITCHING TIME TEST CIRCUIT



D1 MUST BE FAST RECOVERY TYPE, eg:
MB05300 USED ABOVE $I_B \approx 100 \text{ mA}$
MSD6100 USED BELOW $I_B \approx 100 \text{ mA}$

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 — TURN-ON TIME



NPN • BD785, BD787
PNP • BD786, BD788

FIGURE 4 – THERMAL RESPONSE

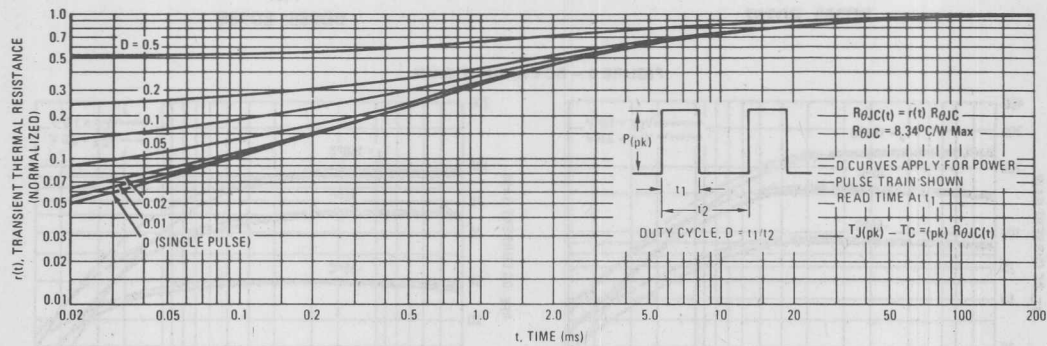
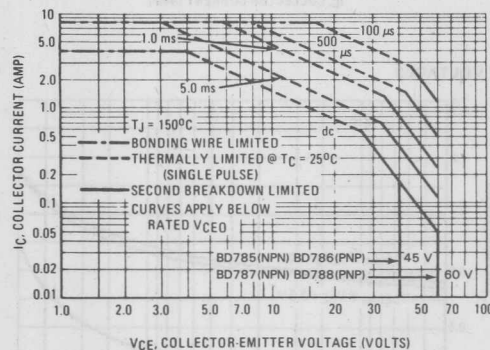


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_J(pk) = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(pk) \leq 150^\circ\text{C}$. $T_J(pk)$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

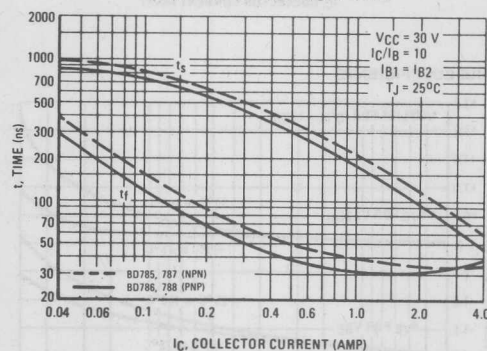
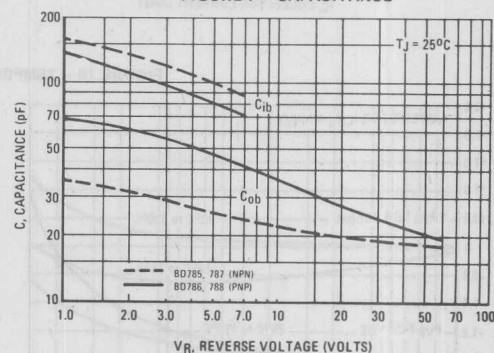


FIGURE 7 – CAPACITANCE



NPN • BD785, BD787
PNP • BD786, BD788

NPN
BD785, BD787

PNP
BD786, BD788

FIGURE 8 - DC CURRENT GAIN

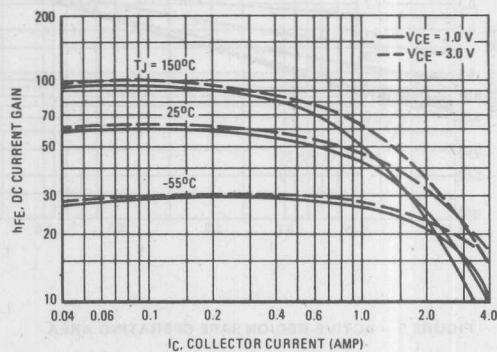
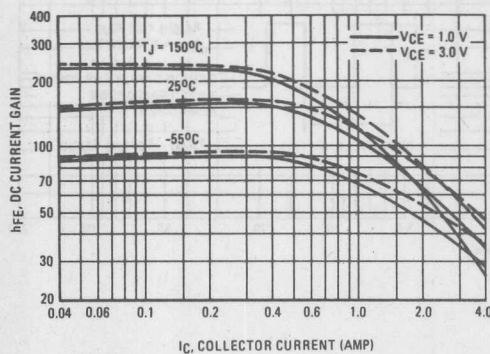


FIGURE 9 - "ON" VOLTAGES

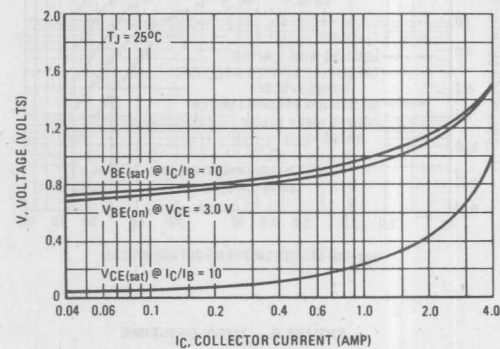
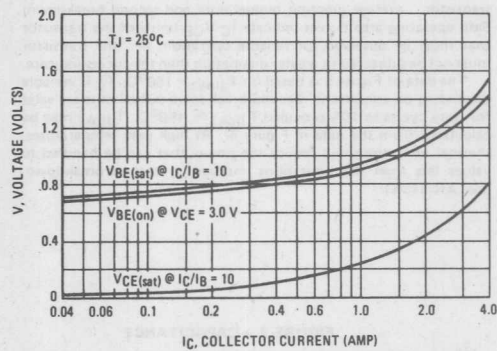
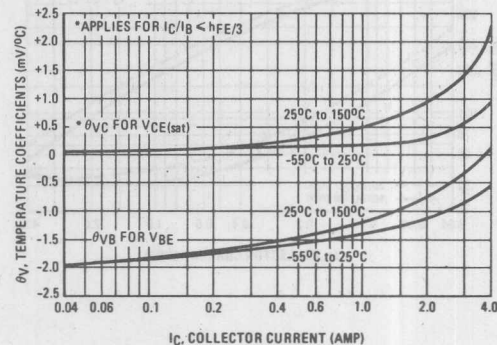
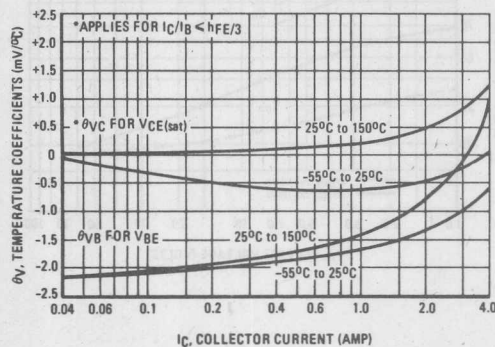


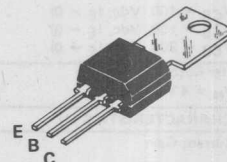
FIGURE 10 - TEMPERATURE COEFFICIENTS



**MOTOROLA****BF466
BF467
BF468****NPN SILICON ANNULAR
HIGH VOLTAGE AMPLIFIER TRANSISTORS**

... designed for horizontal driver applications in television receivers.

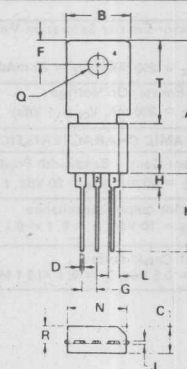
- High Collector-Emitter Breakdown Voltage —
BVCEO = 250 Vdc (min) @ IC = 1.0 mAdc — BF468
- Low Collector-Emitter Saturation Voltage —
VCE(sat) = 1.5 Vdc (max) @ IC = 200 mAdc
- Duowatt Package —
2 Watts Free Air Dissipation @ TA = 25 °C

**NPN SILICON
AMPLIFIER TRANSISTORS****MAXIMUM RATINGS**

Rating	Symbol	BF466	BF467	BF468	Unit
Collector-Emitter Voltage	VCEO	150	200	250	Vdc
Collector-Base Voltage	VCEO	150	200	250	Vdc
Emitter-Base Voltage	VEBO	5			Vdc
Collector Current — Continuous	IC	1			Adc
Collector Current — Peak	IC	2			Adc
Base Current	IB	300			mAdc
Total Power Dissipation @ TA = 25°C	PD	2.0			Watts
Derate above 25°C	PD	16			mW/°C
Total Power Dissipation @ TC = 25°C	PD	10			Watts
Derate above 25°C	PD	80			mW/°C
Operating and Storage Junction Temperature Range	TJ, Tstg	-55 to +150			°C
Solder Temperature, 1/16" from Case for 10 Seconds	—	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	RθJA	62.5	°C/W
Thermal Resistance, Junction to Case	RθJC	12.5	°C/W



STYLE 1
PIN 1 EMITTER
2 BASE
3 COLLECTOR
4 COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}$, $I_B = 0$)	BV_{CEO}	150 200 250	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100 \mu\text{Adc}$, $I_E = 0$)	BV_{CBO}	150 200 250	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{Adc}$, $I_C = 0$)	BV_{EBO}	5	—	Vdc
Collector Cutoff Current ($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 150 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 200 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	— — —	0.1 0.1 0.1	μAdc
Emitter Cutoff Current ($V_{BE} = 4 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 10 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$) ($I_C = 100 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$)	h_{FE}	40 40	—	—
Collector-Emitter Saturation Voltage ($I_C = 200 \text{ mAdc}$, $I_B = 20 \text{ mAdc}$)	$V_{CE(sat)}$	—	1.5	Vdc
Base-Emitter On Voltage ($I_C = 200 \text{ mA}$, $V_{CE} = 1 \text{ Vdc}$)	$V_{BE(on)}$	—	1	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($I_C = 50 \text{ mA}$, $V_{CE} = 20 \text{ Vdc}$, $f = 20 \text{ MHz}$)	f_T	100	—	MHz
Collector output capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	—	12	pF
Input Capacitance ($V_{BE} = 0.5 \text{ Vdc}$, $I_C = 0$, $f = 0.1 \text{ MHz}$)	C_{ib}	—	110	pF

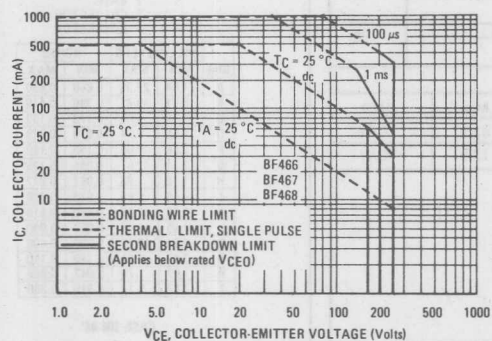


FIGURE 1 — ACTIVE-REGION SAFE-OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

TYPICAL CHARACTERISTICS

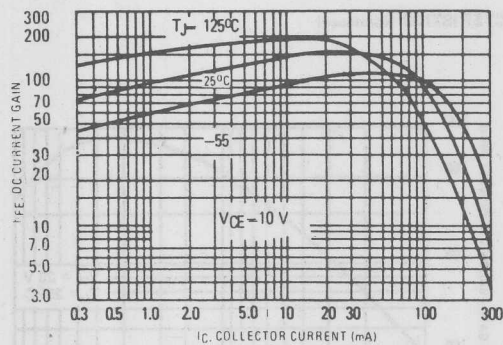


FIGURE 2 - DC CURRENT GAIN

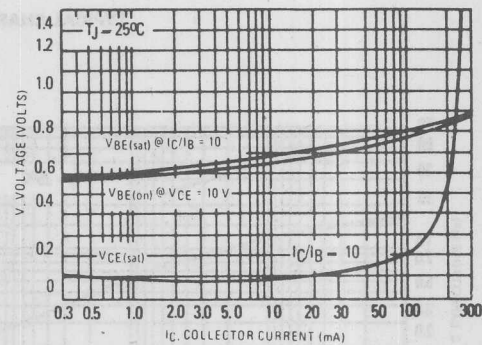


FIGURE 3 - "ON" VOLTAGES

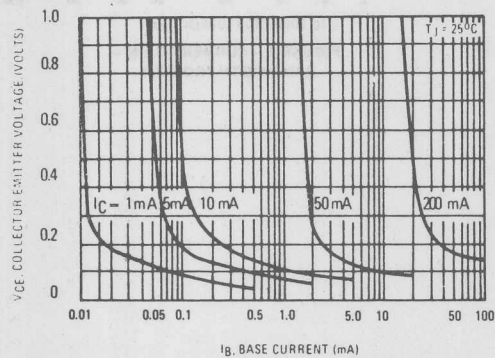


FIGURE 4 - COLLECTOR SATURATION REGION

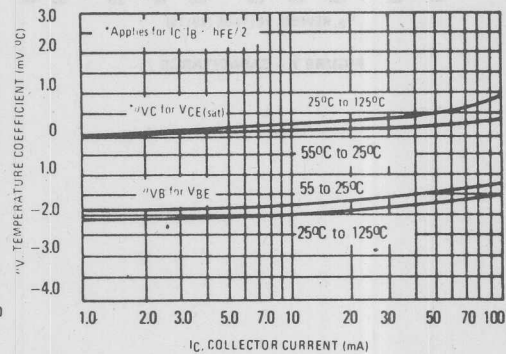


FIGURE 5 - TEMPERATURE COEFFICIENTS

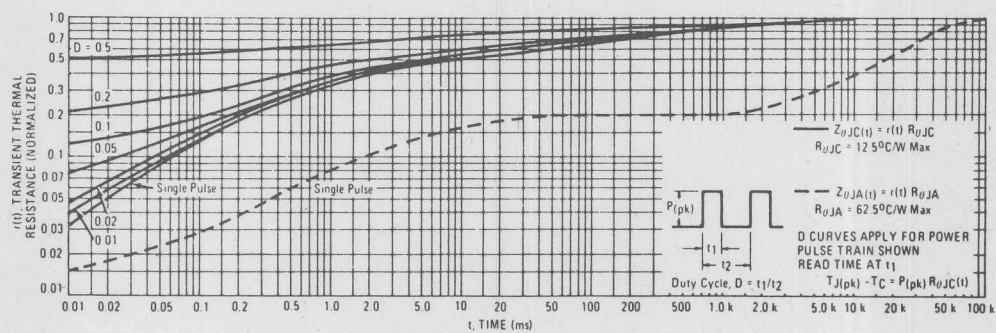


FIGURE 6 - THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

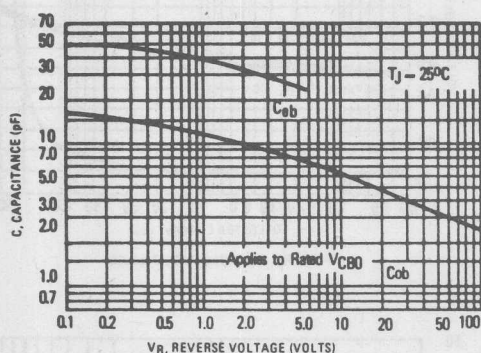


FIGURE 7 - CAPACITANCE

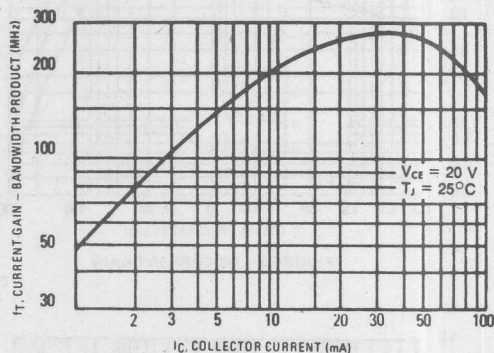


FIGURE 8 - CURRENT-GAIN -
BANDWIDTH PRODUCT

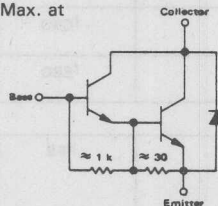
NPN SILICON POWER DARLINGTON TRANSISTOR

The BU323, BU323A are monolithic darlington transistors designed for automotive ignition, switching regulator and motor control applications.

- V_{CE} Sat Specified at $-40^{\circ}\text{C} = 2\text{ V Max. at } I_C = 6\text{ A.}$

- 550 mJ Energy Capability Tested in Automotive Ignition Circuit.

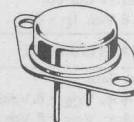
- Photoglass Passivation for Reliability and Stability.



16 AMPERE PEAK

POWER TRANSISTORS DARLINGTON NPN SILICON

350 - 400 VOLTS
175 WATTS

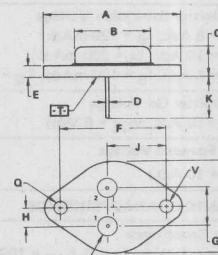


MAXIMUM RATINGS

Rating	Symbol	BU323	BU323A	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	350	400	Vdc
Collector-Base Voltage	V_{CBO}	500	600	Vdc
Emitter-Base Voltage	V_{EBO}	8	8	Vdc
Collector Current — Continuous	I_C	10	10	Adc
Peak (1)		16	16	
Base Current — Continuous	I_B	3	3	Adc
Total Power Dissipation @ $T_C = 25^{\circ}\text{C}$	P_D	175	175	Watts
@ $T_C = 100^{\circ}\text{C}$		100	100	Watts
Derate above 25°C		1	1	W/ $^{\circ}\text{C}$
Operating and Storage Junction	T_J, T_{stg}	-65 to +200		$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	$^{\circ}\text{C/W}$
Maximum Lead Temperature for Soldering	T_L	275	$^{\circ}\text{C}$
Purposes: 1/8" from Case for 5 Seconds			
(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.			



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D.

⌀ 0.13 (0.005) T V

FOR LEADS:

⌀ 0.13 (0.005) T V Q

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.08	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.48 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	26.67	—	1.050
N	4.83	5.33	0.190	0.210
O	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS¹						
Collector-Emitter Sustaining Voltage (Figure 1) $L = 10\text{ mH}$ $(I_C = 200\text{ mA}, I_B = 0, V_{\text{clamp}} = \text{Rated } V_{\text{CEO}})$	BU323 BU323A	$V_{\text{CEO(sus)}}$	350 400			Vdc
Collector-Emitter Sustaining Voltage (Figure 1) $(I_C = 3\text{ A}, R_{\text{BE}} = 100\text{ Ohms}, L = 500\text{ }\mu\text{H})$ Unclamped	BU323 BU323A	$V_{\text{CER(sus)}}$	400 475			Vdc
Collector Cutoff Current (Rated $V_{\text{CER}}, R_{\text{BE}} = 100\text{ Ohms}$)		I_{CER}			1	mA
Collector Cutoff Current (Rated $V_{\text{CBO}}, I_E = 0$)		I_{CBO}			1	mA
Emitter Cutoff Current ($V_{\text{EB}} = 6\text{ Vdc}, I_C = 0$)		I_{EBO}			40	mA
ON CHARACTERISTICS¹						
DC Current Gain $(I_C = 3\text{ A}, V_{\text{CE}} = 6\text{ Vdc})$ $(I_C = 6\text{ A}, V_{\text{CE}} = 6\text{ Vdc})$ $(I_C = 10\text{ A}, V_{\text{CE}} = 6\text{ Vdc})$		h_{FE}	300 150 50	550 350 150	2000	
Collector-Emitter Saturation Voltage $(I_C = 3\text{ A}, I_B = 60\text{ mA})$ $(I_C = 6\text{ A}, I_B = 120\text{ mA})$ $(I_C = 10\text{ A}, I_B = 300\text{ mA})$ $(I_C = 6\text{ A}, I_B = 120\text{ mA}, T_C = -40^\circ\text{C})$		$V_{\text{CE(sat)}}$			1.5 1.7 2.7 2.0	Vdc
Base-Emitter Saturation Voltage $(I_C = 6\text{ A}, I_B = 120\text{ mA})$ $(I_C = 10\text{ A}, I_B = 300\text{ mA})$ $(I_C = 6\text{ A}, I_B = 120\text{ mA}, T_C = -40^\circ\text{C})$		$V_{\text{BE(sat)}}$			2.2 3 2.4	Vdc
Base-Emitter On Voltage $(I_C = 10\text{ A}, V_{\text{CE}} = 6\text{ Vdc})$		$V_{\text{BE(on)}}$			2.5	Vdc
Diode Forward Voltage $(I_F = 10\text{ A})$		V_f		2	3.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}, I_E = 0, f_{\text{test}} = 100\text{ kHz}$)		C_{ob}		165	350	pF
SWITCHING CHARACTERISTICS						
Storage Time ($V_{\text{CC}} = 12\text{ Vdc}, I_C = 6\text{ A}, I_{\text{B1}} = I_{\text{B2}} = 0.3\text{ A}$) Fig. 2		t_s		7.5	15	μs
Fall Time		t_f		5.2	15	μs
FUNCTIONAL TESTS						
Second Breakdown Collector Current with Base-Forward Biased		$I_{\text{S/B}}$		See Figure 10		
Pulsed Energy Test (See Figure 12)		$\frac{I_{\text{C2L}}}{2}$	550			mJ

¹ Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

FIGURE 1 – SUSTAINING VOLTAGE TEST CIRCUIT

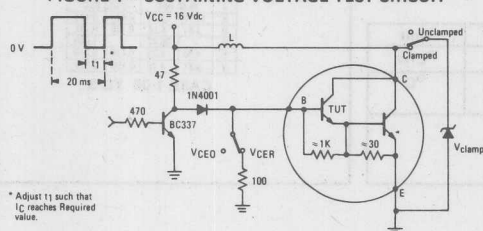


FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

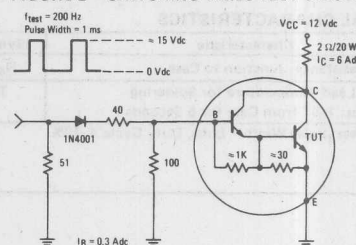


FIGURE 3 — DC CURRENT GAIN

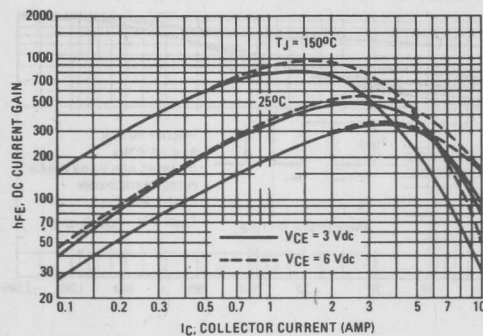


FIGURE 4 — COLLECTOR-SATURATION REGION

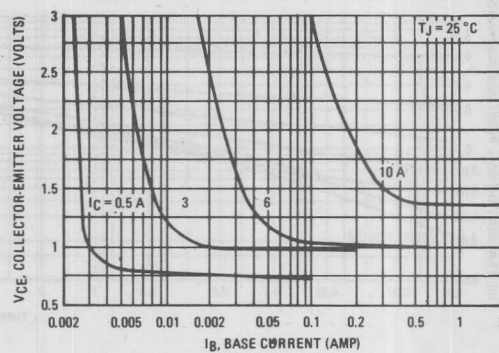


FIGURE 5 — COLLECTOR-EMITTER SATURATION VOLTAGE

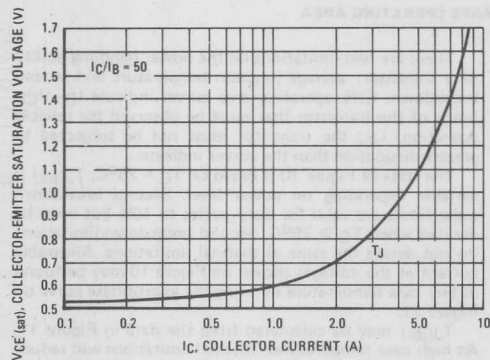


FIGURE 6 — BASE-EMITTER VOLTAGE

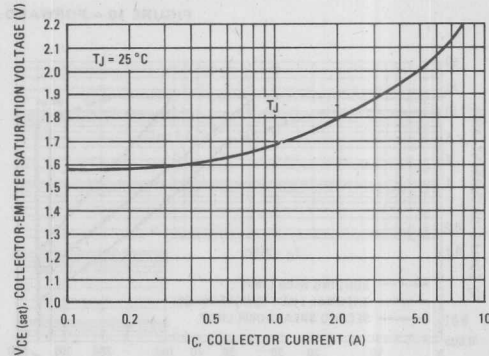


FIGURE 7 — TURN-OFF SWITCHING TIME

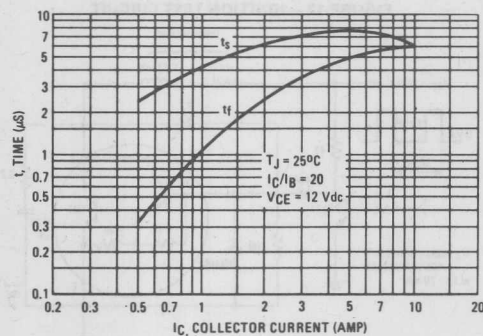
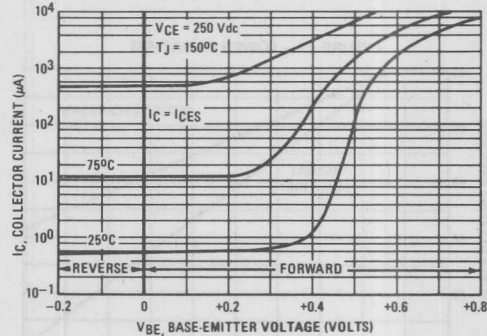


FIGURE 8 — COLLECTOR CUTOFF REGION



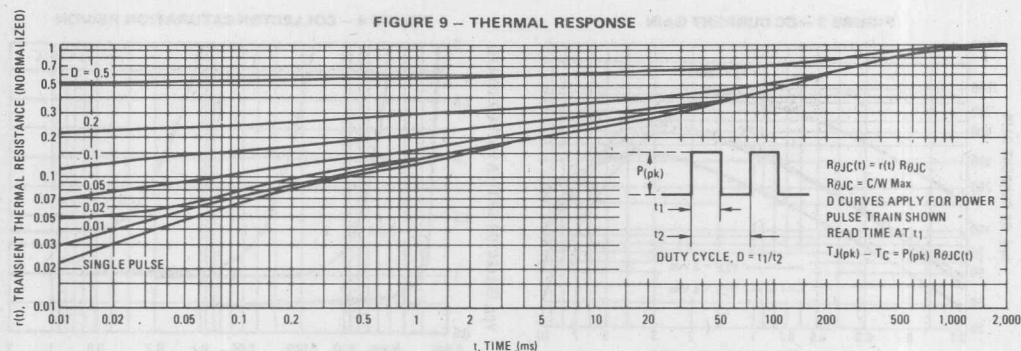
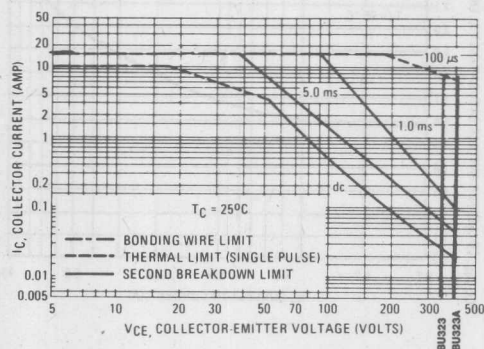


FIGURE 10 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_J(pk)$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING

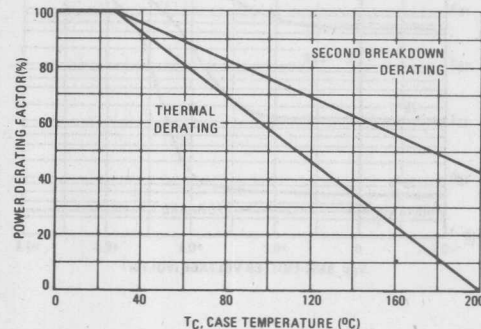
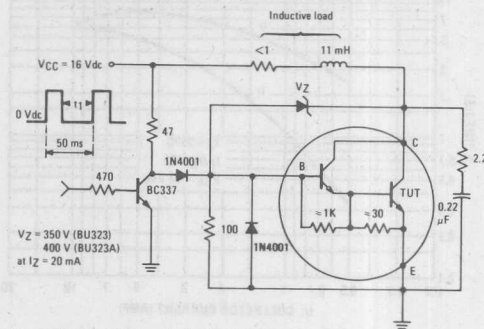


FIGURE 12 – IGNITION TEST CIRCUIT



NOTE: Figure 12 specifies energy handling capabilities in an automotive ignition circuit.

**MOTOROLA**

BU 406 BU 407

HIGH VOLTAGE NPN SILICON TRANSISTOR

... designed for use in the switched mode power supply and television horizontal deflection.

- High Collector-Emitter Voltage
 $V_{CES} = 400 \text{ V}, 330 \text{ V}$
- Collector Current
 $I_C = 7 \text{ Adc}$
- Low Collector Emitter Saturation Voltage
 $V_{CE(sat)} = 1 \text{ Vdc}, @ I_C = 5 \text{ A}, I_B = 0.5 \text{ A}$
- Fall Time @ $I_C = 5 \text{ A}, I_B(\text{end}) = 0.5 \text{ A}, V_{CC} = 40 \text{ V}$
 $t_f = 0.75 \mu\text{s} (\text{max.})$
- TO-66 lead form also available ordered with "-66" suffix

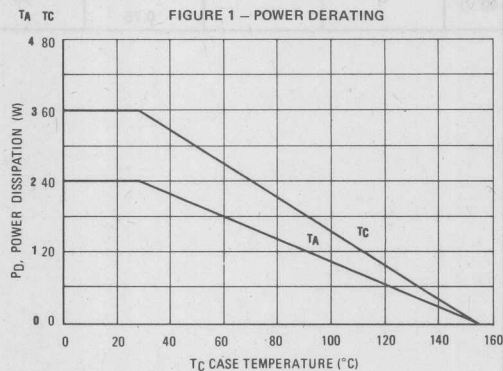
MAXIMUM RATINGS

Rating	Symbol	BU406	BU407	Unit
Collector-Emitter Voltage	V_{CEO}	200	150	Vdc
Collector-Emitter Voltage $V_{BE} = 0$	V_{CES}	400	330	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current - Continuous	I_C	7.0		Adc
- Peak		15.0		
Base Current	I_B	4.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	60		Watts
Derate above 25°C		0.48		W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

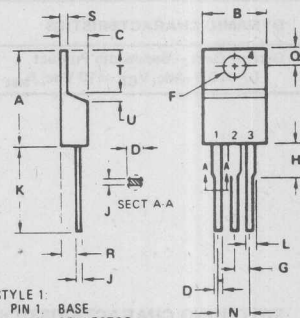
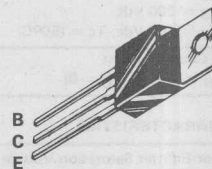
THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	$^\circ\text{C/W}$

FIGURE 1 - POWER DERATING

**7 AMPERES**

NPN SILICON POWER TRANSISTOR

**200, 150 VOLTS
60 WATTS**

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
T	1.14	1.39	0.045	0.055
U	5.97	6.48	0.235	0.255
	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 100\text{ mA}$)	V_{CEO}	200 150		Vdc
Collector Cutoff Current $V_{CES} = 400\text{ Vdc}$ $V_{CES} = 250\text{ Vdc}$ $V_{CES} = 250\text{ Vdc}, T_C = 150^\circ\text{C}$ $V_{CES} = 330\text{ Vdc}$ $V_{CES} = 200\text{ Vdc}$ $V_{CES} = 200\text{ Vdc}, T_C = 150^\circ\text{C}$	I_{CES}		5 0.1 1 5 0.1 1	mAdc
Emitter Cutoff Current ($V_{EB} = 6\text{ Vdc}, I_C = 0$)	I_{EBO}		1	mAdc
ON CHARACTERISTICS				
Collector-Emitter Saturation Voltage ($I_C = 5\text{ Adc}, I_B = 0.5\text{ Adc}$)	$V_{CE(sat)}$	—	1.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 5\text{ Adc}, I_B = 0.5\text{ Adc}$)	$V_{BE(sat)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($I_C = 0.5\text{ Adc}, V_{CE} = 10\text{ Vdc}, f_{test} = 1.0\text{ MHz}$)	f_T	10		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Fall Time	($I_C = 5\text{ Adc}, I_{B1} = I_{B2} = 0.5\text{ Adc}, V_{CC} = 40\text{ V}$)	t_f	0.75	μs
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(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 – DC CURRENT GAIN

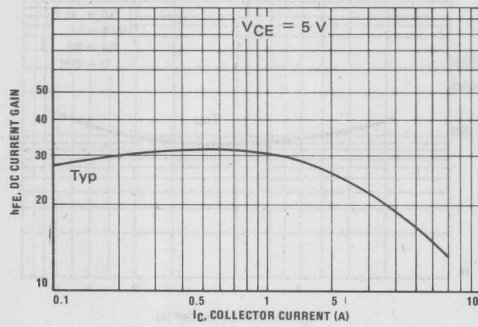


FIGURE 3 – COLLECTOR SATURATION REGION

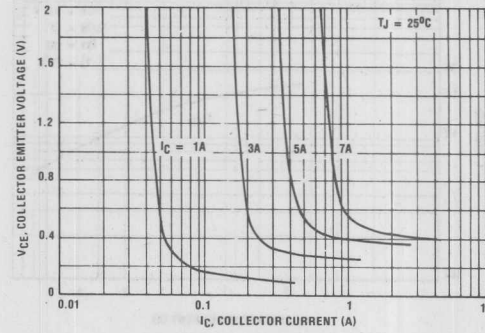


FIGURE 4 – "SATURATION" AND "ON" VOLTAGES

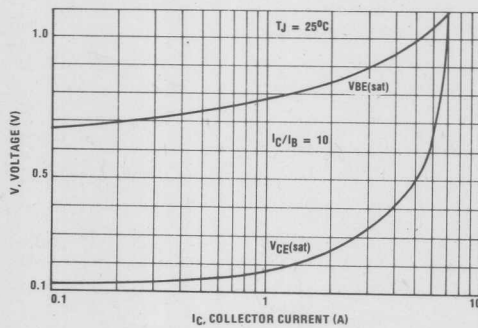


FIGURE 5 – FORWARD BIAS SAFE OPERATING AREA

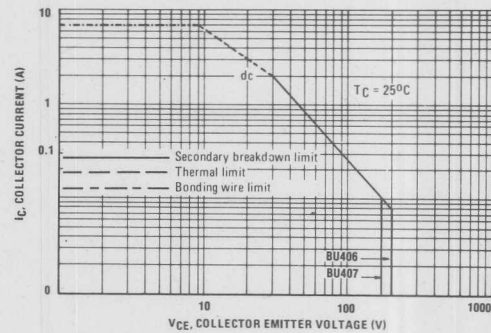


FIGURE 7 — STORAGE TIME

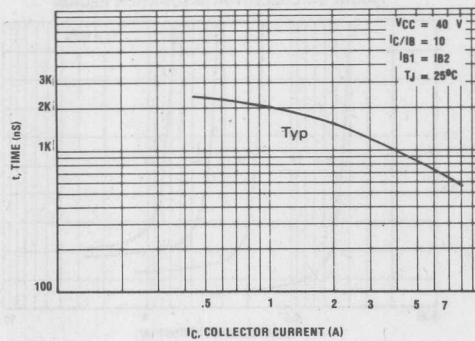
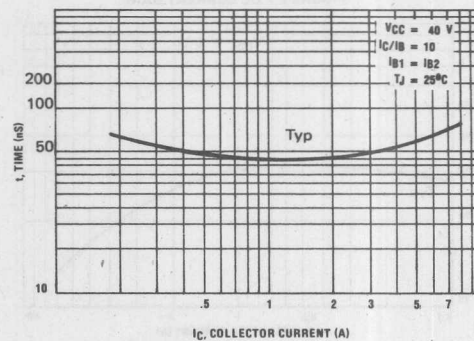


FIGURE 8 — FALL TIME



**MOTOROLA****BU 522
BU 522A
BU 522B****HIGH VOLTAGE SILICON POWER DARLINGTONS**

Power Transistor mainly intended for use as ignition circuit output transistor.

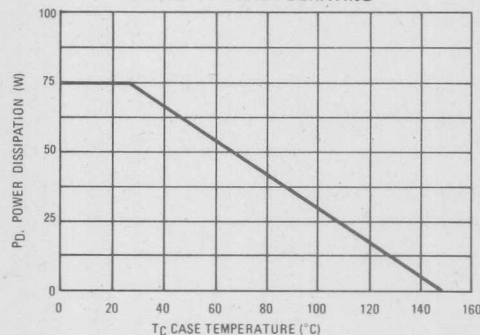
- Specified minimum sustaining voltage:
 $V_{CE(sus)} = 350 \text{ V (BU522)}$
 at $I_C = 1 \text{ A}$ 400 V (BU522A)
 425 V (BU522B)
- High S.O.A. capability:
 $V_{CE} = 350 \text{ V (BU522) at } I_C = 5 \text{ A}$
 400 V (BU522A, BU522B)
- Low $V_{CE(sat)} = 2.0 \text{ V max. at } I_C = 4 \text{ A (BU522A, BU522B)}$

MAXIMUM RATINGS

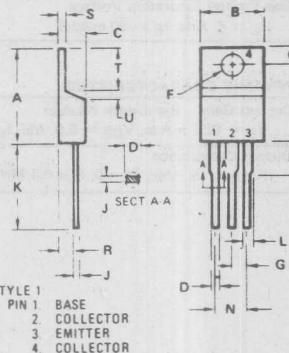
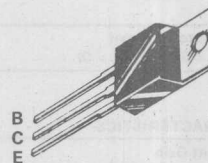
Rating	Symbol	BU522	BU522A	BU522B	Unit
Collector-Emitter Voltage Sust.	$V_{CE(sus)}$	350	400	425	Vdc
Collector-Emitter Voltage	V_{CE}	375	425	450	Vdc
Collector-Base Voltage	V_{CB}	400	450	475	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current - Continuous	I_C	7.0			Adc
Base Current	I_B	2.0			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.60			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

FIGURE 1 - POWER DERATING**7 AMPERES****DARLINGTON
TRIPLE DIFFUSED
POWER TRANSISTORS
NPN SILICON**

375, 425, 450 VOLTS
75 WATTS



STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
O	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

**ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (See Figure 2) ($I_C = 1.0\text{ A}$) See Figure 2	$V_{CE(sus)}$				Vdc
BU522		350			
BU522A		400			
BU522B		425			
Collector Cutoff Current (Rated V_{CE} , $R_{BE} = 270\ \Omega$)	I_{CER}			1.0	mA _{dc}
Collector Cutoff Current (Rated V_{CB} , $I_E = 0$)	I_{CBO}			1.0	mA _{dc}
Emitter Cutoff Current ($V_{EB} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}			40	mA _{dc}

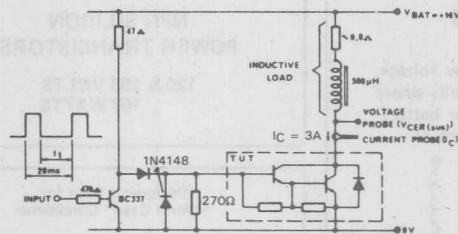
ON CHARACTERISTICS

DC Current Gain ($I_C = 2.5\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	250			—
Collector-Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 80\text{ mA}$)	$V_{CE(sat)}$			2.5 2	Vdc
Base-Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 80\text{ mA}$)	$V_{BE(sat)}$			2.5	Vdc

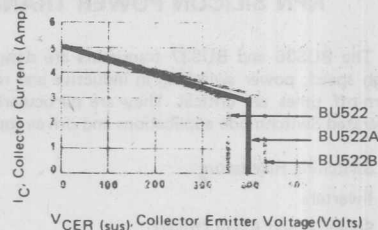
DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ($I_C = 0.3\text{ mA}$, $V_{CE} = 5.0\text{ Vdc}$, $f_{test} = 1.0\text{ MHz}$)	f_T		7.5		MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}		150		pF

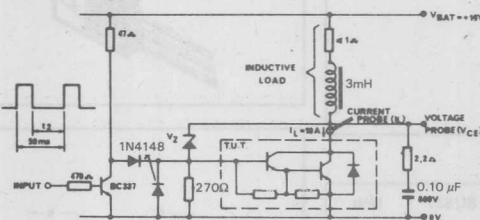
FIGURE 2 - SUSTAINING VOLTAGE TEST $V_{CER(sus)}$



t_1 to be selected that I_C reaches 3 Adc before switch-off
Case temperature of the power transistor: $T_C = 25^\circ\text{C}$



Test conditions of the Collector-Base Clamping Circuit:



Clamping device characteristics:

$V_Z = 350\text{ V (BU522)} \pm 1\% \text{ at } I_Z = 20\text{ mA}$
 400 V (BU522A/B)

Clamping duration is around $45\text{ }\mu\text{sec (BU522)}$
 $40\text{ }\mu\text{sec (BU522A/B)}$

t_2 to be selected that I_L reaches
5 Adc before switch-off

Case temperature of the power
transistor: $T_C = 25^\circ\text{C}$.

FIGURE 3 - S.O.A. TEST

**MOTOROLA****BUS 36
BUS 37****SWITCHMODE II[▲] SERIES
NPN SILICON POWER TRANSISTORS**

The BUS36 and BUS37 transistors are designed for low voltage, high speed, power switching in inductive and resistive circuits where turn-off times are critical. They are particularly suited for battery-operated Switchmode applications and driver applications such as :

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

Fast Turn-Off Times

60 ns Inductive Fall Time – 25°C (Typ)

110 ns Inductive Crossover Time – 25°C (Typ)

Operating Temperature Range – 65 to + 175°C

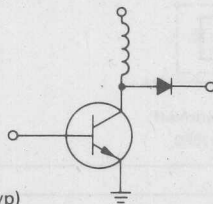
100°C Performance Specified for :

Reverse-Biased SOA with Inductive Loads

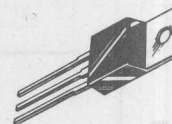
Switching Times with Inductive Loads

Saturation Voltages

Leakage Currents (125°C)

**12 AMPERES****NPN SILICON
POWER TRANSISTORS****120 & 150 VOLTS
107 WATTS****Designer's Data for
"Worst Case" Conditions**

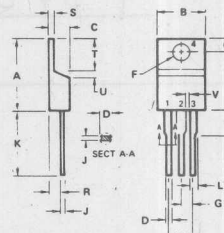
The Designers[▲] Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

**MAXIMUM RATINGS**

Rating	Symbol	BUS36	BUS37	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	120	150	Vdc
Collector-Emitter Voltage	V_{CEV}	250	300	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous	I_C	12		Adc
– Peak(1)	I_{CM}	25		
– Overload		40		
Base Current – Continuous	I_B	7		Adc
– Peak(1)	I_{BM}	15		
Total Power Dissipation – $T_C = 25^\circ\text{C}$	P_D	107		Watts
– $T_C = 100^\circ\text{C}$		53		
Derate above 25°C		0.71		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to + 175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.85	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.84	0.89	0.035	0.035
F	3.81	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.565
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

**CASE 221A-02
TO-220**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 50\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	BUS36 BUS37	$V_{CE(sus)}$ 120 150	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 125^\circ\text{C}$)		I_{CEV} — —	— —	0.1 1.0	mAdc
Collector Cutoff Current BUS36 : $V_{CE} = 60\text{ V}$ BUS37 : $V_{CE} = 75\text{ V}$		I_{CEO} — —	— —	0.05 0.05	mAdc
Emitter Cutoff Current ($V_{EB} = 6\text{ Vdc}$, $I_C = 0$)		I_{EBO}		0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50\text{ mA}$ - $I_C = 0$)		BV_{EBO} 8.0			Vdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$) ($I_C = 0.5\text{ Amp}$, $V_{CE} = 2\text{ V}$)	h_{FE}	30 50	— —	— —	—
Collector-Emitter Saturation Voltage ($I_C = 12\text{ Amp}$, $I_B = 1.2\text{ Amp}$) ($I_C = 12\text{ Amp}$, $I_B = 1.2\text{ Amp}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— —	— —	0.8 1.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 12\text{ Amp}$, $I_B = 1.2\text{ Amp}$) ($I_C = 12\text{ Amp}$, $I_B = 1.2\text{ Amp}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.8 1.8	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	—	—	300	pF
Current Gain — Bandwidth Product (2) ($I_C = 1.0\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f_{\text{test}} = 1.0\text{ MHz}$)	f_T	30	—	—	MHz

SWITCHING CHARACTERISTICS**Resistive Load (Table 1)**

Delay Time	(VCC = 100 Vdc, $I_C = 12\text{ A}$, $I_{B1} = 1.2\text{ A}$, $t_p = 30\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$, $V_{BE(off)} = 5\text{ V}$)	t_d	—	0.07	0.15	μs
Rise Time		t_r	—	0.15	0.3	
Storage Time		t_s	—	0.5	1.0	
Fall Time		t_f	—	0.12	0.25	

Inductive Load, Clamped (Table 1)

Storage Time	$(I_{C(pk)} = 12\text{ A},$ $I_{B1} = 1.2\text{ A},$ $V_{BE(off)} = 5\text{ V},$ $V_{CE(c1)} = 100\text{ V})$	$(T_C = 25^\circ\text{C})$	t_{sv}	—	0.5	—	μs
Fall Time			t_{fi}	—	0.06	—	
Storage Time		$(T_C = 100^\circ\text{C})$	t_{sv}	—	0.6	1.0	
Fall Time			t_{fi}	—	0.15	0.30	

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

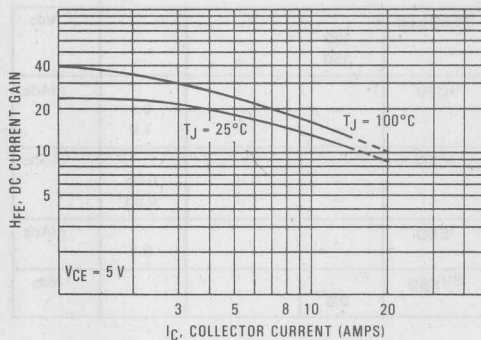


FIGURE 2 — COLLECTOR SATURATION REGION

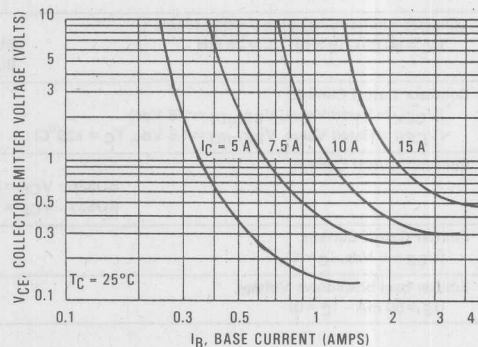


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

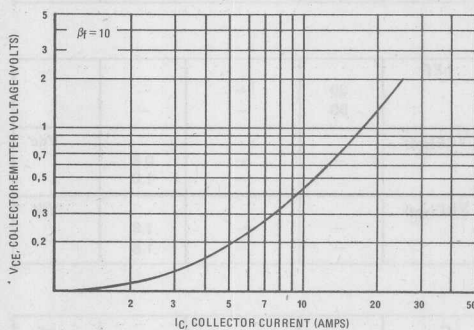


FIGURE 4 — BASE-EMITTER VOLTAGE

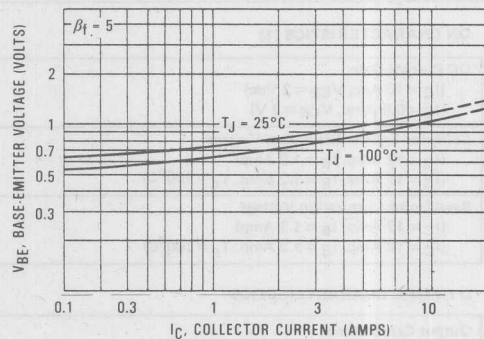


FIGURE 5 — COLLECTOR CUTOFF REGION

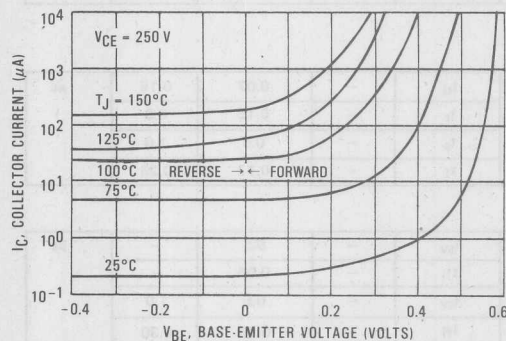


FIGURE 6 — CAPACITANCE

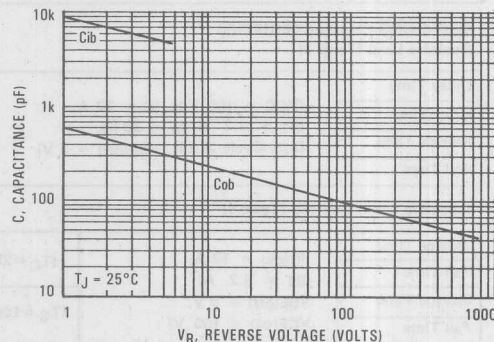


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

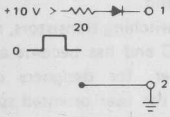
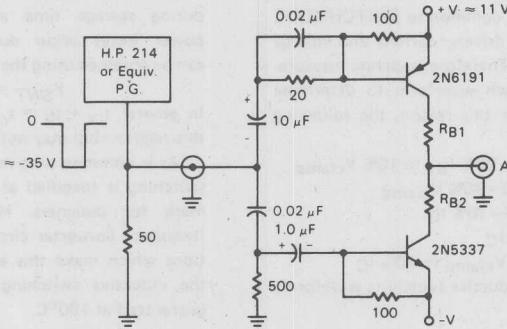
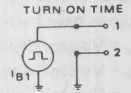
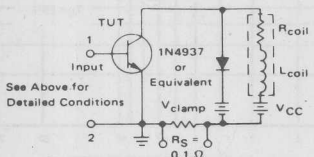
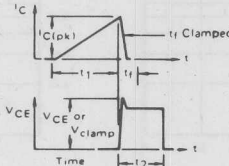
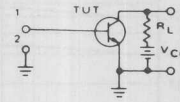
	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>	 <p>Adjust R_1 to obtain I_{B1} For switching and R_{BSOA}, $R_2 = 0$ For $BV_{CEO(sus)}$, $R_2 = \infty$</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 100 \text{ V}$ R_B adjusted to attain desired I_{B1}	$V_{CC} = 100 \text{ V}$ $R_L = 83 \Omega$ Pulse Width = $10 \mu\text{s}$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

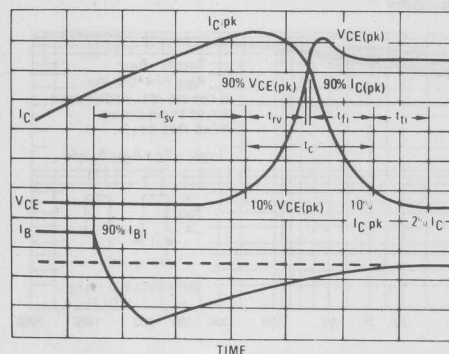
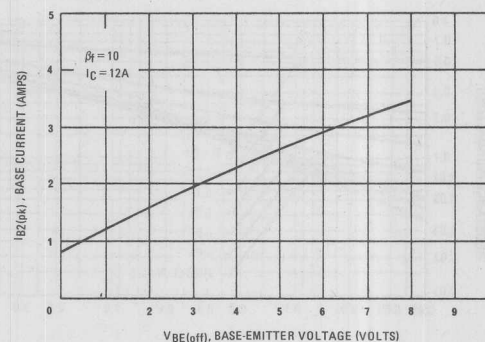


FIGURE 8 — PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME, T_{sv}

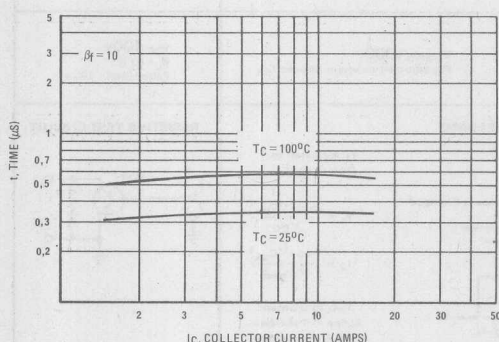


FIGURE 10 — FALL TIMES

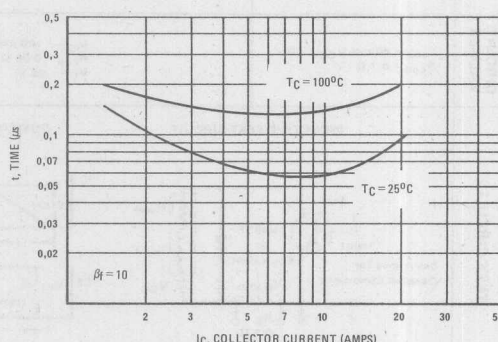
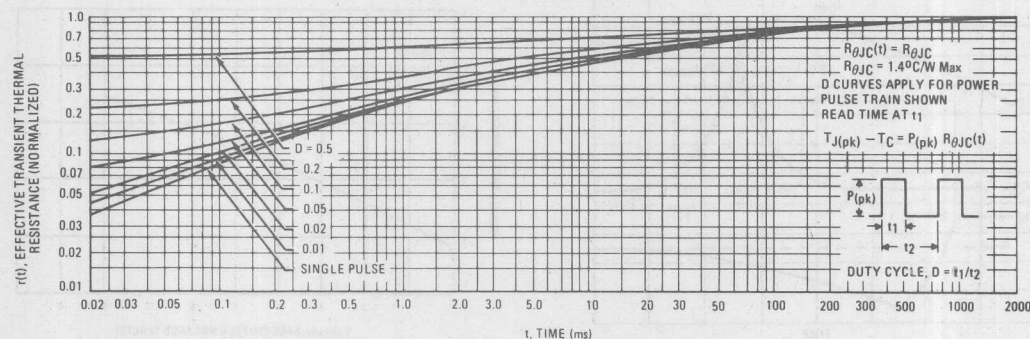


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 11a — TURN-OFF TIMES vs FORCED GAIN

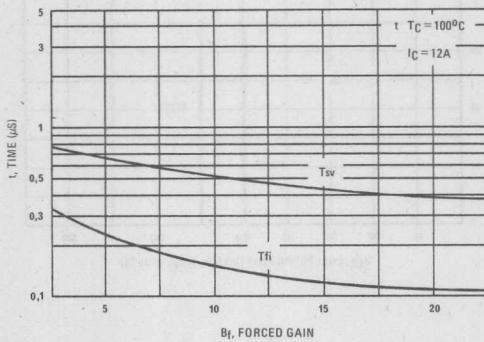


FIGURE 11b — TURN-OFF TIMES vs I_{B2}/I_{B1}

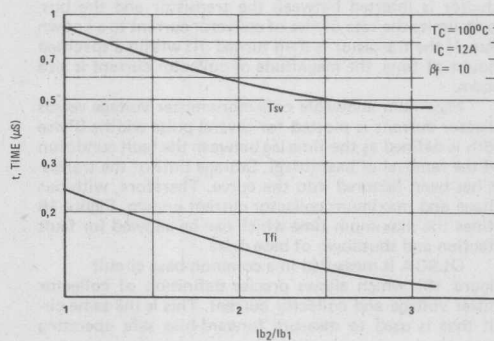
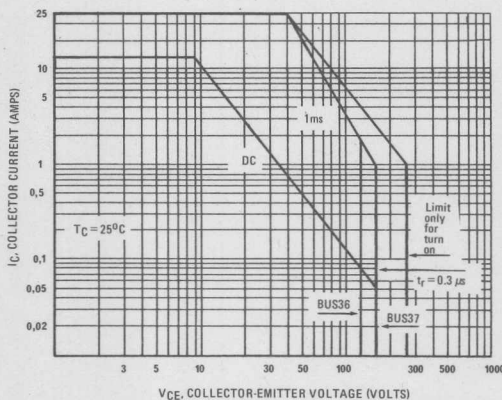


FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ C$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(pk)$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

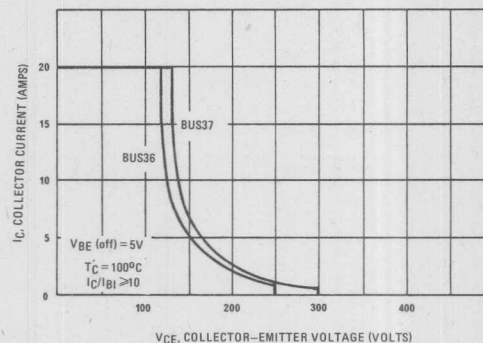


FIGURE 14 — POWER DERATING

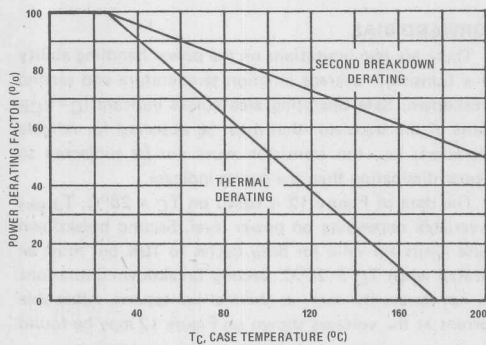
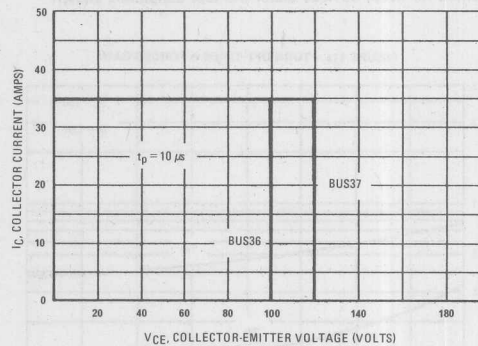


FIGURE 15 — RATED OVERLOAD SAFE OPERATING AREA (OLSOA)



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths (Pulse width is defined as the time lag between the fault condition and the removal of base drive). Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.



SWITCHMODE II SERIES NPN SILICON POWER TRANSISTORS

The BUS 45P transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

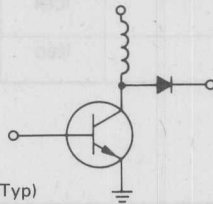
Fast Turn-Off Times

- 100 ns Inductive Fall Time—25°C (Typ)
- 150 ns Inductive Crossover Time—25°C (Typ)
- 400 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range —65 to +150°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

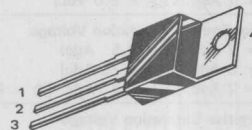


3 AMPERES NPN SILICON POWER TRANSISTORS

450 VOLTS
75 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



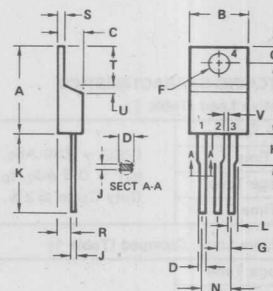
MAXIMUM RATINGS

Rating	Symbol	BUS 45P	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6	Vdc
Collector Current — Continuous	I_C	3	Adc
— Peak (1)	I_{CM}	5	
Base Current — Continuous	I_B	1.5	Adc
— Peak (1)	I_{BM}	3	
Total Power Dissipation — $T_C = 25^\circ\text{C}$	P_D	75	Watts
Derate above 25°C			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	—65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.84	0.89	0.035	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

CASE 221A-02
TO 220

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ V}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ V}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.5 2.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ V}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 2\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	6	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 3\text{ Adc}$, $I_B = 0.75\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc

SWITCHING CHARACTERISTICS**Resistive Load (Table 1)**

Delay Time	(VCC = 250 Adc, $I_C = 2\text{ A}$, $I_{B1} = 0.5\text{ Adc}$, $t_p = 30\ \mu\text{s}$, Duty Cycle $\leq 2\%$, $V_{BE(off)} = 5.0\text{ Vdc}$)	t_d	—	0.03	0.05	μs
Rise Time		t_r	—	0.10	0.40	
Storage Time		t_s	—	0.40	1.50	
Fall Time		t_f	—	0.175	0.50	

Inductive Load, Clamped (Table 1)

Storage Time	(I _{C(pk)} = 2 A, $I_{B1} = 0.5\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 250\text{ V}$)	(T _J = 100°C)	t_{sv}	—	0.70	2.0	μs
Crossover Time			t_c	—	0.28	0.50	
Fall Time			t_{fi}	—	0.15	0.35	
Storage Time		(T _J = 25°C)	t_{sv}	—	0.40	—	
Crossover Time			t_c	—	0.15	—	
Fall Time			t_{fi}	—	0.10	—	

(1) Pulse Test: PW = 300 μs , Duty Cycle $\leq 2\%$.

$$\beta_f = \frac{I_C}{I_B}$$



SWITCHMODE II SERIES NPN SILICON POWER TRANSISTORS

The BUS 46P transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

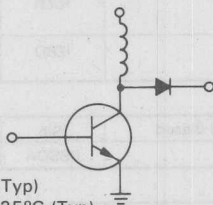
Fast Turn-Off Times

- 100 ns Inductive Fall Time—25°C (Typ)
- 150 ns Inductive Crossover Time—25°C (Typ)
- 400 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range –65 to +150°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



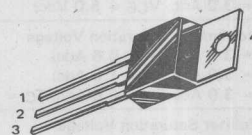
5 AMPERES

NPN SILICON
POWER TRANSISTORS

450 VOLTS
80 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



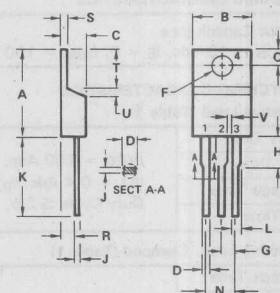
MAXIMUM RATINGS

Rating	Symbol	BUS 46P	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6	Vdc
Collector Current — Continuous	I_C	5	Adc
— Peak (1)	I_{CM}	8	
Base Current — Continuous	I_B	2	Adc
— Peak (1)	I_{BM}	4	
Total Power Dissipation — $T_C = 25^\circ\text{C}$	P_D	80	Watts
— $T_C = 100^\circ\text{C}$			
Derate above 25°C			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—

STYLE 1:
PIN 1: BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-02
TO 220

**ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (1)

Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ V}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ V}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.5 2.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ V}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$			See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	$RBSOA$			See Figure 13	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.0	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ KHz}$)	C_{ob}	—	—	250	pF
--	----------	---	---	-----	----

SWITCHING CHARACTERISTICS**Resistive Load (Table 1)**

Delay Time	(VCC = 250 Adc, $I_C = 3.0\text{ Adc}$, $I_{B1} = 0.4\text{ Adc}$, $t_p = 30\ \mu\text{s}$, Duty Cycle $\leq 2\%$, $V_{BE(off)} = 5.0\text{ Vdc}$)	t_d	—	0.03	0.05	μs
Rise Time		t_r	—	0.10	0.40	
Storage Time		t_s	—	0.40	1.50	
Fall Time		t_f	—	0.175	0.50	

Inductive Load, Clamped (Table 1)

Storage Time	$I_{C(pk)} = 3.0\text{ A}$, $I_{B1} = 0.4\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 250\text{ V}$	$(T_J = 100^\circ\text{C})$	t_{sv}	—	0.70	2.0	μs
Crossover Time			t_c	—	0.28	0.50	
Fall Time			t_{fi}	—	0.15	0.30	
Storage Time		$(T_J = 25^\circ\text{C})$	t_{sv}	—	0.40	—	
Crossover Time			t_c	—	0.15	—	
Fall Time			t_{fi}	—	0.10	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

$$\beta_f = \frac{I_C}{I_B}$$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

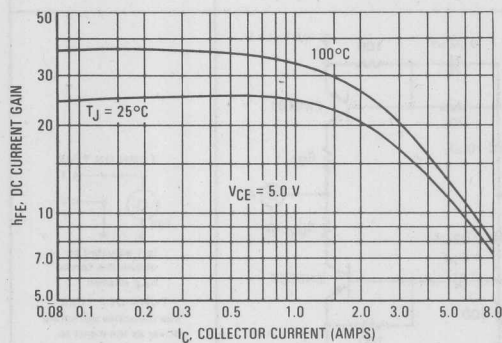


FIGURE 2 — COLLECTOR SATURATION REGION

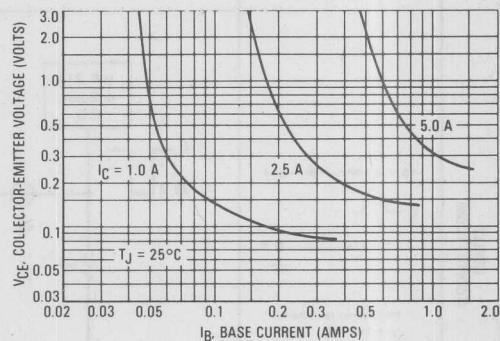


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

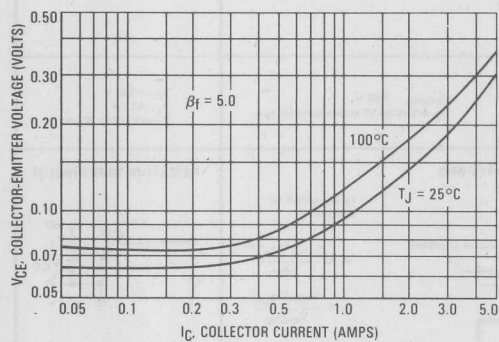


FIGURE 4 — BASE-EMITTER VOLTAGE

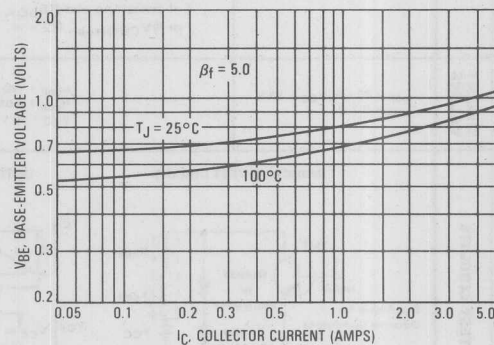


FIGURE 5 — COLLECTOR CUTOFF REGION

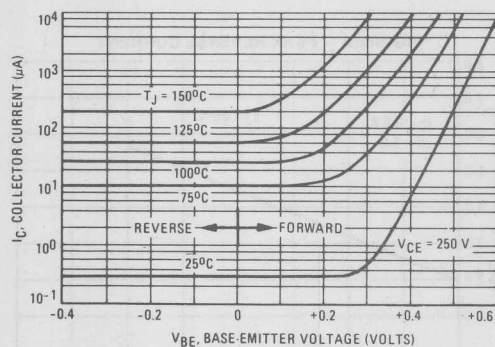


FIGURE 6 — CAPACITANCE

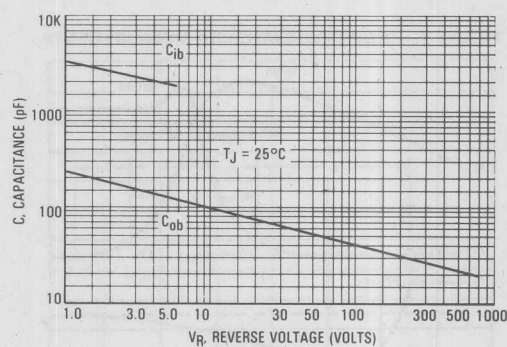


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

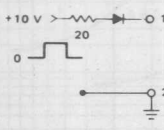
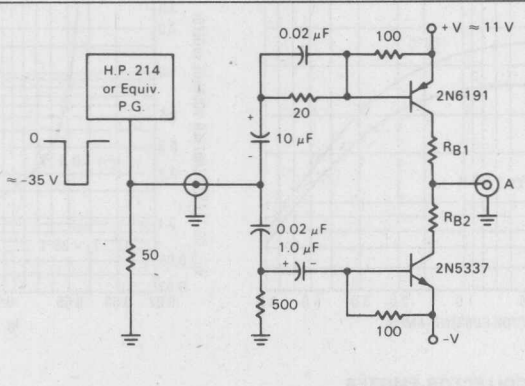
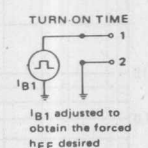
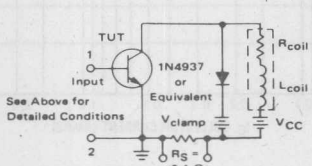
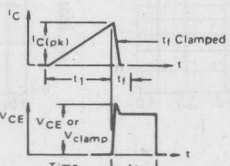
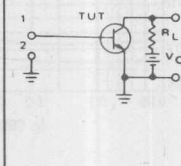
	$V_{CE(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>	 <p>Adjust R_1 to obtain I_{B1} For switching and R_{BSOA}, $R_2 = 0$ For $BV_{CEO(sus)}$, $R_2 = \infty$</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 250 \text{ V}$ R_B adjusted to attain desired I_{B1}	$V_{CC} = 250 \text{ V}$ $R_L = 83 \Omega$ Pulse Width = $10 \mu\text{s}$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

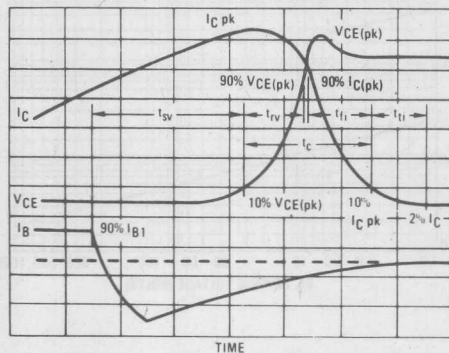
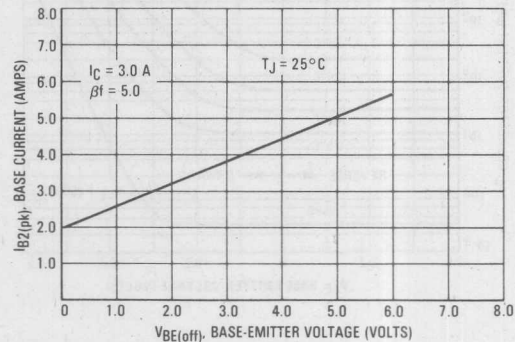


FIGURE 8 - PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

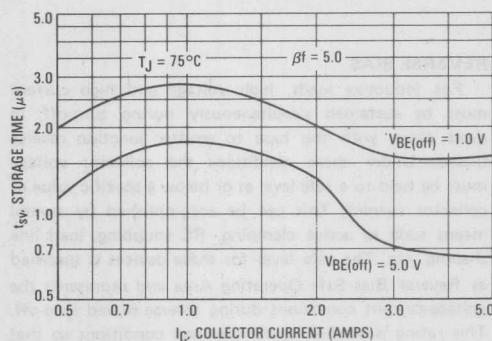


FIGURE 10 — CROSSOVER AND FALL TIMES

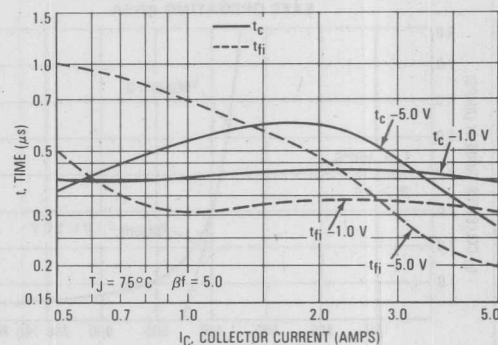
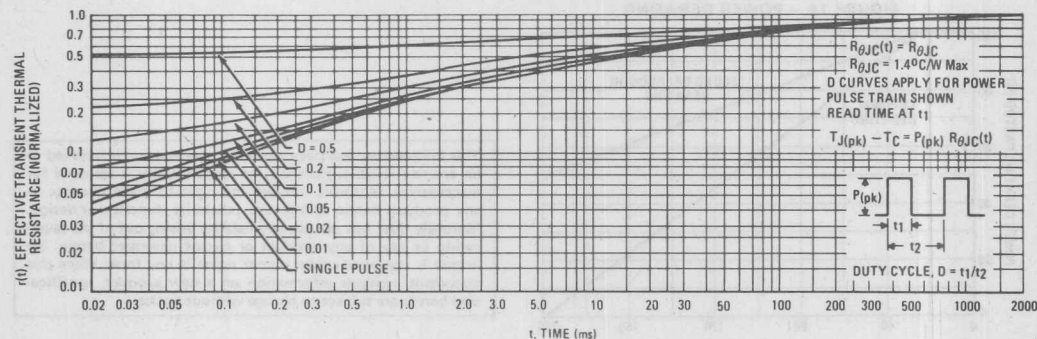


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

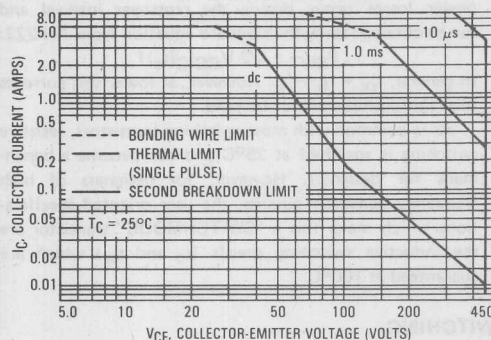


FIGURE 13 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

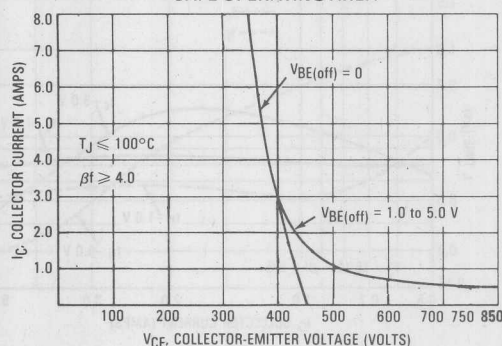
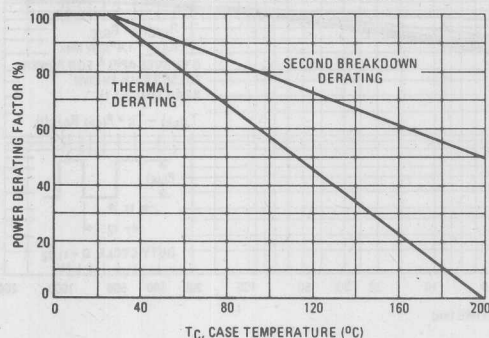


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

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**MOTOROLA****BUS 47
BUS 47A****SWITCHMODE II[▲] SERIES
NPN SILICON POWER TRANSISTORS**

The BUS 47 and BUS 47A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

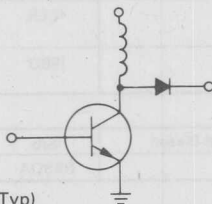
Fast Turn-Off Times

- 100 ns Inductive Fall Time—25°C (Typ)
- 150 ns Inductive Crossover Time—25°C (Typ)
- 400 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

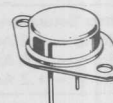
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

**9 AMPERES
NPN SILICON
POWER TRANSISTORS**

450 VOLTS - $V_{CE(sus)}$
150 WATTS
850 VOLTS - V_{CES}

**Designer's Data for
"Worst Case" Conditions**

The Designers[▲] Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

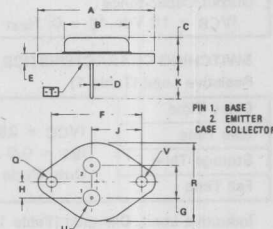
**MAXIMUM RATINGS**

Rating	Symbol	BUS 47	BUS 47A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous	I_C	9		Adc
— Peak (1)	I_{CM}	12		
Base Current — Continuous	I_B	3		Adc
— Peak (1)	I_{BM}	6		
Total Power Dissipation — $T_C = 25^\circ\text{C}$	P_D	150		Watts
— $T_C = 100^\circ\text{C}$		85.5		
Derate above 25°C		0.86		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.52 BSC	—	0.410 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	2.87	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3 TYPE

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCEO(sus)	450	—	—	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 100°C)	ICEV	—	—	0.5 2.5	mAdc
Collector Cutoff Current (VCE = Rated VCEV, RBE = 50 Ω, TC = 100°C)	ICER	—	—	3.0	mAdc
Emitter Cutoff Current (VEB = 6 Vdc, IC = 0)	IEBO	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	IS/b	—	See Figure 12	—
Clamped Inductive SOA with Base Reverse Biased	RBSOA	—	See Figure 13	—

ON CHARACTERISTICS (1)

DC Current Gain (IC = 6 Adc, VCE = 5 Vdc)	hFE	6	—	—	—
Collector-Emitter Saturation Voltage (IC = 6 Adc, IB = 1.2 Adc) (IC = 9 Adc, IB = 3.0 Adc) (IC = 6 Adc, IB = 1.2 Adc, TC = 100°C)	VCE(sat)	— — —	— — —	1.5 3.0 2.5	Vdc
Base-Emitter Saturation Voltage (IC = 6 Adc, IB = 1.2 Adc) (IC = 6 Adc, IB = 1.2 Adc, TC = 100°C)	VBE(sat)	— —	— —	1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (VCB = 10 Vdc, IE = 0, ftest = 100 KHz)	Cob	—	—	300	pF
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SWITCHING CHARACTERISTICS
Resistive Load (Table 1)

Delay Time	(VCC = 250 Vdc, IC = 6 A, IB1 = 0.9 A, tp = 30 μs, Duty Cycle ≤ 2%, VBE(off) = 5 V)	td	—	0.025	0.05	μs
Rise Time		tr	—	0.10	0.50	
Storage Time		ts	—	0.50	1.50	
Fall Time		tf	—	0.10	0.40	

Inductive Load, Clamped (Table 1)

Storage Time	(IC(pk) = 6 A, IB1 = 0.9 A, VBE(off) = 5 V, VCE(pk) = 250 V)	(TC = 25°C)	tstv	—	0.40	—	μs
Crossover Time		(TC = 25°C)	tc	—	0.15	—	
Storage Time		(TC = 100°C)	tstv	—	0.75	2.2	
Crossover Time		(TC = 100°C)	tc	—	0.20	0.40	
Fall Time			tft	—	0.17	0.35	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

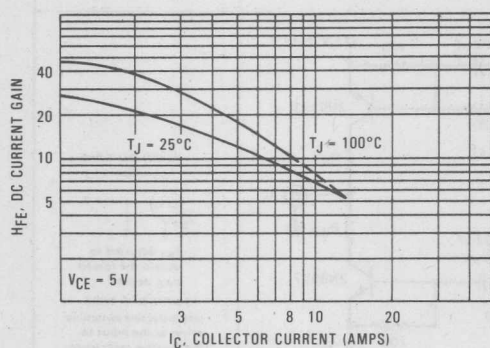


FIGURE 2 — COLLECTOR SATURATION REGION

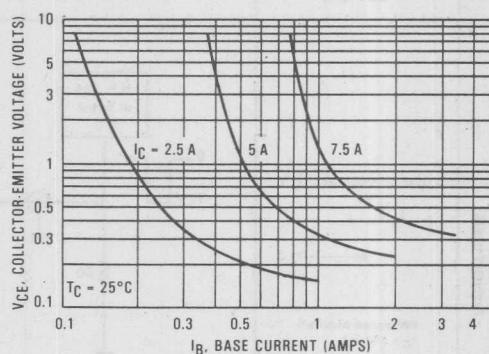


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

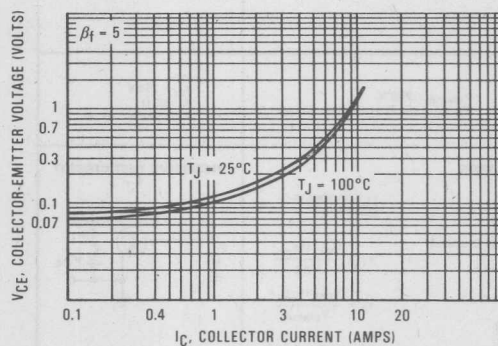


FIGURE 4 — BASE-EMITTER VOLTAGE

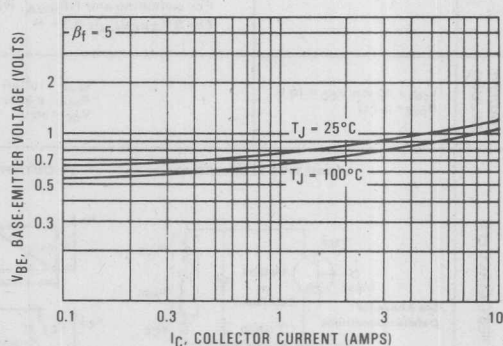


FIGURE 5 — COLLECTOR CUTOFF REGION

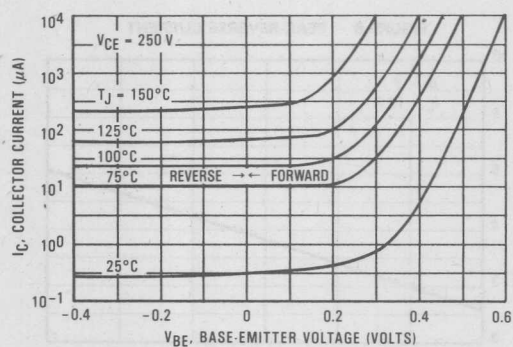


FIGURE 6 — CAPACITANCE

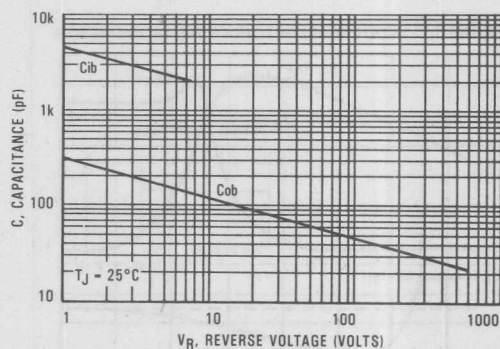


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

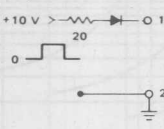
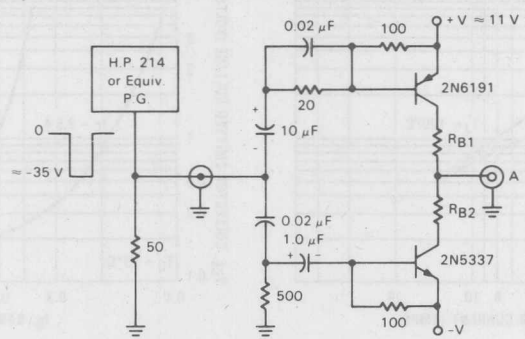
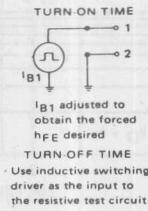
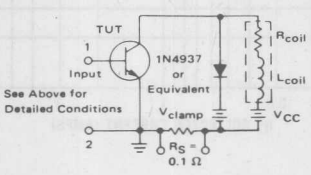
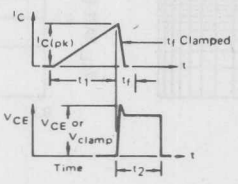
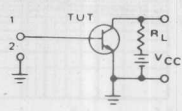
	V _{CEO} (sus)	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>	 <p>Adjust R_1 to obtain I_{B1} For switching and R_{BSOA}, $R_2 = 0$ For $V_{CEO}(sus)$, $R_2 = \infty$</p>	 <p>TURN-ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 250 \text{ V}$ R_B adjusted to attain desired I_{B1}	$V_{CC} = 250 \text{ V}$ $R_L = 83 \Omega$ Pulse Width = $10 \mu\text{s}$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> $t_1 = \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 = \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

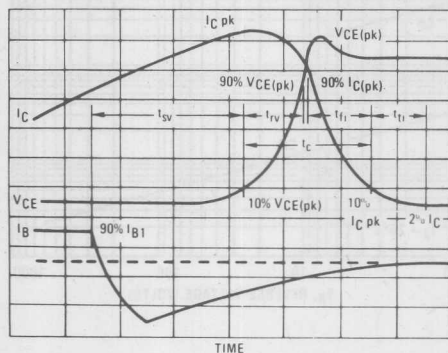
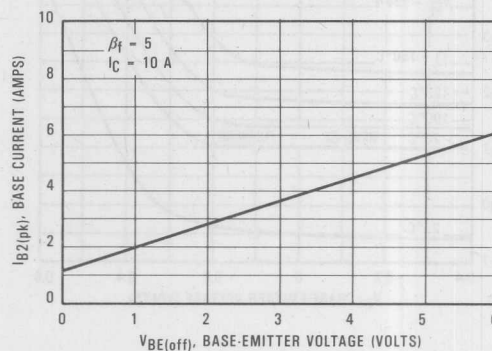


FIGURE 8 - PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

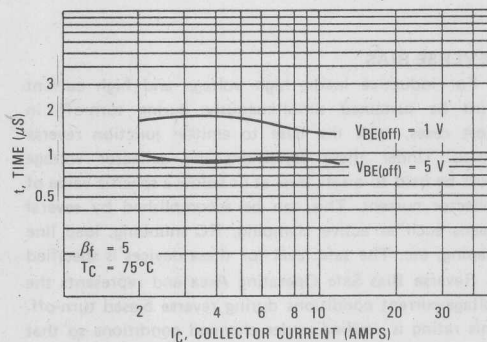
FIGURE 9 — STORAGE TIME, T_{sv} 

FIGURE 10 — CROSSOVER AND FALL TIMES

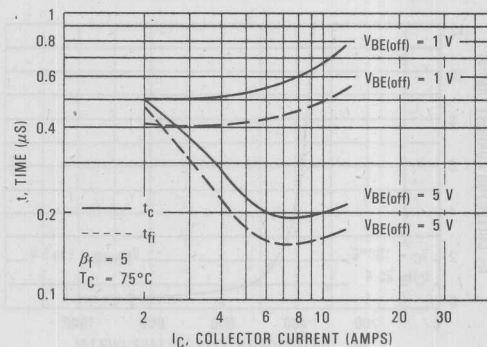
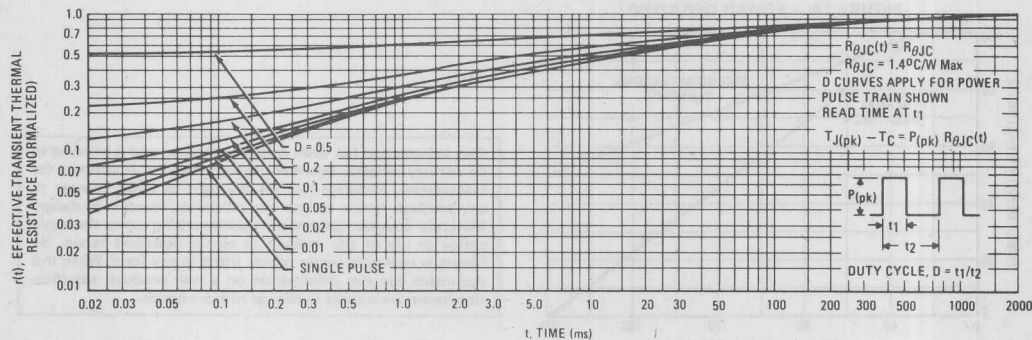
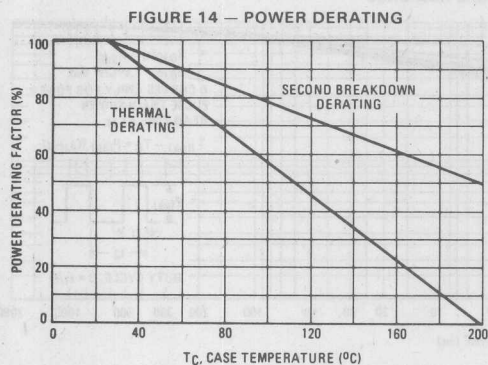
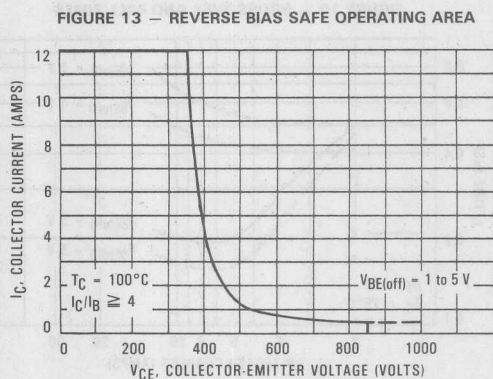
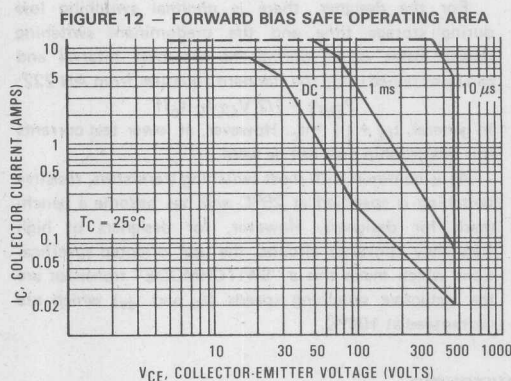


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

This information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein. No license is conveyed under patent rights in any form. When this document contains information on a new product, specification herein are subject to change without notice.

**MOTOROLA****BUS 47P
BUS 47AP****SWITCHMODE II⁺ SERIES
NPN SILICON POWER TRANSISTORS**

The BUS 47P/BUS 47AP transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

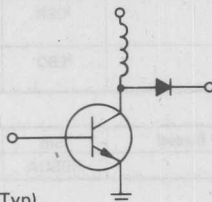
Fast Turn-Off Times

- 100 ns Inductive Fall Time—25°C (Typ)
- 150 ns Inductive Crossover Time—25°C (Typ)
- 400 ns Inductive Storage Time—25°C (Typ)

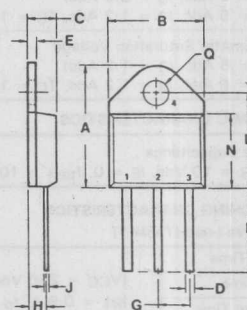
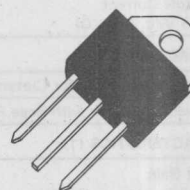
Operating Temperature Range -65 to +150°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

**9 AMPERES
NPN SILICON
POWER TRANSISTORS**

450 VOLTS - $V_{CE(sus)}$
107 WATTS
850 VOLTS - V_{CES}



STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	BUS 47P	BUS 47AP	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	450	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous	I_C	9		Adc
— Peak (1)	I_{CM}	12		
Base Current — Continuous	I_B	3		Adc
— Peak (1)	I_{BM}	6		
Total Power Dissipation — $T_C = 25^\circ\text{C}$	P_D	107		Watts
— $T_C = 100^\circ\text{C}$		85.5		
Derate above 25°C		0.86		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.


ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.5 2.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 6\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12
Clamped Inductive SOA with Base Reverse Biased	$RBSOA$	See Figure 13

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 6\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	6	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 6\text{ Adc}$, $I_B = 1.2\text{ Adc}$) ($I_C = 9\text{ Adc}$, $I_B = 3.0\text{ Adc}$) ($I_C = 6\text{ Adc}$, $I_B = 1.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.5 3.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 6\text{ Adc}$, $I_B = 1.2\text{ Adc}$) ($I_C = 6\text{ Adc}$, $I_B = 1.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ KHz}$)	C_{ob}	—	—	300	pF
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SWITCHING CHARACTERISTICS
Resistive Load (Table 1)

Delay Time	(VCC = 250 Vdc, $I_C = 6\text{ A}$, $I_{B1} = 0.9\text{ A}$, $t_p = 30\ \mu\text{s}$, Duty Cycle $\leq 2\%$, $V_{BE(off)} = 5\text{ V}$)	t_d	—	0.025	0.05	μs
Rise Time		t_r	—	0.10	0.50	
Storage Time		t_s	—	0.50	1.50	
Fall Time		t_f	—	0.10	0.40	

Inductive Load, Clamped (Table 1)

Storage Time	(IC(pk) = 6 A, $I_{B1} = 0.9\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $V_{CE(pk)} = 250\text{ V}$)	($T_C = 25^\circ\text{C}$)	t_{sv}	—	0.40	—	μs
Crossover Time		($T_C = 25^\circ\text{C}$)	t_c	—	0.15	—	
Storage Time		($T_C = 100^\circ\text{C}$)	t_{sv}	—	0.75	2.2	
Crossover Time		($T_C = 100^\circ\text{C}$)	t_c	—	0.20	0.40	
Fall Time			t_{fi}	—	0.17	0.35	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

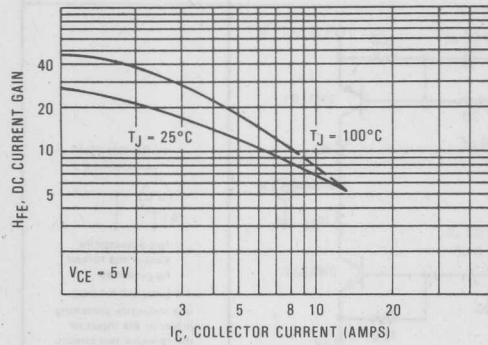


FIGURE 2 — COLLECTOR SATURATION REGION

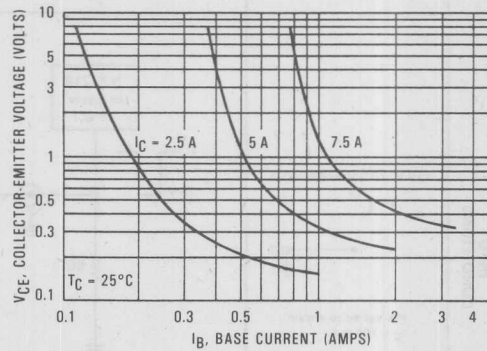


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

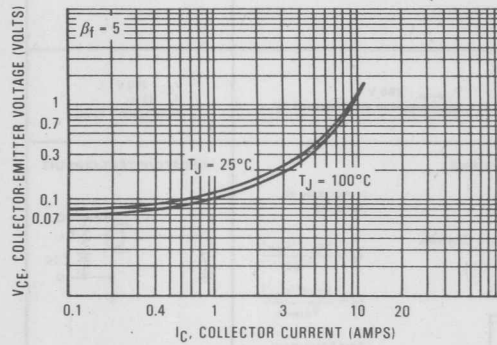


FIGURE 4 — BASE-EMITTER VOLTAGE

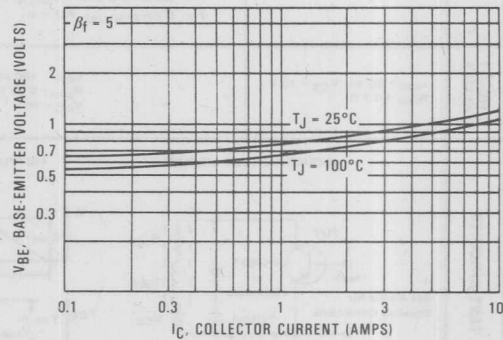


FIGURE 5 — COLLECTOR CUTOFF REGION

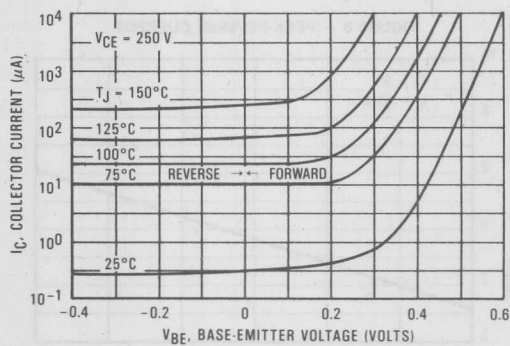


FIGURE 6 — CAPACITANCE

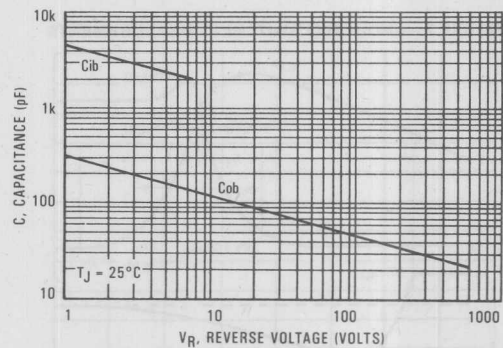


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

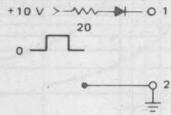
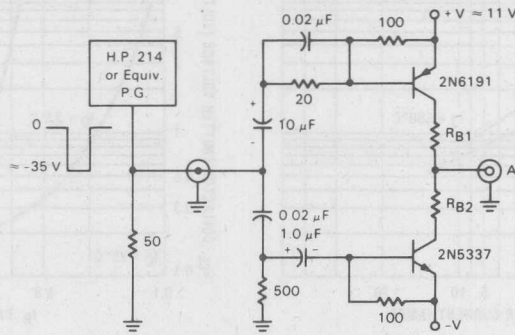
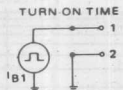
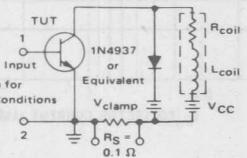
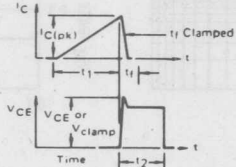
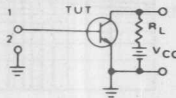
	V _{CEO(sus)}	RB _{SOA} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>	 <p>Adjust R₁ to obtain I_{B1} For switching and R_{BSOA}, R₂ = 0 For BV_{CEO(sus)}, R₂ = ∞</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced hFE desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}</p>	<p>V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

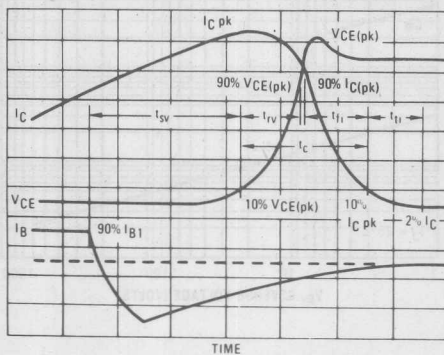
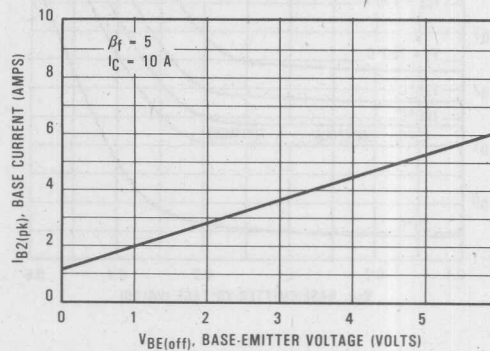


FIGURE 8 – PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME, T_{sv}

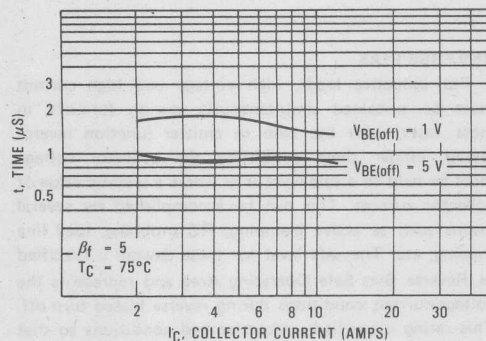


FIGURE 10 — CROSSOVER AND FALL TIMES

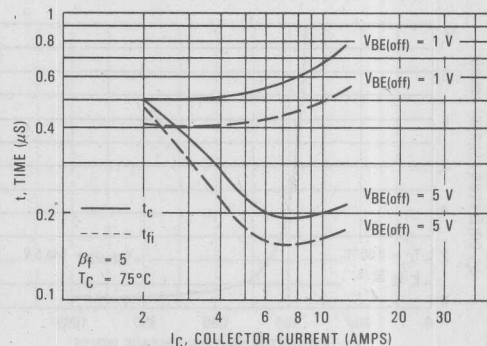
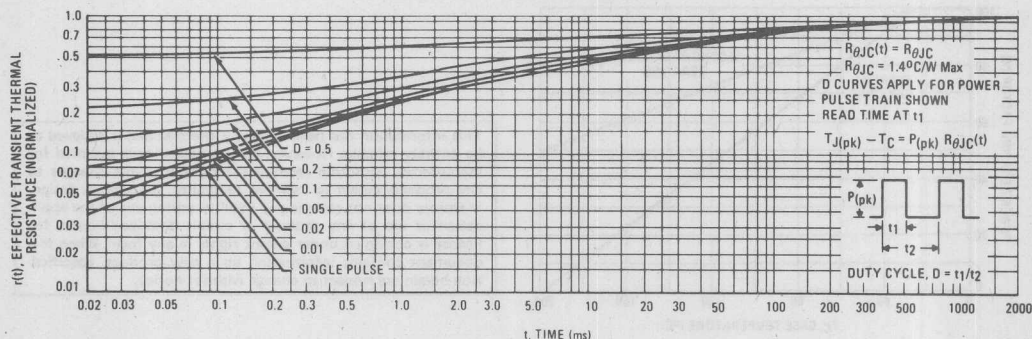


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

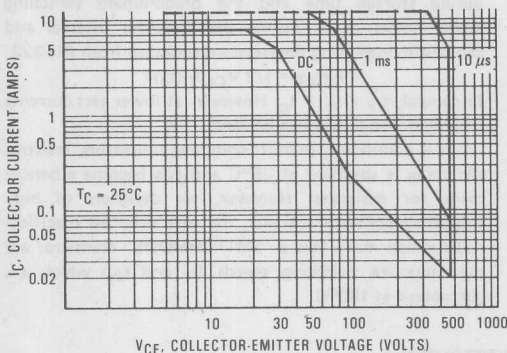


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

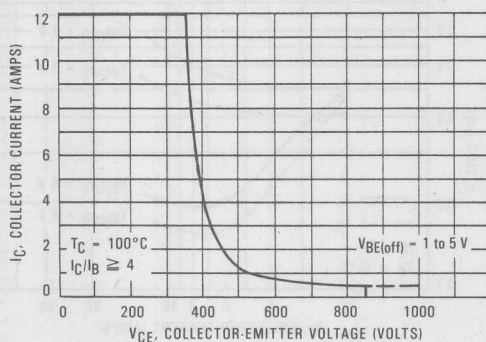
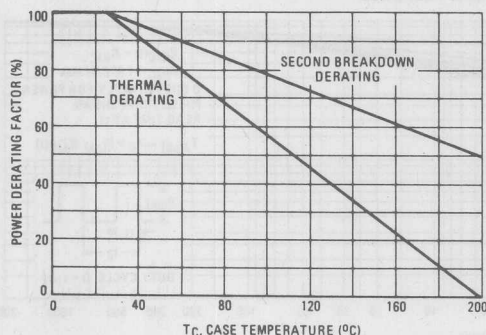


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

This information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein. No license is conveyed under patent rights in any form. When this document contains information on a new product, specification herein are subject to change without notice.



BUS 48
BUS 48A

The BUS 48 and BUS 48A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

100 ns Inductive Fall Time—25°C (Typ)
150 ns Inductive Crossover Time—25°C (Typ)
500 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range -65 to +200°C

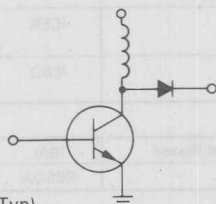
100°C Performance Specified for:

Reverse-Biased SOA with Inductive Loads

Switching Times with Inductive Loads

Saturation Voltages

Leakage Currents

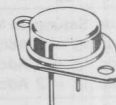


**15 AMPERES
NPN SILICON
POWER TRANSISTORS**

450 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



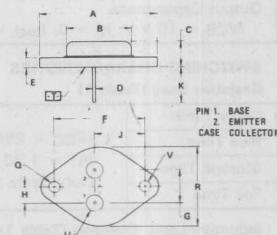
MAXIMUM RATINGS

Rating	Symbol	BUS 48	BUS 48A	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	450	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	6		Vdc
Collector Current – Continuous	I_C	15		Adc
– Peak (1)	I_{CM}	20		
Base Current – Continuous	I_B	5		Adc
– Peak (1)	I_{BM}	10		
Total Power Dissipation – $T_C = 25^\circ C$	P_D	175		Watts
– $T_C = 100^\circ C$		100		
Derate above $25^\circ C$		1.0		W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



NOTES

1. DIMENSIONS O AND V ARE DATUMS

1. DIMENSIONS Q AND V ARE DATUMS.
2. **T** IS SEATING PLANE AND DATUM

3. POSITIONAL TOLERANCE OF MOUNTING HOLE Q.

FOR LEADS:

4. DIMENSIONS AND TOLERANCES PER
ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.91	1.09	0.036	0.043
E	1.40	1.78	0.055	0.070
F	10.15 BSC		1.187 BSC	
G	30.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
W	7.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.5 2.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 6\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	$RBSOA$		See Figure 13	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	6	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 3\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ KHz}$)	C_{ob}	—	—	350	pF
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SWITCHING CHARACTERISTICS**Resistive Load (Table 1)**

Delay Time	$\sqrt{V_{CC} = 250\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{B1} = 1.25\text{ A}$, $t_p = 30\ \mu\text{s}$, Duty Cycle $\leq 2\%$, $V_{BE(off)} = 5\text{ V}$	t_d	—	0.03	0.05	μs
Rise Time		t_r	—	0.13	0.50	
Storage Time		t_s	—	0.55	2.0	
Fall Time		t_f	—	0.10	0.40	

Inductive Load, Clamped (Table 1)

Storage Time	$I_{C(pk)} = 10\text{ A}$, $I_{B1} = 1.25\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $V_{CE(pk)} = 250\text{ V}$	($T_C = 25^\circ\text{C}$)	t_{sv}	—	0.50	—	μs
Crossover Time		($T_C = 100^\circ\text{C}$)	t_c	—	0.15	—	
Storage Time			t_{sv}	—	0.80	2.5	
Crossover Time			t_c	—	0.175	0.40	
Fall Time			t_{fi}	—	0.15	0.30	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

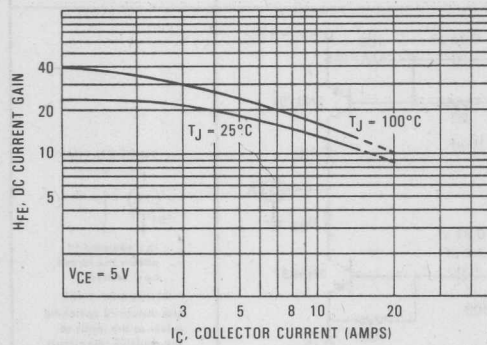


FIGURE 2 — COLLECTOR SATURATION REGION

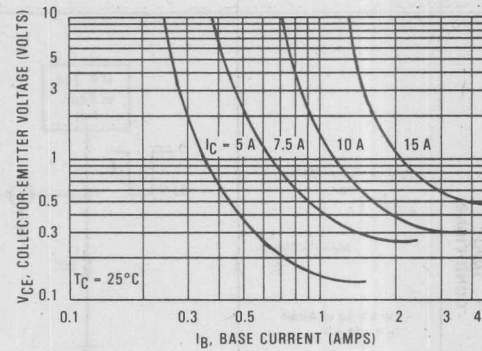


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

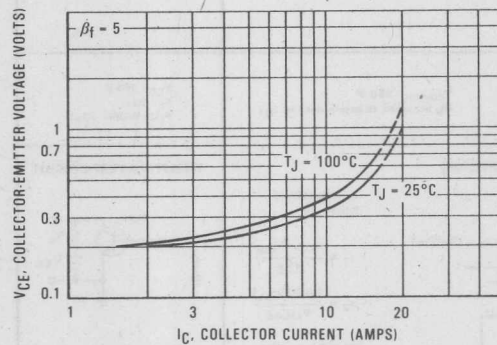


FIGURE 4 — BASE-EMITTER VOLTAGE

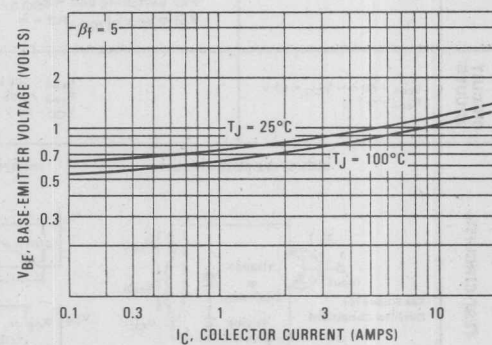


FIGURE 5 — COLLECTOR CUTOFF REGION

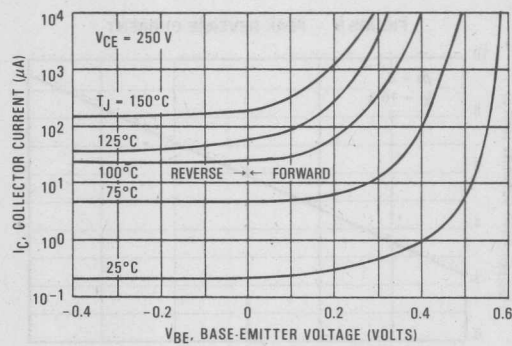


FIGURE 6 — CAPACITANCE

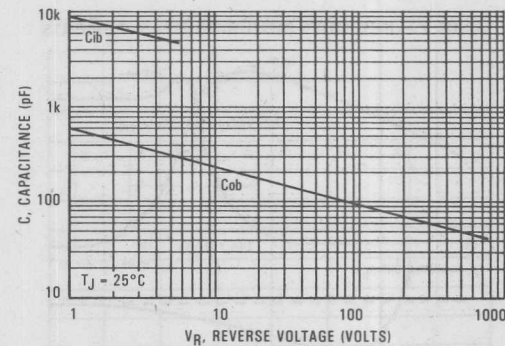


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

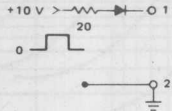
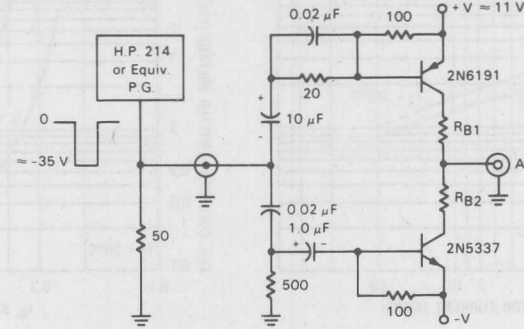
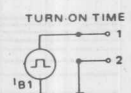
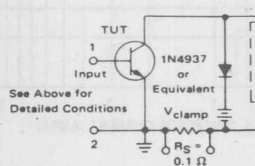
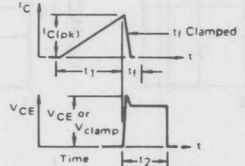
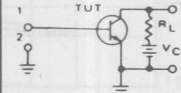
	$V_{CE(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>	 <p>Adjust R_1 to obtain I_{B1} For switching and R_{BSOA}, $R_2 = 0$ For $BV_{CE(sus)}$, $R_2 = \infty$</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 80 \text{ mH}$ $R_{coil} = 0.7 \Omega$ $V_{CC} = 10 \text{ V}$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 250 \text{ V}$ R_B adjusted to attain desired I_{B1}	$V_{CC} = 250 \text{ V}$ $R_L = 83 \Omega$ Pulse Width = $10 \mu\text{s}$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

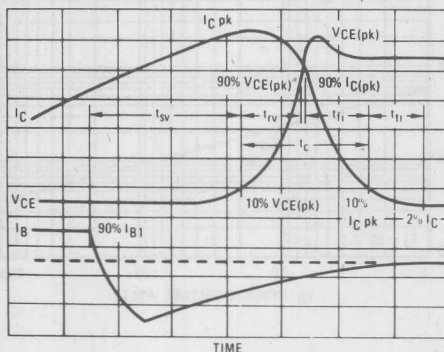
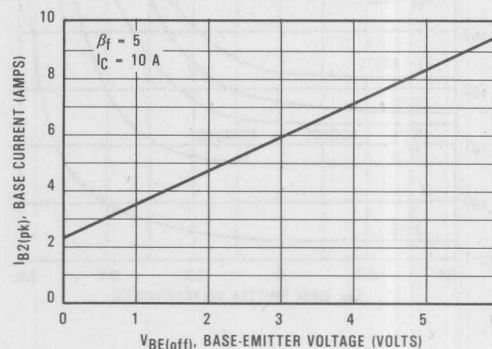


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As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

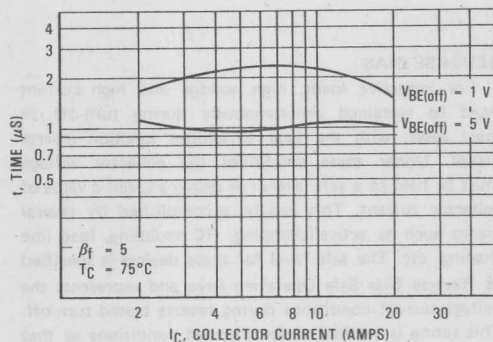
FIGURE 9 — STORAGE TIME, T_{sv} 

FIGURE 10 — CROSSOVER AND FALL TIMES

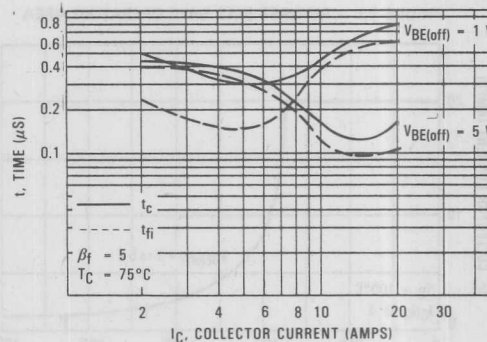
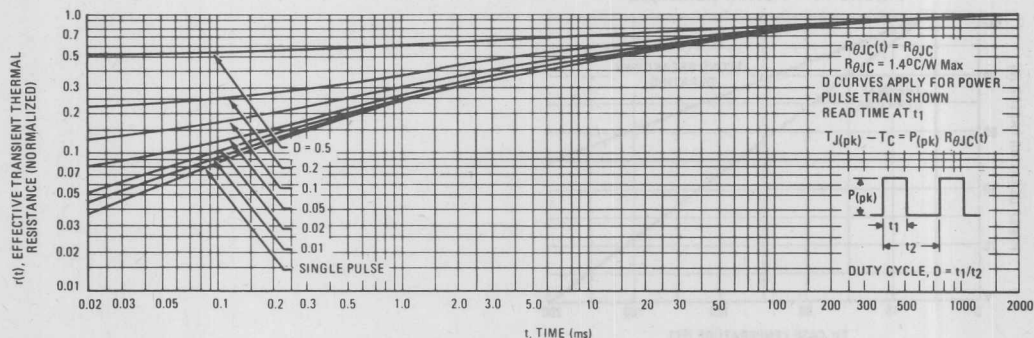


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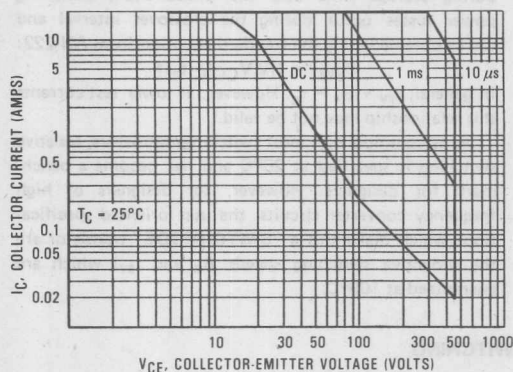


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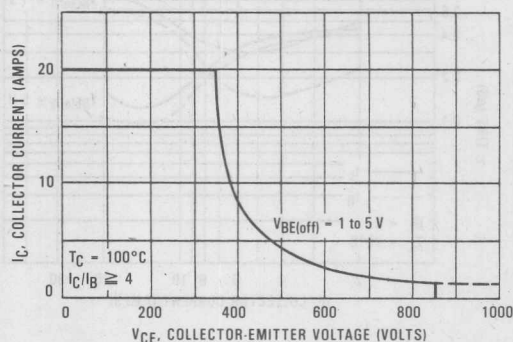
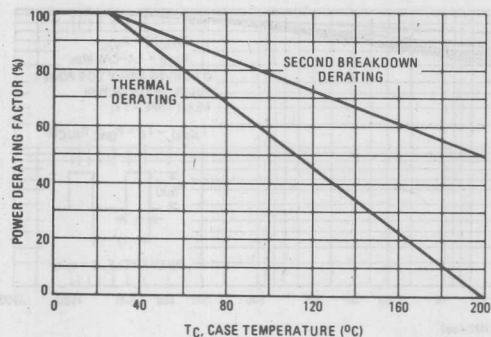


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SAFE OPERATING AREA INFORMATION

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REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.



MOTOROLA

BUS 48P BUS 48AP

SWITCHMODE II⁺ SERIES NPN SILICON POWER TRANSISTORS

The BUS 48P/BUS 48AP transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

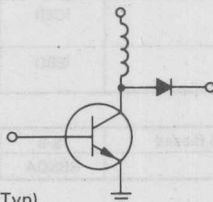
Fast Turn-Off Times

100 ns Inductive Fall Time—25°C (Typ)
150 ns Inductive Crossover Time—25°C (Typ)
500 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range – 65 to +150°C

100°C Performance Specified for:

Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

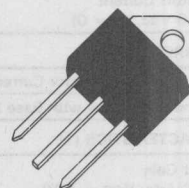


15 AMPERES

NPN SILICON
POWER TRANSISTORS

450 VOLTS

125 WATTS



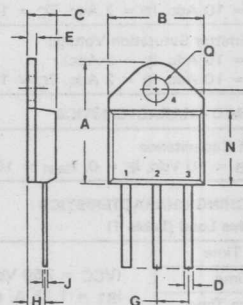
MAXIMUM RATINGS

Rating	Symbol	BUS 48P	BUS 48AP	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	450	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	6		Vdc
Collector Current – Continuous	I_C	15		Adc
– Peak (1)	I_{CM}	20		
Base Current – Continuous	I_B	5		Adc
– Peak (1)	I_{BM}	10		
Total Power Dissipation – $T_C = 25^\circ\text{C}$	P_D	125		Watts
– $T_C = 100^\circ\text{C}$		100		
Derate above 25°C		1.0		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

CASE 340-01
TO-218AC

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCEO(sus)	450	—	—	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 100°C)	ICEV	—	—	0.5 2.5	mAdc
Collector Cutoff Current (VCE = Rated VCEV, RBE = 50 Ω, TC = 100°C)	ICER	—	—	3.0	mAdc
Emitter Cutoff Current (VEB = 6 Vdc, IC = 0)	IEBO	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	IS/b	—	See Figure 12	—
Clamped Inductive SOA with Base Reverse Biased	RBSOA	—	See Figure 13	—

ON CHARACTERISTICS (1)

DC Current Gain (IC = 10 Adc, VCE = 5 V)	hFE	6	—	—	—
Collector-Emitter Saturation Voltage (IC = 10 Adc, IB = 2 Adc) (IC = 15 Adc, IB = 3 Adc) (IC = 10 Adc, IB = 2 Adc, TC = 100°C)	VCE(sat)	—	—	1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (IC = 10 Adc, IB = 2 Adc) (IC = 10 Adc, IB = 2 Adc, TC = 100°C)	VBE(sat)	—	—	1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (VCB = 10 Vdc, IE = 0, ftest = 100 KHz)	Cob	—	—	350	pF
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SWITCHING CHARACTERISTICS
Resistive Load (Table 1)

Delay Time	(VCC = 250 Vdc, IC = 10 A, IB1 = 1.25 A, tp = 30 μs, Duty Cycle ≤ 2%, VBE(off) = 5 V)	td	—	0.03	0.05	μs
Rise Time		tr	—	0.13	0.50	
Storage Time		ts	—	0.55	2.0	
Fall Time		tf	—	0.10	0.40	

Inductive Load, Clamped (Table 1)

Storage Time	(IC(pk) = 10 A, IB1 = 1.25 A, VBE(off) = 5 V, VCE(pk) = 250 V)	(TC = 25°C)	tsv	—	0.50	—	μs
Crossover Time		(TC = 25°C)	tc	—	0.15	—	
Storage Time		(TC = 100°C)	tsv	—	0.80	2.5	
Crossover Time		(TC = 100°C)	tc	—	0.175	0.40	
Fall Time			tfj	—	0.15	0.30	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

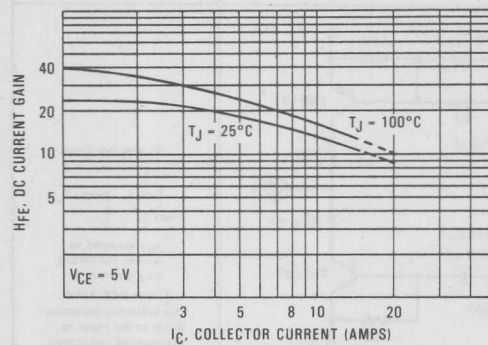


FIGURE 2 — COLLECTOR SATURATION REGION

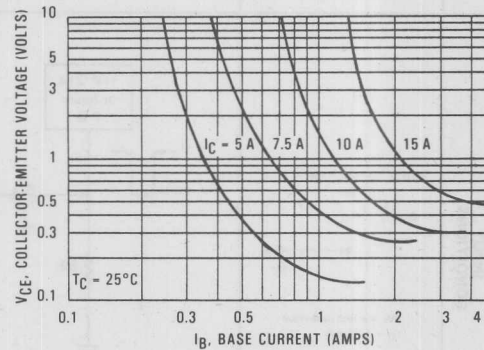


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

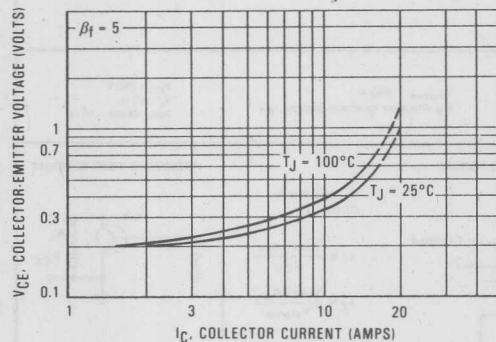


FIGURE 4 — BASE-EMITTER VOLTAGE

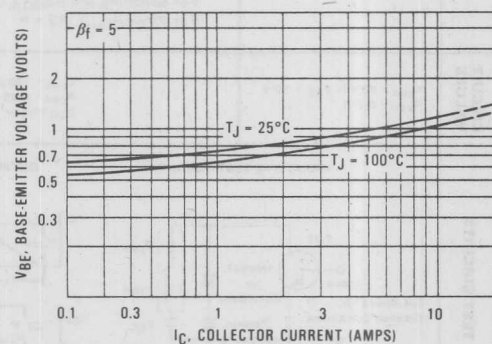


FIGURE 5 — COLLECTOR CUTOFF REGION

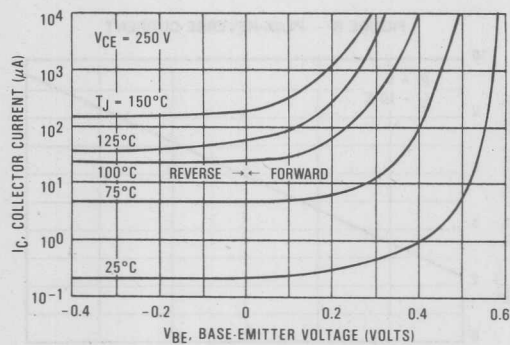


FIGURE 6 — CAPACITANCE

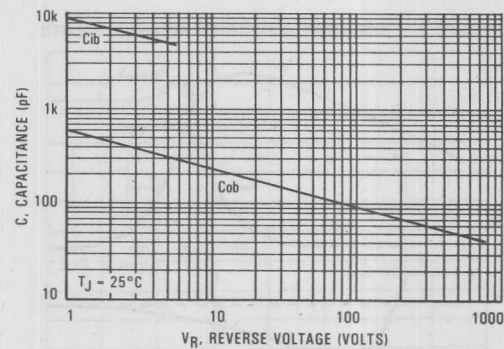


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

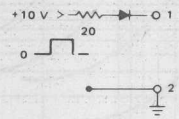
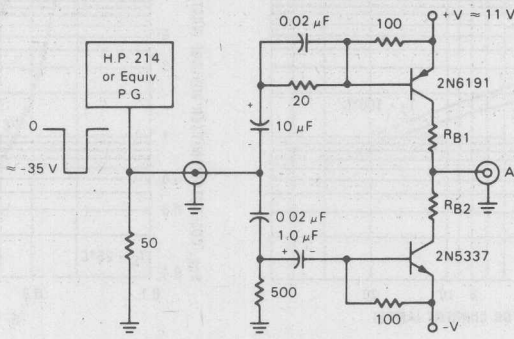
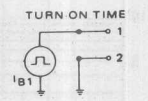
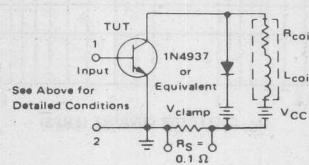
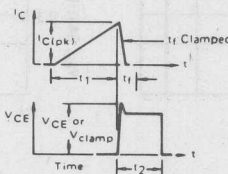
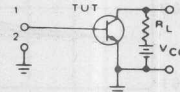
	$V_{CE(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>	 <p>Adjust R_1 to obtain I_{B1} For switching and R_{BSOA}, $R_2 = 0$ For $BV_{CE(sus)}$, $R_2 = \infty$</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 250 \text{ V}$ R_B adjusted to attain desired I_{B1}	$V_{CC} = 250 \text{ V}$ $R_L = 83 \Omega$ Pulse Width = $10 \mu\text{s}$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

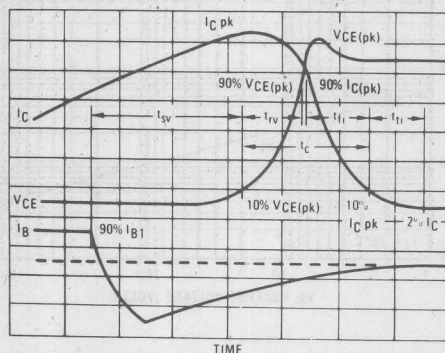
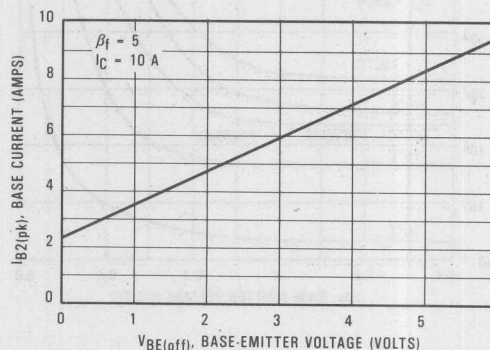


FIGURE 8 - PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME, T_{sv}

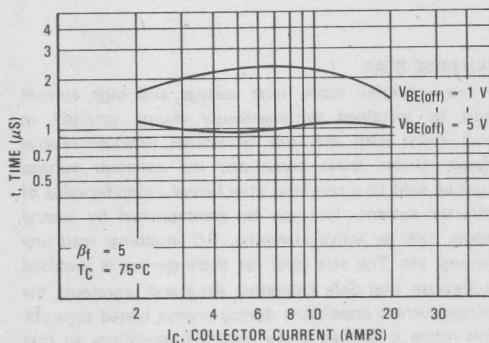


FIGURE 10 — CROSSOVER AND FALL TIMES

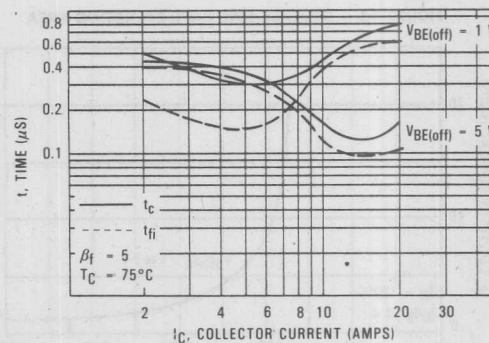
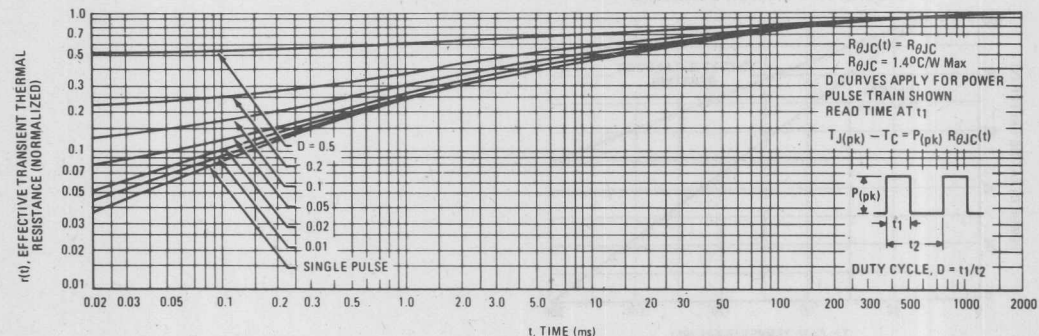


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

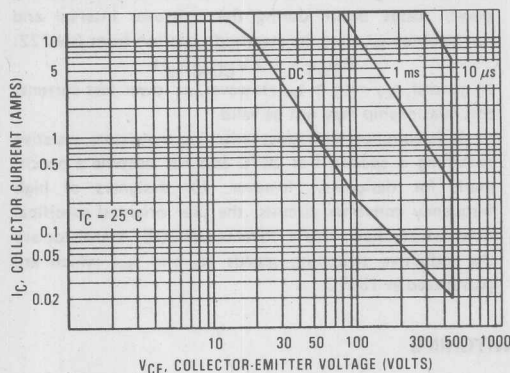


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

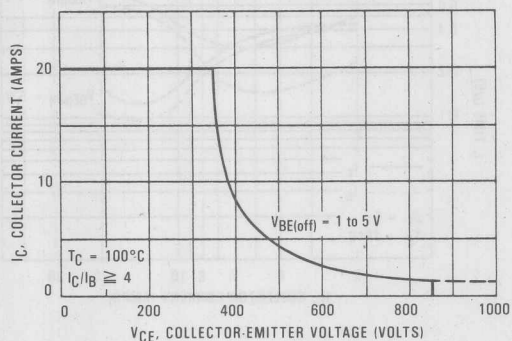
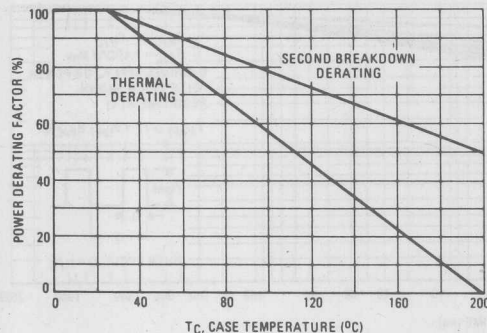


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

**MOTOROLA**

BUS 98 BUS 98A

SWITCHMODE II SERIES NPN SILICON POWER TRANSISTORS

The BUS 98 and BUS 98A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

60 ns Inductive Fall Time – 25°C (Typ)

120 ns Inductive Crossover Time – 25°C (Typ)

Operating Temperature Range – 65 to +200°C

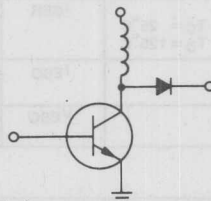
100°C Performance Specified for:

Reverse-Biased SOA with Inductive Loads

Switching Times with Inductive Loads

Saturation Voltages

Leakage Currents (125°C)

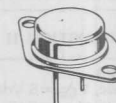


30 AMPERES NPN SILICON POWER TRANSISTORS

450 VOLTS
250 WATTS
850-1000 VOLTS (V_{ces})

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



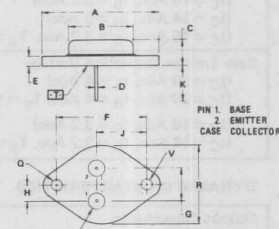
MAXIMUM RATINGS

Rating	Symbol	BUS 98	BUS98A	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	400	450	Vdc
Collector-Emitter Voltage	V _{CEV}	850	1000	Vdc
Emitter Base Voltage	V _{EB}	6		Vdc
Collector Current – Continuous	I _C	30		Adc
– Peak (1)	I _{CM}	60		
– Overload	I _{ol}	120		
Base Current – Continuous	I _B	10		Adc
– Peak (1)	I _{BM}	30		
Total Power Dissipation – T _C = 25°C	P _D	250		Watts
– T _C = 100°C		142		
Derate above 25°C		1.42		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	– 65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
1. DIMENSIONS D AND V ARE DATUMS
2. IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MIN	MAX	MIN	MAX
A	29.27	29.27	1.150	1.150
B	21.88	21.88	0.830	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.00	0.038	0.040
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.48 BSC		0.215 BSC	
J	16.80 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	26.67		1.050	
N	4.83	5.33	0.190	0.210
U	3.81	4.19	0.150	0.165

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200\text{ mA}$, $I_B = 0$) $L = 25\text{ mH}$	BUS98 BUS98A	$V_{CEO(sus)}$ 400 450	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 125^\circ\text{C}$)		I_{CEV} — —	— —	0.4 4.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 10\ \Omega$) $T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$		I_{CER} — —	— —	1.0 6.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5\text{ Vdc}$, $I_C = 0$)		I_{EBO}		0.2	mAdc
Emitter-base breakdown Voltage ($I_E = 100\text{ mA}$, $I_C = 0$)		V_{EBO}	6.0		Vdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 20\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 16\text{ Adc}$, $V_{CE} = 5\text{ V}$)	BUS98 BUS98A	h_{FE} 8	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 4\text{ Adc}$) ($I_C = 30\text{ Adc}$, $I_B = 8\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 4\text{ Adc}$, $T_C = 100^\circ\text{C}$) ($I_C = 16\text{ Adc}$, $I_B = 3.2\text{ Adc}$) ($I_C = 24\text{ Adc}$, $I_B = 5\text{ Adc}$) ($I_C = 16\text{ Adc}$, $I_B = 3.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	BUS98 BUS98A	$V_{CE(sat)}$ — — — — — —	— — — — — —	1.5 3.5 2.0 1.5 5.0 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 4\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 4\text{ Adc}$, $T_C = 100^\circ\text{C}$) ($I_C = 16\text{ Adc}$, $I_B = 3.2\text{ Adc}$) ($I_C = 16\text{ Adc}$, $I_B = 3.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	BUS98 BUS98A	$V_{BE(sat)}$ — — — —	— — — —	1.6 1.6 1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ kHz}$)	C_{ob}	—	—	700	pF
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SWITCHING CHARACTERISTICS
Resistive Load (Table 1)

Delay Time	(V _{CC} = 250 Vdc, I _C = 20A, I _{B1} = 4.0 A, t _p = 30 μ s, Duty Cycle $\leq 2\%$, V _{BE(off)} = 5 V) (for BUS98A : I _C = 16A, I _{B1} = 3.2A)	t_d	—	0.1	0.2	μ s
Rise Time		t_r	—	0.4	0.7	
Storage Time		t_s	—	1.55	2.3	
Fall Time		t_f	—	0.2	0.4	

Inductive Load, Clamped (Table 1)

Storage Time	I _{C(pk)} = 20A I _{B1} = 4A (BUS98)	(T _C = 25°C)	t_{sv}	—	1.55	—	μ s
Fall Time			t_{fi}	—	0.06	—	
Storage Time	V _{BE(off)} = 5 V, V _{CE(c1)} = 250 V) I _{C(pk)} = 16A I _{B1} = 3.2A (BUS98A)	(T _C = 100°C)	t_{sv}	—	1.8	2.8	
Crossover Time			t_c	—	0.3	0.6	
Fall Time			t_{fi}	—	0.17	0.35	

(1) Pulse Test : PW = 300 μ s, Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

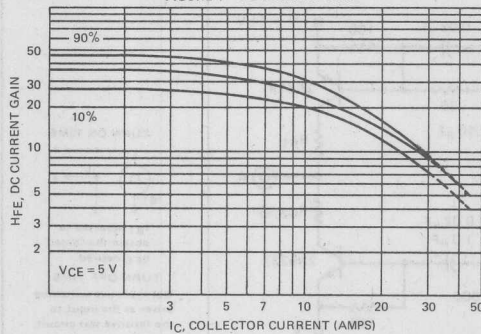


FIGURE 2 — COLLECTOR SATURATION REGION

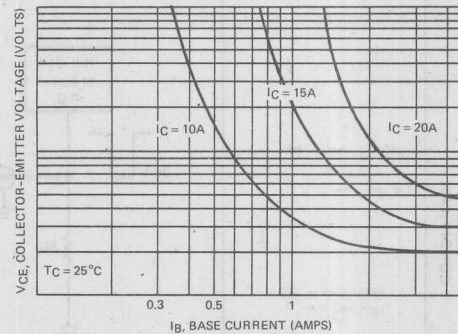


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

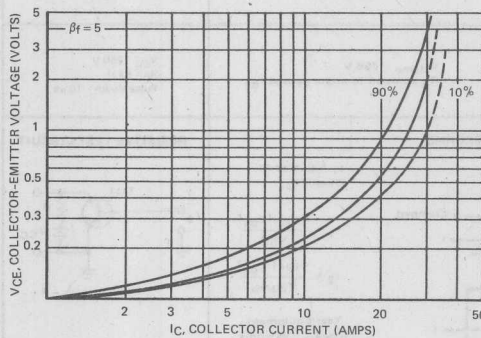


FIGURE 4 — BASE-EMITTER VOLTAGE

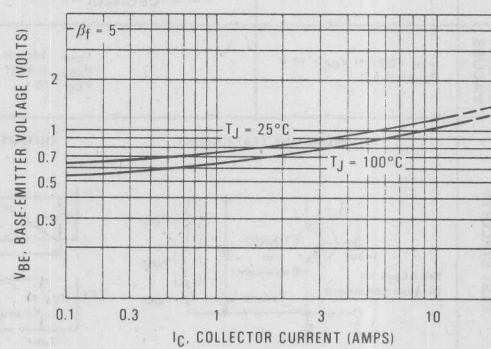


FIGURE 5 — COLLECTOR CUTOFF REGION

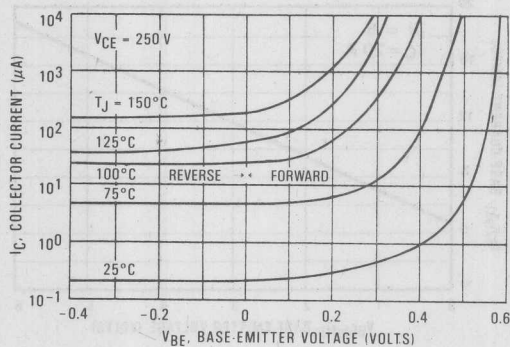


FIGURE 6 — CAPACITANCE

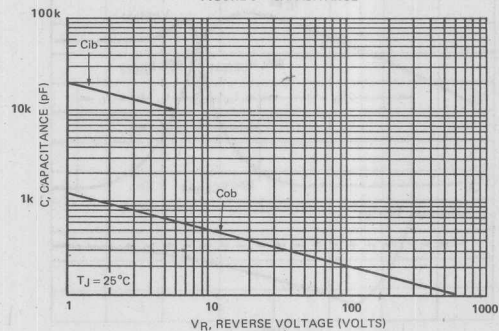


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

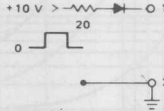
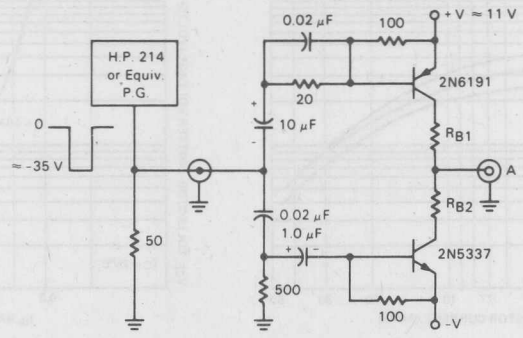
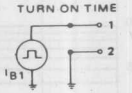
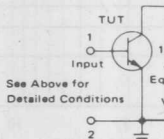
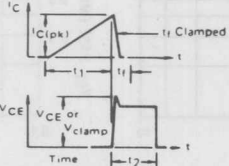
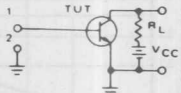
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>	 <p>Adjust R_1 to obtain I_{B1} For switching and R_{BSOA}, $R_2 = 0$ For $BV_{CEO(sus)}$, $R_2 = \infty$</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 25 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 250 \text{ V}$ R_B adjusted to attain desired I_{B1}	$V_{CC} = 250 \text{ V}$ $R_L = 83 \Omega$ Pulse Width: $10 \mu\text{s}$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

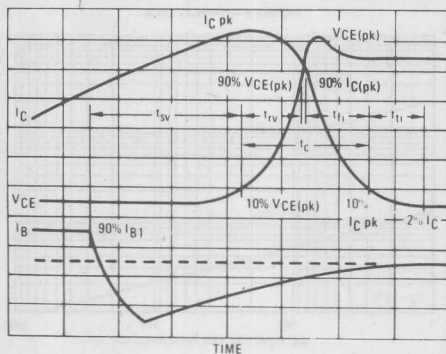
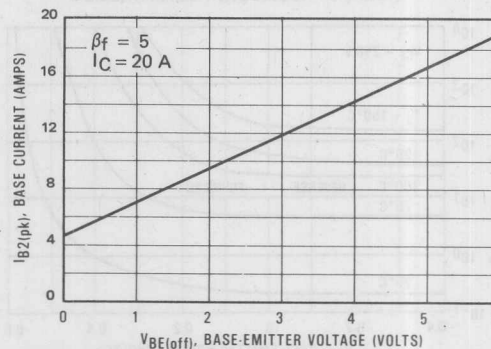


FIGURE 8 — PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
 - t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
 - t_{fi} = Current Fall Time, 90–10% I_C
 - t_{ti} = Current Tail, 10–2% I_C
 - t_c = Crossover Time, 10% V_{clamp} to 10% I_C
- An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

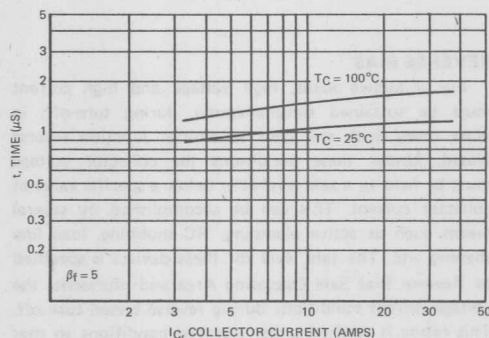
FIGURE 9 — STORAGE TIME, T_{sv} 

FIGURE 10 — CROSSOVER AND FALL TIMES

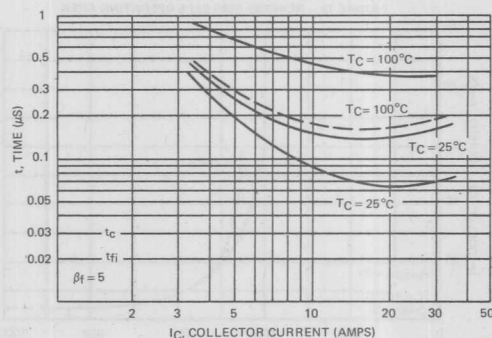
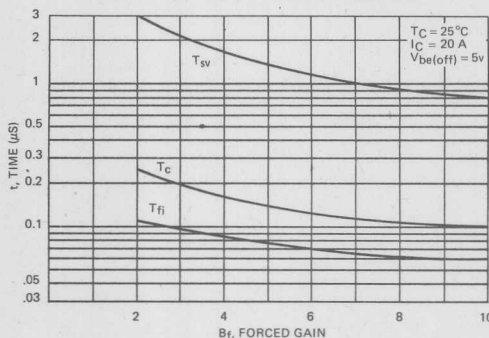
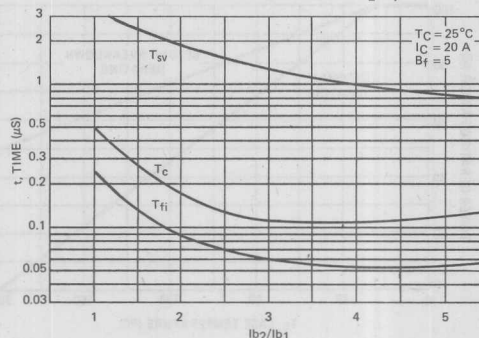


FIGURE 11a — TURN-OFF TIMES vs FORCED GAIN

FIGURE 11b — TURN-OFF TIMES vs I_{b2}/I_{b1} 

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

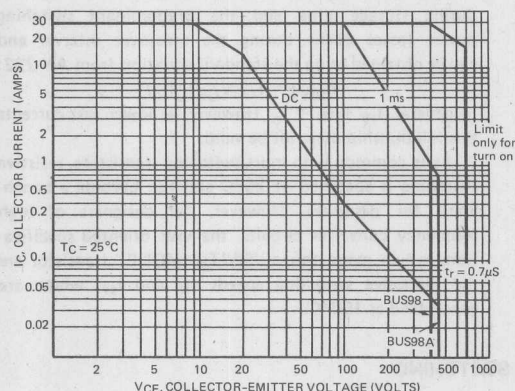


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

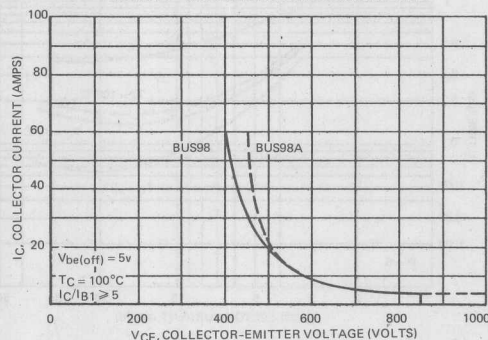
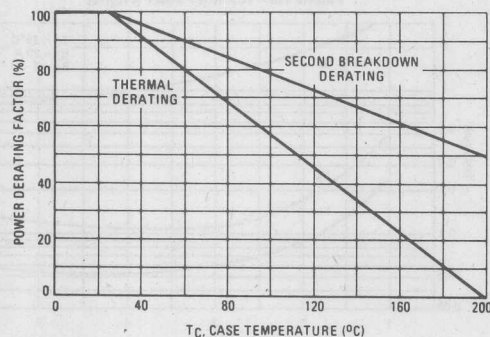


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 15 — THERMAL RESPONSE

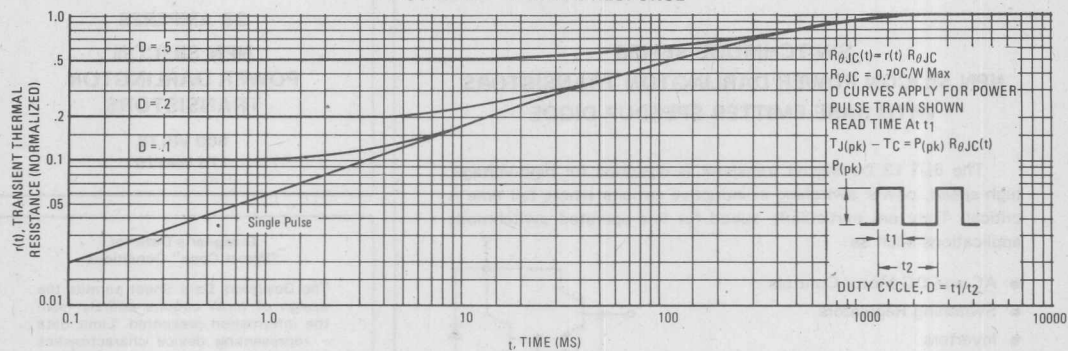
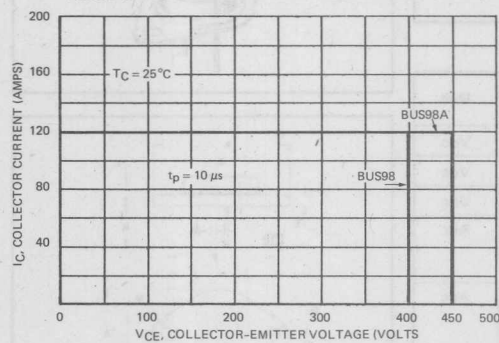
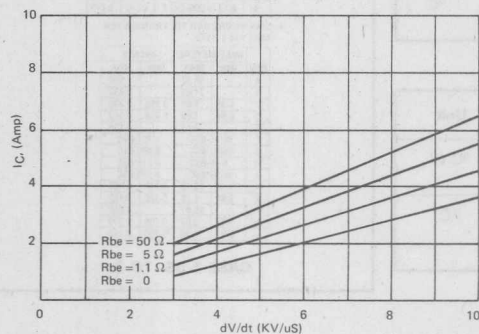


FIGURE 16 — RATED OVERLOAD SAFE OPERATING AREA (OLSOA)


FIGURE 17 — $I_C = f(dV/dt)$


OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

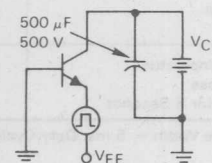
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths (Pulse width is defined as the time lag between the fault condition and the removal of base drive). Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C , t_p

FIGURE 18 — OVERLOAD SOA TEST CIRCUIT



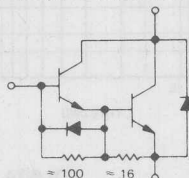
SWITCHMODE SERIES NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The BUT13 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times

300 nS Inductive Fall Time at 25°C (Typ)
1.1 μ S Inductive Storage Time at 25°C (Typ)

- Operating Temperature Range - 65 to 200°C

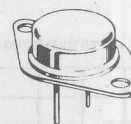


28 AMPERES NPN SILICON POWER DARLINGTON TRANSISTORS

600 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



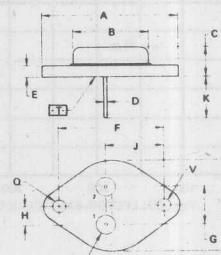
MAXIMUM RATINGS

Rating	Symbol		Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current			Adc
- Continuous	I_C	28	
- Peak (1)	I_{CM}	35	
Base Current			Adc
- Continuous	I_B	6	
- Peak (1)	I_{BM}	7.5	
Free Wheel Diode:			Adc
Forward current - Continuous	I_F	28	
- Peak	I_{FM}	35	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175	Watts
@ $T_C = 100^\circ\text{C}$		100	
Derate above 25°C			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



NOTES
1 DIMENSIONS D AND V ARE DATUMS
2 [] IS SEATING PLANE AND DATUM
3 POSITIONAL TOLERANCE FOR MOUNTING HOLE D

FOR LEADS

4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MIN	MAX	MIN	MAX
A	39.37	1.550		
B	21.08	0.830		
C	6.35	0.250		
D	0.92	0.036		
E	3.43	0.135		
F	30.15 BSC	1.187 BSC		
G	10.97 BSC	0.430 BSC		
H	5.48 BSC	0.215 BSC		
J	16.89 BSC	0.665 BSC		
K	11.18	0.440		
L	3.81	0.150		
M	26.67	1.050		
N	4.83	0.190		
O	3.81	0.150		

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	400	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.1 2.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	$RBSOA$		See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10\text{ A}$, $V_{CE} = 5\text{ V}$) ($I_C = 18\text{ A}$, $V_{CE} = 5\text{ V}$)	h_{FE}	30 20	— —	— —	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 0.5\text{ A}$) ($I_C = 18\text{ A}$, $I_B = 1.8\text{ A}$) ($I_C = 22\text{ A}$, $I_B = 2.2\text{ A}$) ($I_C = 28\text{ A}$, $I_B = 5.6\text{ A}$)	$V_{CE(sat)}$	— — — —	— — — —	2.0 2.5 3.0 5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 0.5\text{ A}$) ($I_C = 18\text{ A}$, $I_B = 1.8\text{ A}$) ($I_C = 22\text{ A}$, $I_B = 2.2\text{ A}$)	$V_{BE(sat)}$	— — —	— — —	2.5 3.0 3.3	Vdc
Diode Forward Voltage ($I_F = 22\text{ A}$)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	$T_C = 25^\circ\text{C}$	See Table 1 $I_C = 18\text{ A}$	t_s	—	1.1	2.6	μs
Fall Time			t_f	—	0.3	0.8	μs
Storage Time	$T_C = 100^\circ\text{C}$	$I_{B1} = 1.8\text{ A}$ $V_{BE(off)} = 5\text{ V}$	t_s	—	1.4	—	μs
Fall Time			t_f	—	0.33	—	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

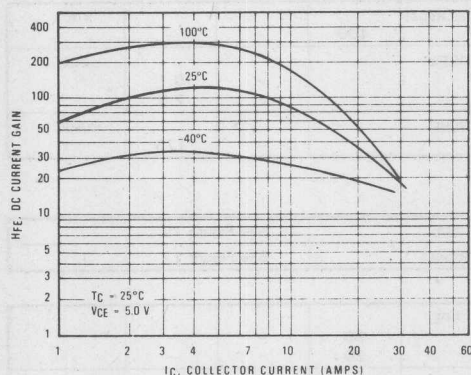


FIGURE 2 — COLLECTOR SATURATION REGION

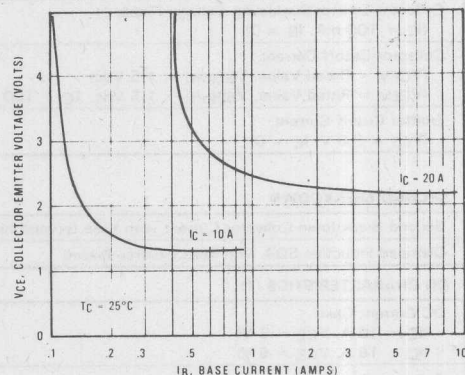


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

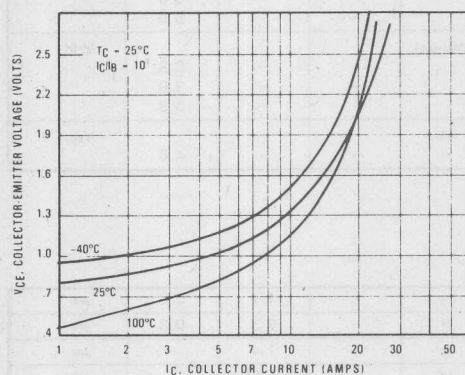


FIGURE 4 — BASE-EMITTER VOLTAGE

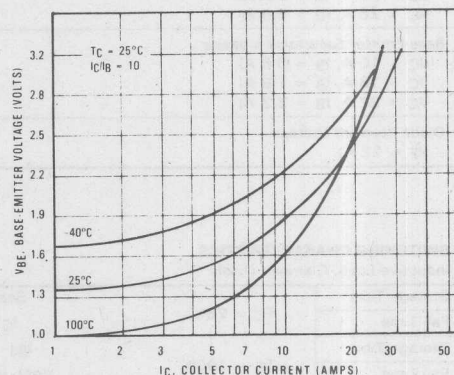
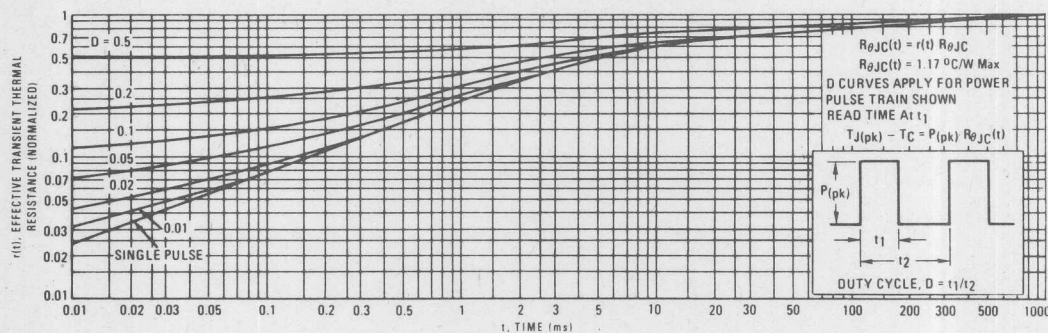


FIGURE 5 — THERMAL RESPONSE



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

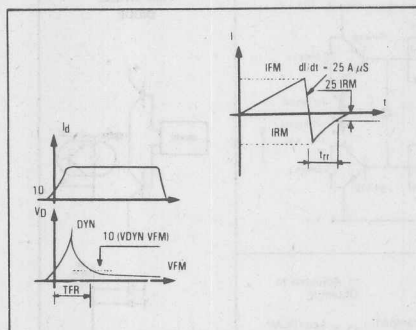


FIGURE 11 — FORWARD VOLTAGE

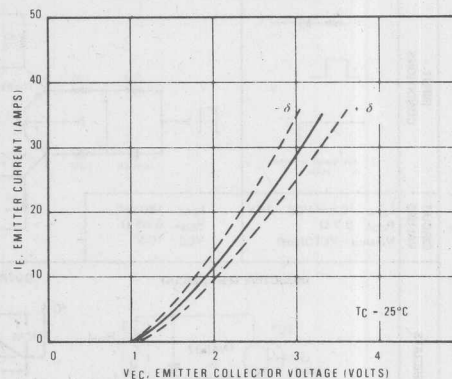


FIGURE 12 — FORWARD MODULATION VOLTAGE

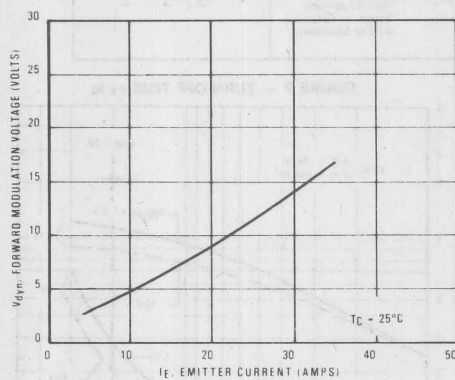


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

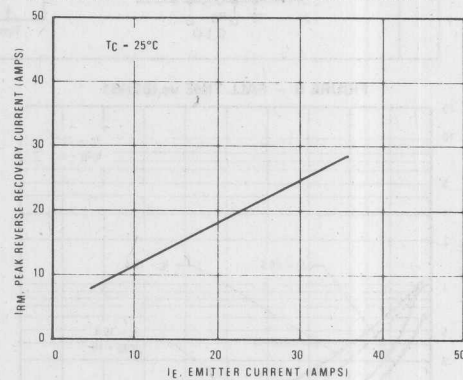


FIGURE 14 — FORWARD RECOVERY TIME

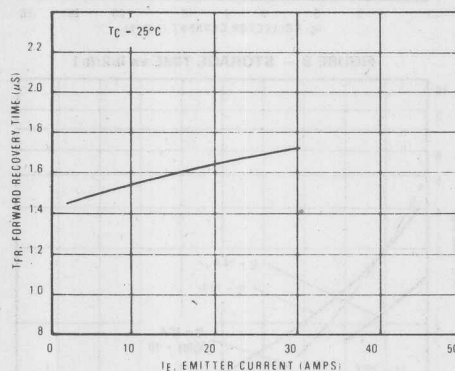
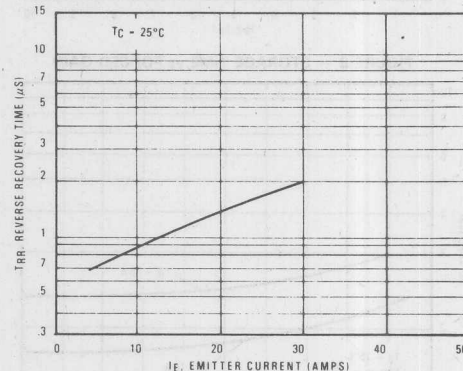


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

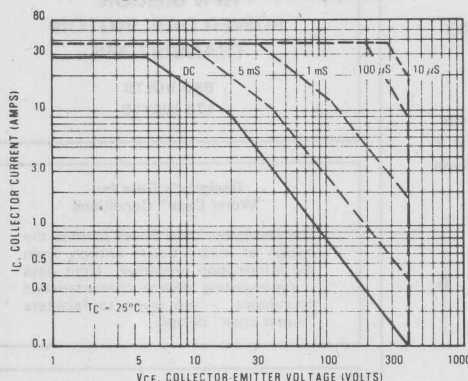


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA

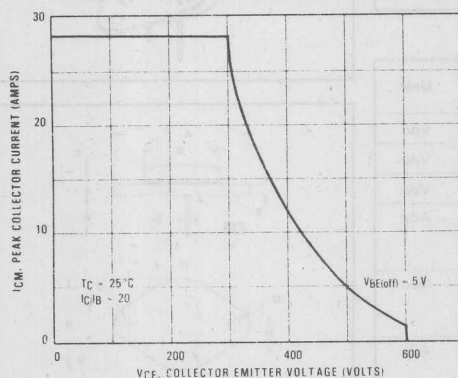
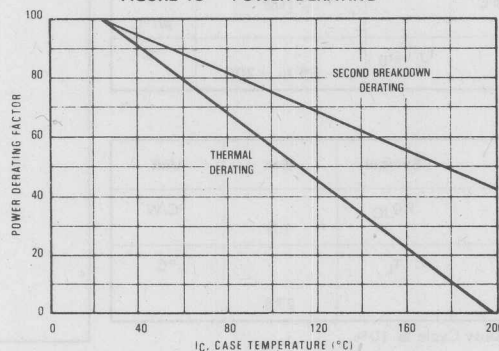


FIGURE 18 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_J(\text{pk})$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.



**SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE**

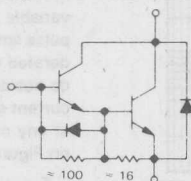
The BUT14 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times

300 nS Inductive Fall Time at 25°C (Typ)

1.3 μS Inductive Storage Time at 25°C (Typ)

- Operating Temperature Range - 65 to 200°C



MAXIMUM RATINGS

Rating	Symbol		Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	500	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current			Adc
- Continuous	I_C	25	
- Peak (1)	I_{CM}	35	
Base Current			Adc
- Continuous	I_B	5	
- Peak (1)	I_{BM}	7.5	
Free Wheel Diode:			Adc
Forward current	I_F	25	
- Peak	I_{FM}	35	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175	Watts
@ $T_C = 100^\circ\text{C}$		100	
Derate above 25°C			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 65 to + 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

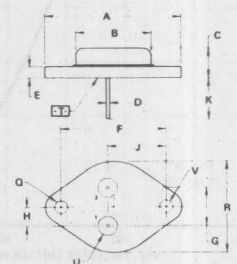
(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≤ 10%.

**25 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS**

**850 VOLTS
175 WATTS**

**Designer's Data for
"Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



NOTES
1 DIMENSIONS D AND V ARE DATUMS
2 \square IS SEATING PLANE AND DATUM
3 POSITIONAL TOLERANCE FOR MOUNTING HOLE G

$\phi .13 (0.0051) \text{ T V } \phi$

FOR LEADS

$\phi .13 (0.0051) \text{ T V } \phi 0 \phi$

4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	35.27	1.550		
B	21.08	0.830		
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	3.43	0.135		
F	30.15 BSC	1.187 BSC		
G	10.92 BSC	0.430 BSC		
H	5.46 BSC	0.215 BSC		
J	16.89 BSC	0.665 BSC		
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	26.67	1.050		
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	500	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.2 2.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17	

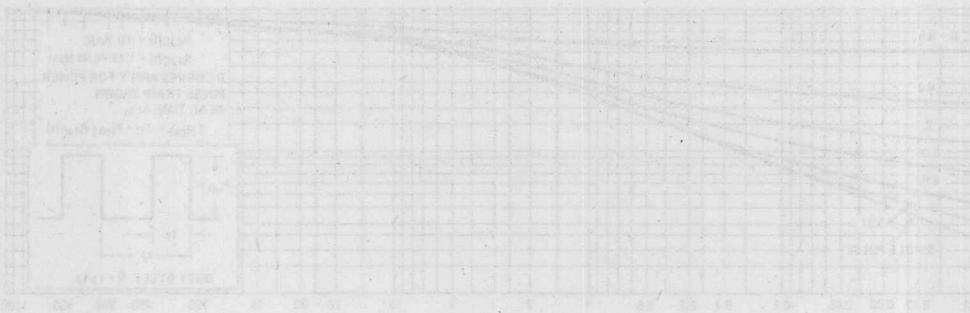
ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 8\text{ A}$, $V_{CE} = 5\text{ V}$) ($I_C = 16\text{ A}$, $V_{CE} = 5\text{ V}$)	h_{FE}	30 15	—	—	
Collector-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 0.4\text{ A}$) ($I_C = 16\text{ A}$, $I_B = 1.6\text{ A}$) ($I_C = 20\text{ A}$, $I_B = 2.0\text{ A}$) ($I_C = 25\text{ A}$, $I_B = 5\text{ A}$)	$V_{CE(sat)}$	—	—	2.0 3.0 3.5 5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 0.4\text{ A}$) ($I_C = 16\text{ A}$, $I_B = 1.6\text{ A}$) ($I_C = 20\text{ A}$, $I_B = 2\text{ A}$)	$V_{BE(sat)}$	—	—	2.5 2.9 3.3	Vdc
Diode Forward Voltage ($I_F = 20\text{ A}$)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	$T_C = 25^\circ\text{C}$	See Table 1 $I_C = 16\text{ A}$	t_s	—	1.3	2.8	μs
Fall Time			t_f	—	0.3	0.8	μs
Storage Time	$T_C = 100^\circ\text{C}$	$I_{B1} = 1.6\text{ A}$ $V_{BE(off)} = 5\text{ V}$	t_s	—	1.5	—	μs
Fall Time			t_f	—	0.35	—	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

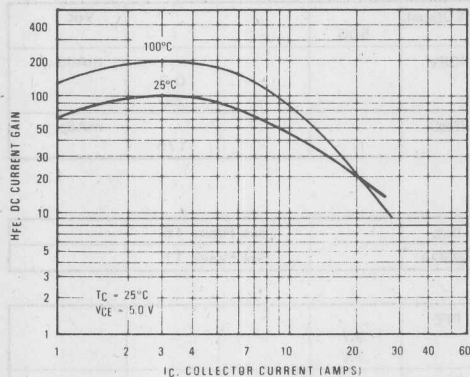


FIGURE 2 — COLLECTOR SATURATION REGION

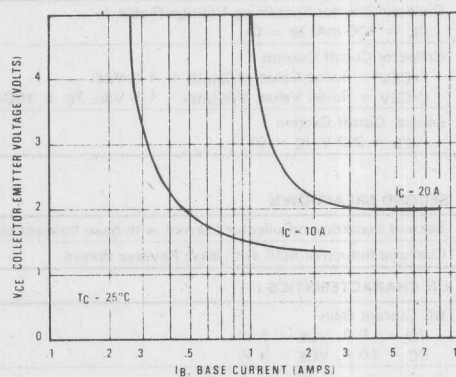


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

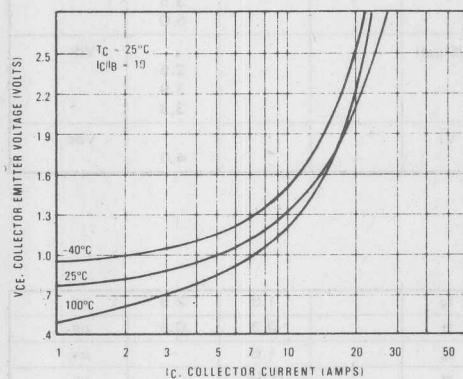


FIGURE 4 — BASE-EMITTER VOLTAGE

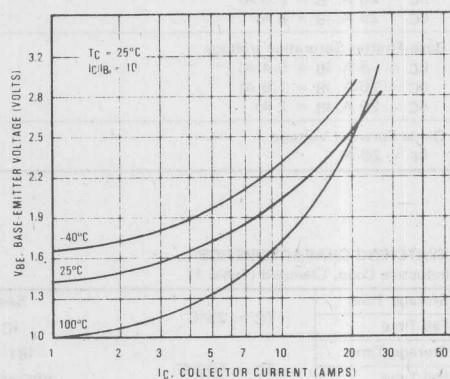


FIGURE 5 — THERMAL RESPONSE

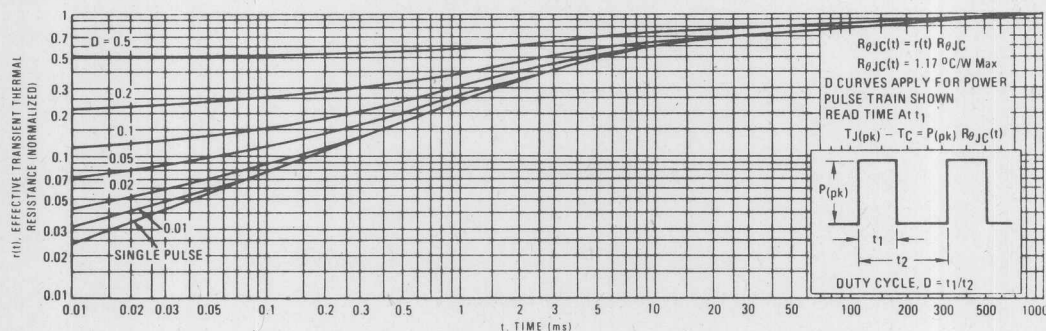


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

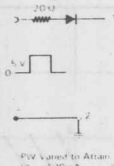
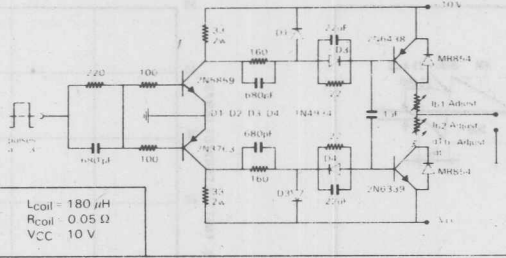
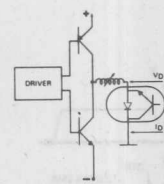
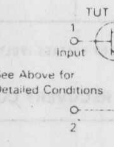
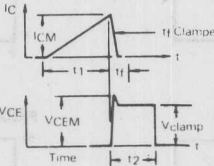
INPUT CONDITIONS	VCE(sus)	RBSOA AND INDUCTIVE SWITCHING	TEST CIRCUIT for FREE WHEEL DIODE
 <p>PW Varied to Attain IC 1.00mA</p>	<p>Lcoil = 10 mH VCC = 10V Rcoil = 0.7 Ω Vclamp = VCE(sus)</p>	 <p>Lcoil = 180 μH Rcoil = 0.05 Ω VCC = 10 V</p>	 <p>DRIVER</p> <p>AV 50 V 50 V</p> <p>CHROMETICS PG138 50 W 50 V</p>
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT	OUTPUT WAVEFORMS	
	 <p>See Above for Detailed Conditions</p> <p>0.1 Ω</p>	 <p>IC</p> <p>ICM</p> <p>t1</p> <p>t2</p> <p>VCE</p> <p>VCEM</p> <p>Vclamp</p> <p>Time</p> <p>t1 Adjusted to Obtain IC</p> <p>t1 = Lcoil(ICM)/VCC</p> <p>t2 = Lcoil(ICM)/Vclamp</p> <p>Test Equipment Scope Tektronix 475 or Equivalent</p>	

FIGURE 6 — FALL TIME vs IB2/IB1

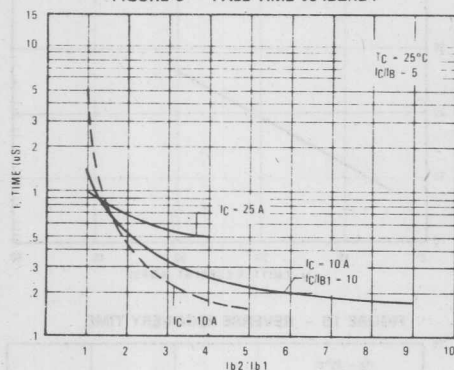


FIGURE 7 — TURN-OFF TIME vs IC

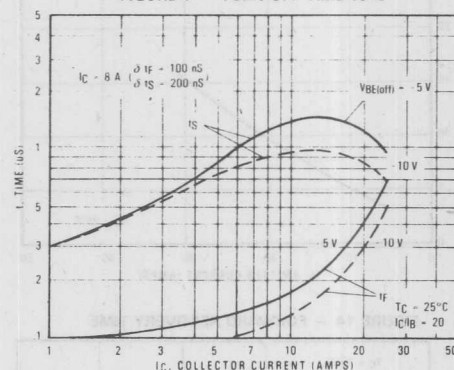


FIGURE 8 — STORAGE TIME vs FORCED GAIN

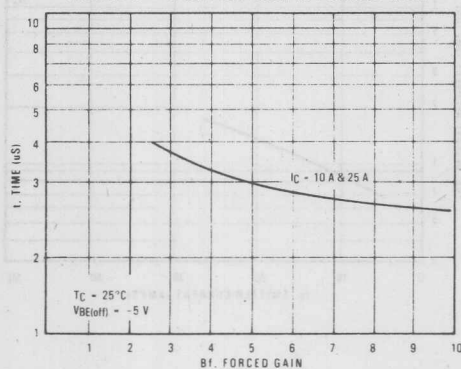
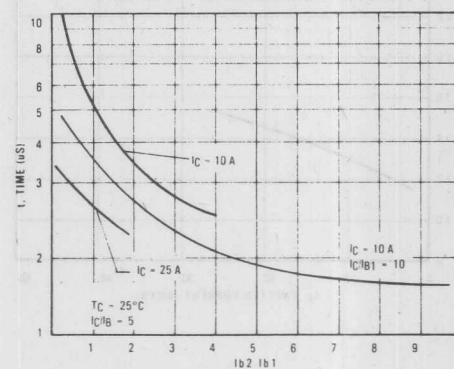


FIGURE 9 — STORAGE TIME vs IB2/IB1



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

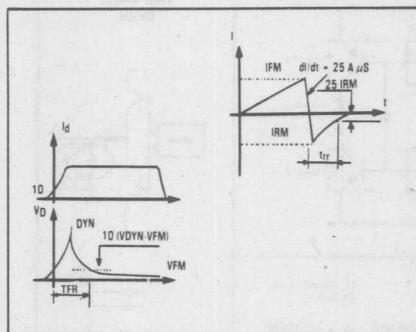


FIGURE 11 — FORWARD VOLTAGE

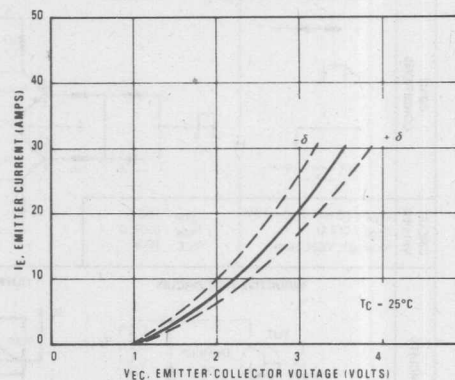


FIGURE 12 — FORWARD MODULATION VOLTAGE

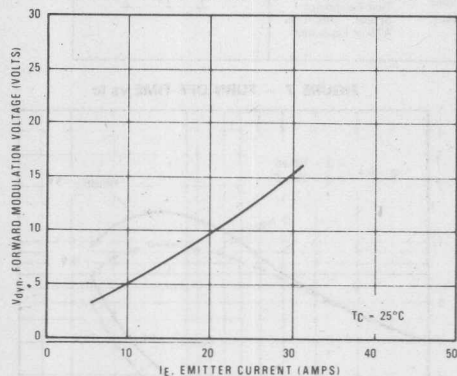


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

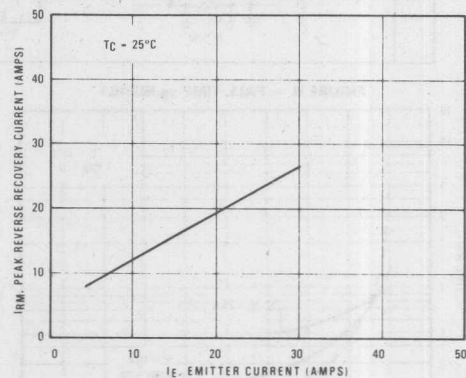


FIGURE 14 — FORWARD RECOVERY TIME

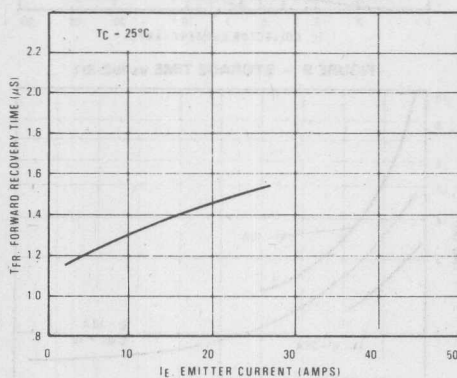
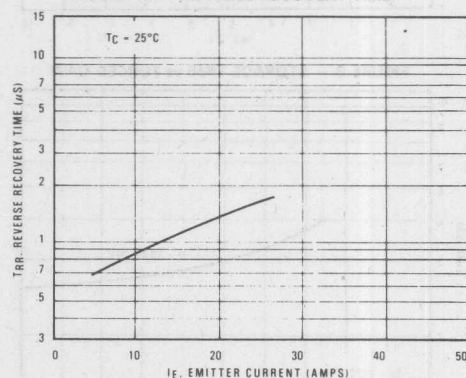


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

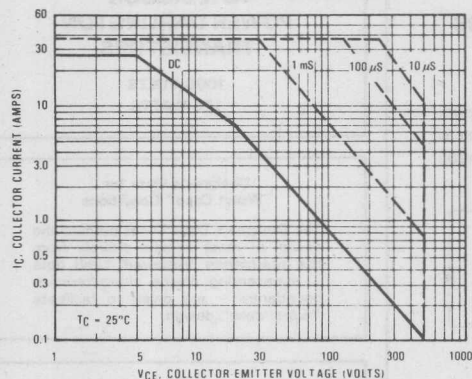
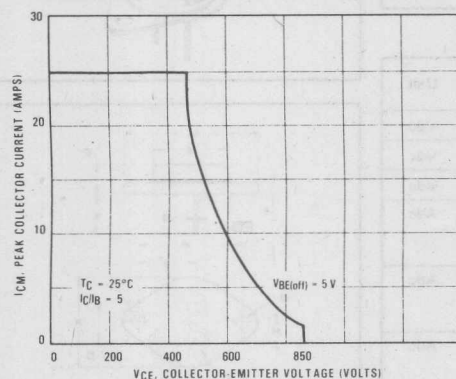


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

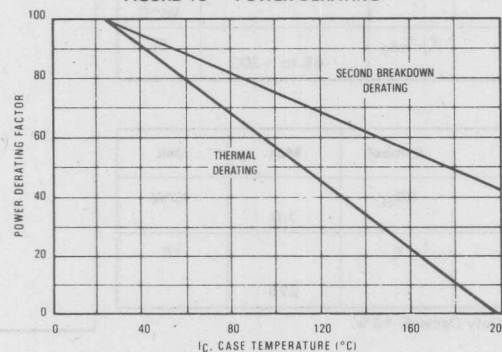
The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

FIGURE 18 — POWER DERATING

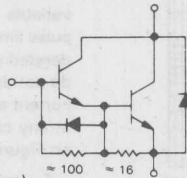




**SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE**

The BUT15 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 300 nS Inductive Fall Time at 25°C (Typ)
 - 1.2 μ S Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range - 65 to 200°C



MAXIMUM RATINGS

Rating	Symbol		Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	700	Vdc
Collector-Emitter Voltage	V_{CEV}	1000	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current	I_C	20	Adc
- Continuous	I_{CM}	25	
- Peak(1)			
Base Current	I_B	5	Adc
- Continuous	I_{BM}	10	
- Peak(1)			
Free Wheel Diode:			Adc
Forward current - Continuous	I_F	20	
- Peak	I_{FM}	25	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175	Watts
@ $T_C = 100^\circ\text{C}$		100	
Derate above 25°C			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

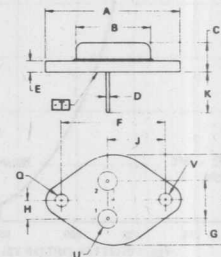
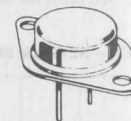
(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle \leq 10%.

**20 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS**

**1000 VOLTS
175 WATTS**

**Designer's Data for
"Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. \square IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

FOR LEADS
 $\phi .13 (0.005) \text{ } \odot \text{ } T \text{ } V \text{ } \odot$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37	1.550		
B	21.08	0.830		
C	6.35	0.250	0.300	
D	0.97	0.038	0.043	
E	3.43	0.135		
F	30.15 BSC	1.187 BSC		
G	10.92 BSC	0.430 BSC		
H	5.46 BSC	0.215 BSC		
J	16.89 BSC	0.665 BSC		
K	11.18	0.440	0.480	
L	3.81	0.150	0.165	
M	26.67	1.050		
N	4.83	0.190	0.210	
O	3.81	0.150	0.165	

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	700	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.1 2.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	$RBSOA$		See Figure 17	

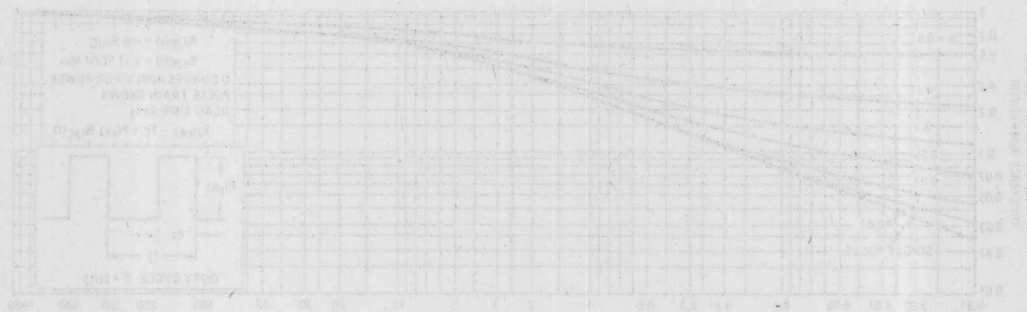
ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 6\text{ A}$, $V_{CE} = 5\text{ V}$) ($I_C = 12\text{ A}$, $V_{CE} = 5\text{ V}$)	h_{FE}	30 15	— —	— —	
Collector-Emitter Saturation Voltage ($I_C = 6\text{ A}$, $I_B = 0.3\text{ A}$) ($I_C = 12\text{ A}$, $I_B = 1.2\text{ A}$) ($I_C = 16\text{ A}$, $I_B = 1.6\text{ A}$) ($I_C = 20\text{ A}$, $I_B = 4\text{ A}$)	$V_{CE(sat)}$	— — — —	— — — —	2.0 3.0 3.5 5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 6\text{ A}$, $I_B = 0.3\text{ A}$) ($I_C = 12\text{ A}$, $I_B = 1.2\text{ A}$) ($I_C = 16\text{ A}$, $I_B = 1.6\text{ A}$)	$V_{BE(sat)}$	— — —	— — —	2.5 2.9 3.3	Vdc
Diode Forward Voltage ($I_F = 16\text{ A}$)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	$T_C = 25^\circ\text{C}$	See Table 1 $I_C = 12\text{ A}$	t_s	—	1.2	2.5	μs
Fall Time			t_f	—	0.3	0.8	μs
Storage Time	$T_C = 100^\circ\text{C}$	$I_{B1} = 1.2\text{ A}$ $V_{BE(off)} = 5\text{ V}$	t_s	—	1.4	—	μs
Fall Time			t_f	—	0.35	—	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

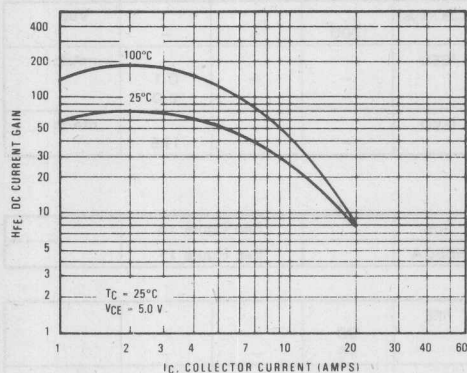


FIGURE 2 — COLLECTOR SATURATION REGION

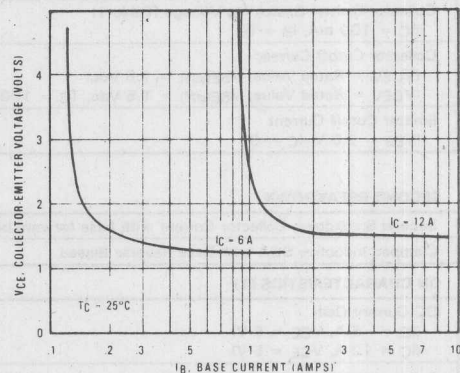


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

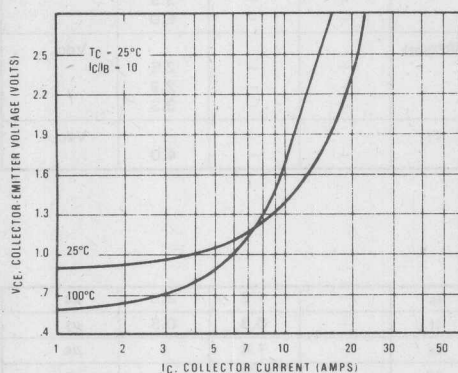


FIGURE 4 — BASE-EMITTER VOLTAGE

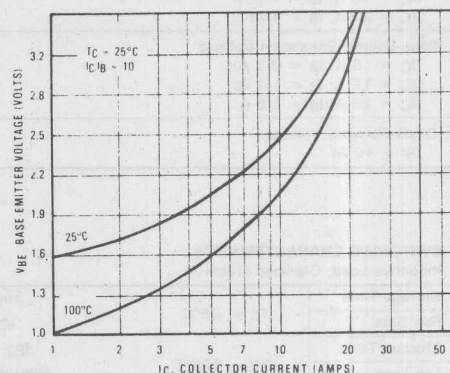


FIGURE 5 — THERMAL RESPONSE

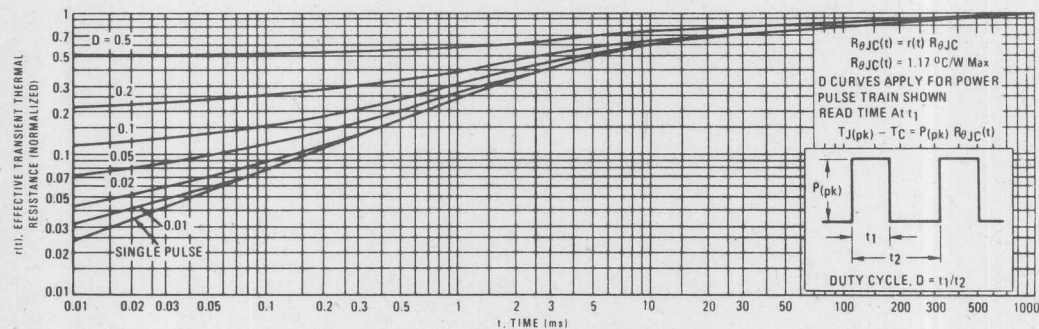


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

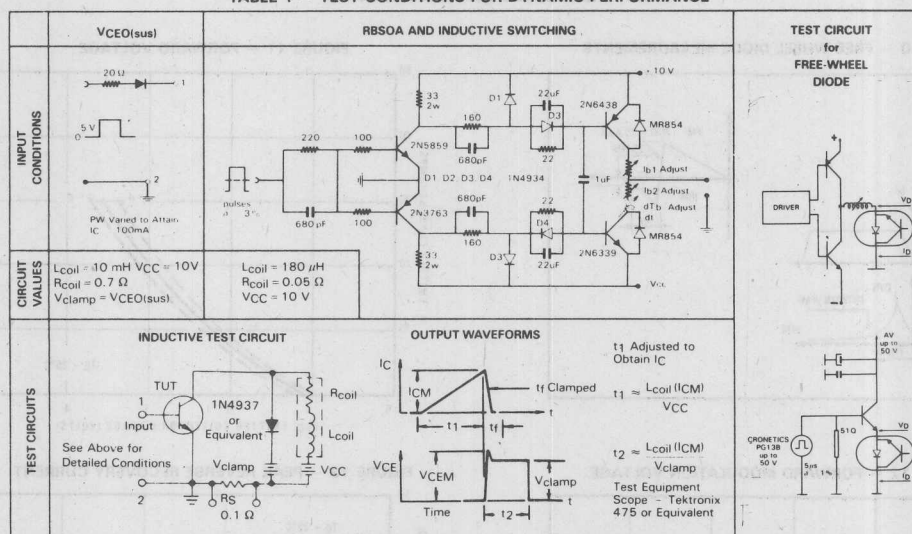
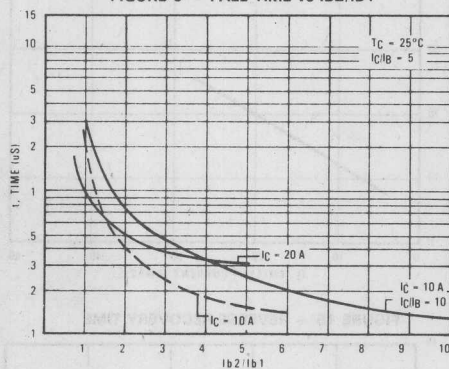
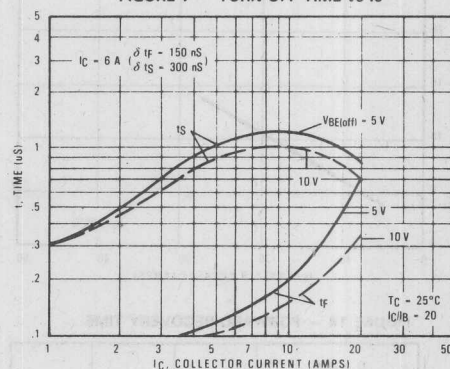
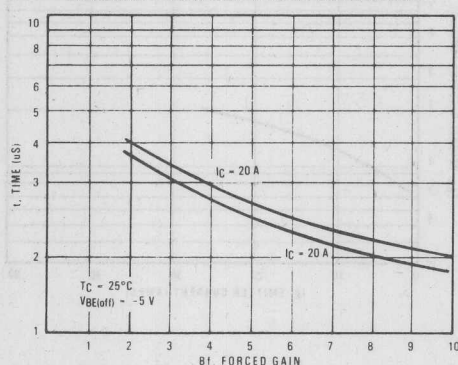
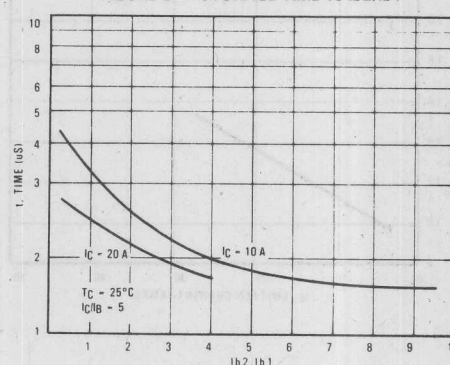
FIGURE 6 - FALL TIME vs I_{B2}/I_{B1} FIGURE 7 - TURN-OFF TIME vs I_C 

FIGURE 8 - STORAGE TIME vs FORCED GAIN

FIGURE 9 - STORAGE TIME vs I_{B2}/I_{B1} 

FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

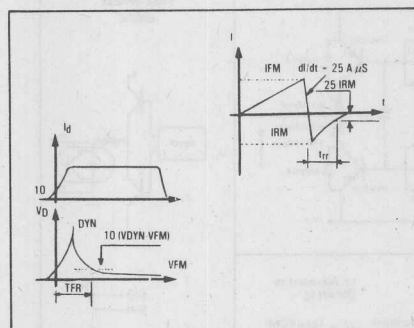


FIGURE 11 — FORWARD VOLTAGE

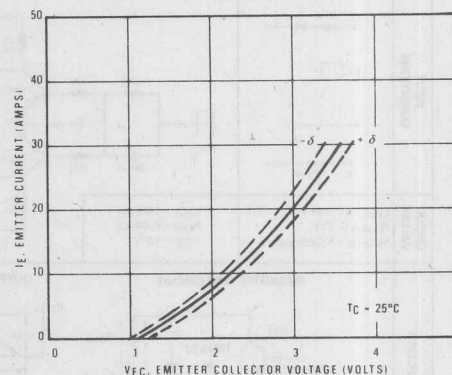


FIGURE 12 — FORWARD MODULATION VOLTAGE

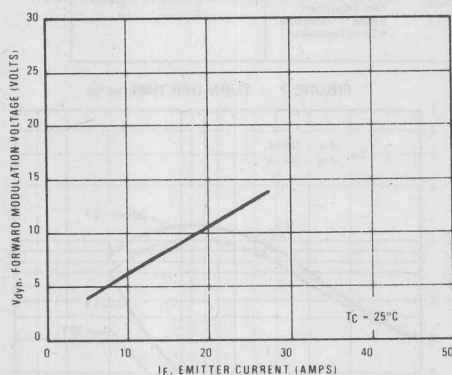


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

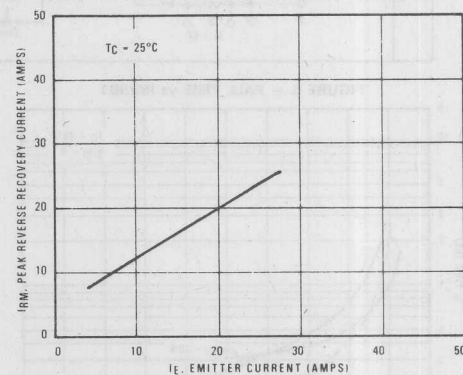


FIGURE 14 — FORWARD RECOVERY TIME

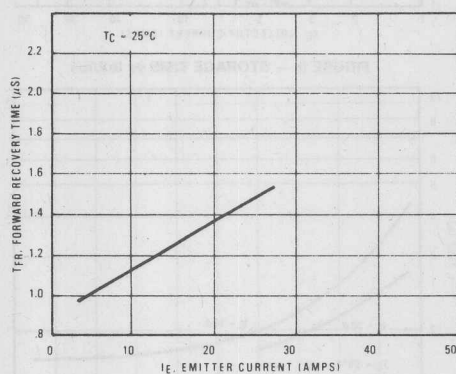
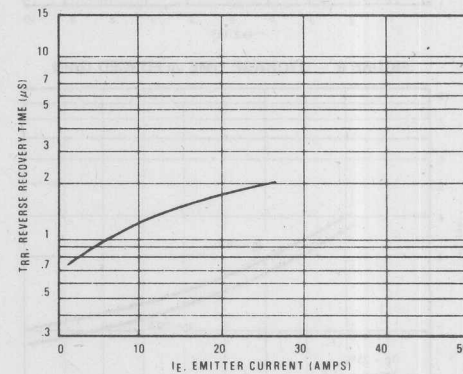


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

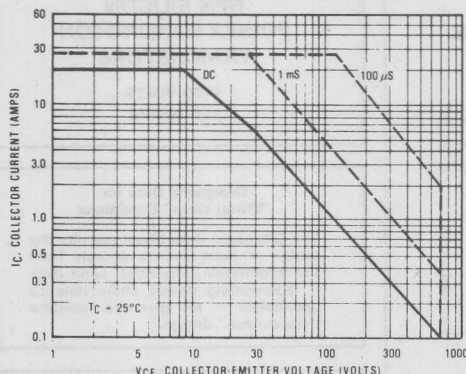


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA

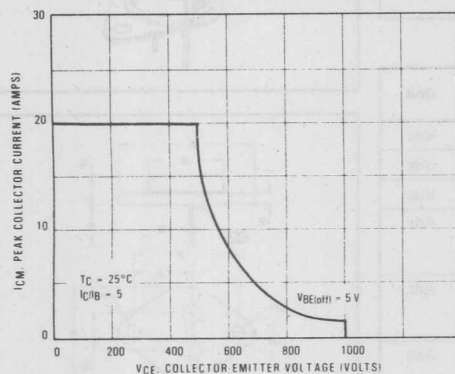
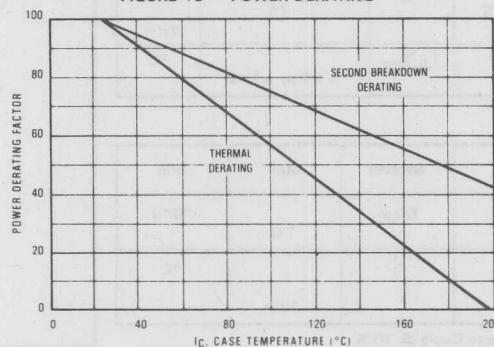


FIGURE 18 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

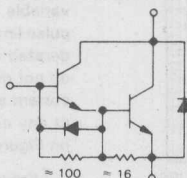
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**SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE**

The BUT 16 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 2.0 μ s Inductive Fall Time at 100°C (Typ)
 - 0.8 μ s Inductive Storage Time at 100°C (Typ)
- Operating Temperature Range - 65 to 175°C



MAXIMUM RATINGS

Rating	Symbol		Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	1000	Vdc
Collector-Emitter Voltage	V_{CEV}	1400	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current			Adc
- Continuous	I_C	12	
- Peak (1)	I_{CM}	20	
Base Current			Adc
- Continuous	I_B	8	
- Peak (1)	I_{BM}	10	
Free Wheel Diode:			Adc
Forward current	I_F	12	
- Peak	I_{FM}	20	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
@ $T_C = 100^\circ\text{C}$		75	
Derate above 25°C			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

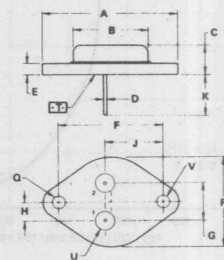
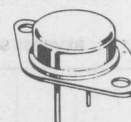
(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle \leq 10%.

**12 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS**

**1400 VOLTS
150 WATTS**

**Designer's Data for
"Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



- NOTES:
1 DIMENSIONS Q AND V ARE DATUMS
2 \square IS SEATING PLANE AND DATUM
3 POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

$\phi .13$ (0.005) ϕ T V ϕ

FOR LEADS:

$\phi .13$ (0.005) ϕ T V ϕ D ϕ

4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	5.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	-	3.43	-	0.135
F	30.15 BSC	-	1.187 BSC	-
G	10.92 BSC	-	0.430 BSC	-
H	5.46 BSC	-	0.215 BSC	-
J	16.89 BSC	-	0.665 BSC	-
K	11.18 12.78	-	0.440 0.500	-
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	1000	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.1 2.0	mA _{dc}
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	175	mA _{dc}

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	—	See Figure 16	—
Clamped Inductive SOA with Base Reverse Biased	RBSOA	—	See Figure 17	—

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 4\text{ A}$, $V_{CE} = 5\text{ V}$) ($I_C = 8\text{ A}$, $V_{CE} = 5\text{ V}$)	h_{FE}	20 5	— —	— —	—
Collector-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 6\text{ A}$)	$V_{CE(sat)}$	—	—	5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 1.6\text{ A}$)	$V_{BE(sat)}$	—	—	3.3	Vdc
Diode Forward Voltage ($I_F = 12\text{ A}$)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	$T_C = 25^\circ\text{C}$	See Table 1 $I_C = 8\text{ A}$	t_s	—	—	3.3	μs
Fall Time			t_f	—	—	1.5	μs
Storage Time	$T_C = 100^\circ\text{C}$	$I_{B1} = 1.6\text{ A}$ $V_{BE(off)} = 5\text{ V}$	t_s	—	2.0	—	μs
Fall Time			t_f	—	0.8	—	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

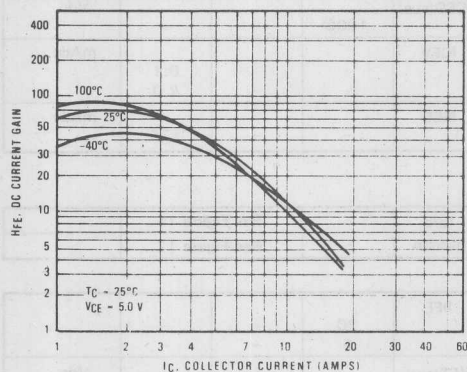


FIGURE 2 — COLLECTOR SATURATION REGION

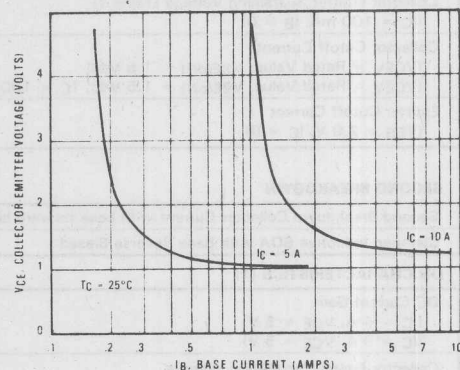


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

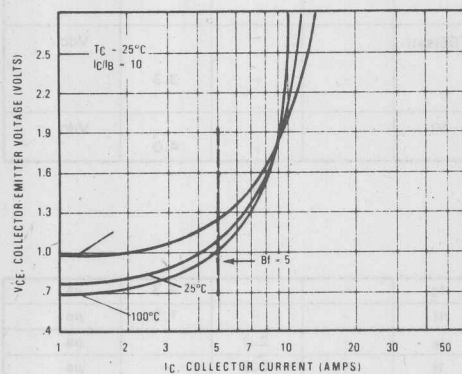


FIGURE 4 — BASE-EMITTER VOLTAGE

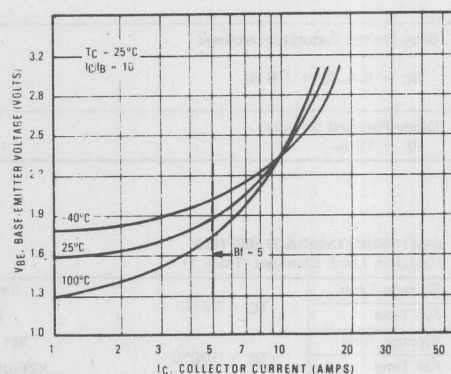


FIGURE 5 — THERMAL RESPONSE

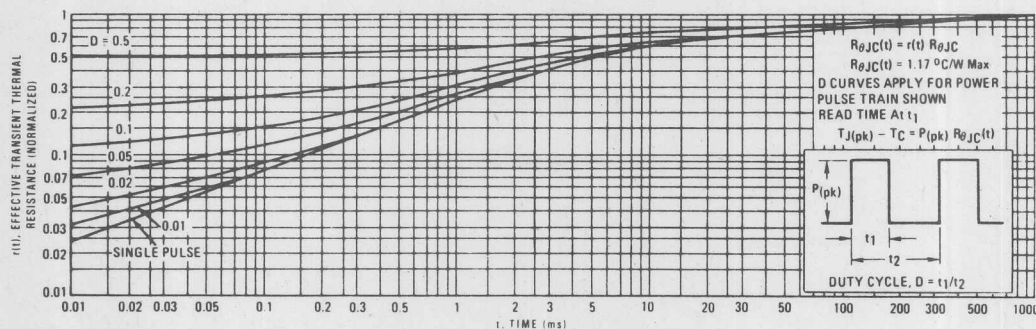


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE


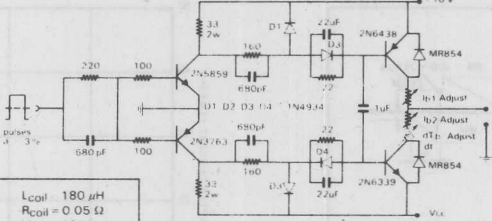
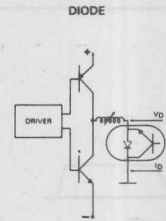
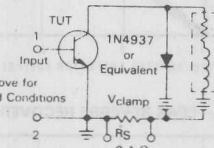
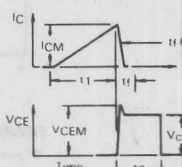
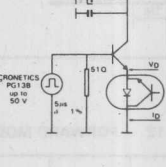
V _{CE0} (sus)	RBSOA AND INDUCTIVE SWITCHING	TEST CIRCUIT for FREE-WHEEL DIODE
INPUT CONDITIONS  PW Varied to Attain I _C = 100mA		
CIRCUIT VALUES L _{coil} = 10 mH V _{CC} = 10V R _{coil} = 0.7 Ω V _{clamp} = V _{CE0} (sus)	INDUCTIVE TEST CIRCUIT  OUTPUT WAVEFORMS  <p> t_1 Adjusted to Obtain I_C $t_1 = L_{coil} / (I_{CM} V_{CC})$ $t_2 = L_{coil} / (I_{CM} V_{clamp})$ Test Equipment Scope - Tektronix 475 or Equivalent </p>	

FIGURE 6 - FALL TIME vs IB2/IB1

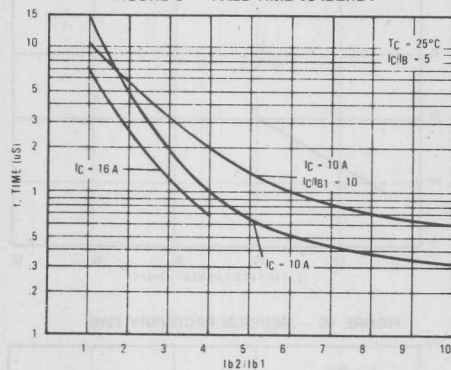


FIGURE 7 - TURN-OFF TIME vs IC

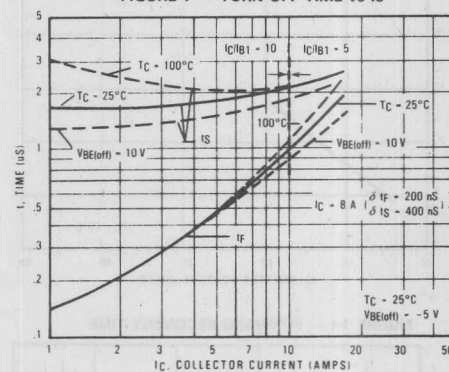


FIGURE 8 - STORAGE TIME vs FORCED GAIN

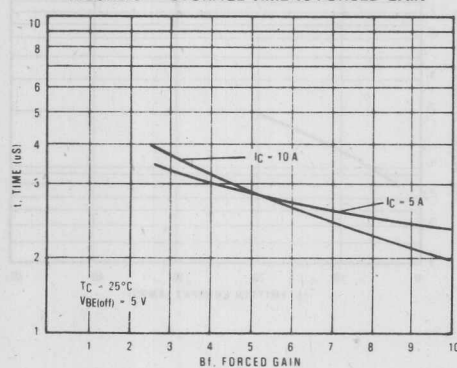
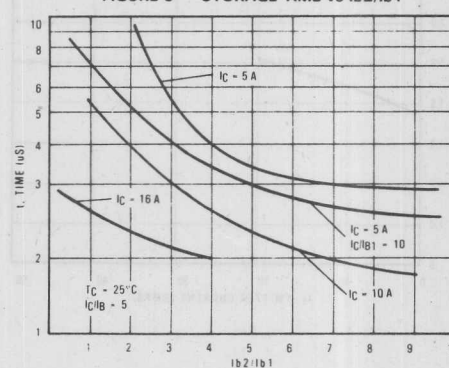


FIGURE 9 - STORAGE TIME vs IB2/IB1



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

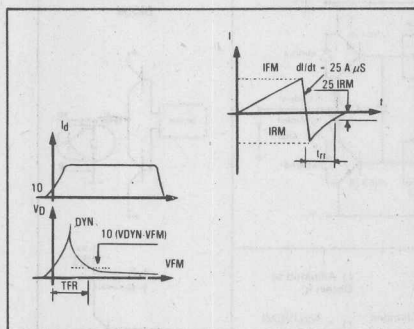


FIGURE 11 — FORWARD VOLTAGE

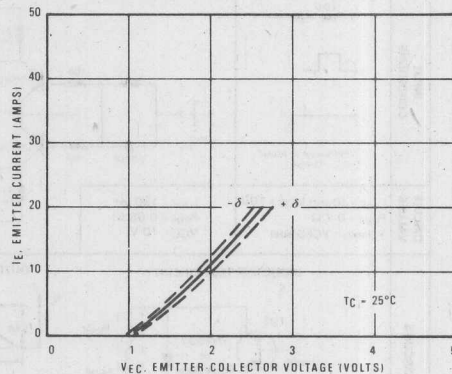


FIGURE 12 — FORWARD MODULATION VOLTAGE

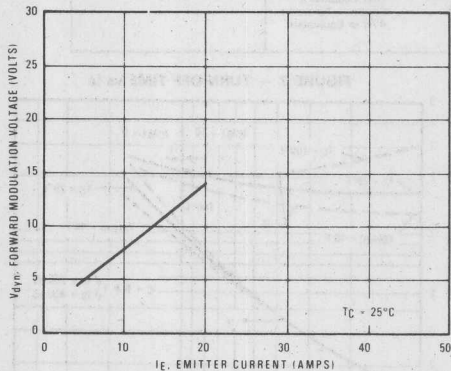


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

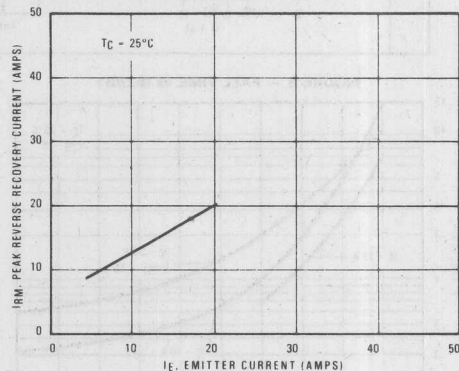


FIGURE 14 — FORWARD RECOVERY TIME

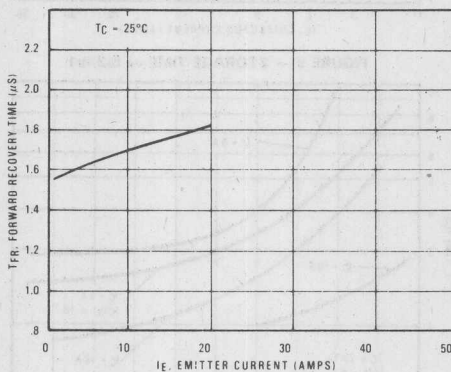
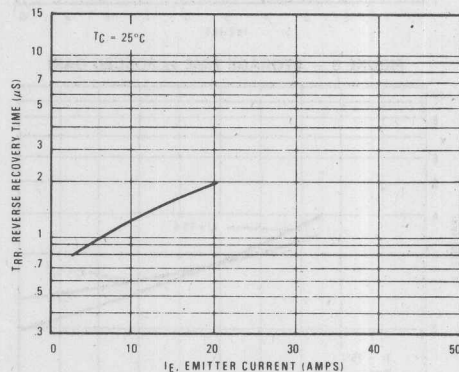


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

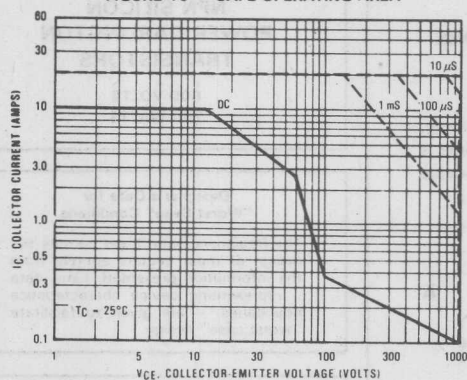


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA

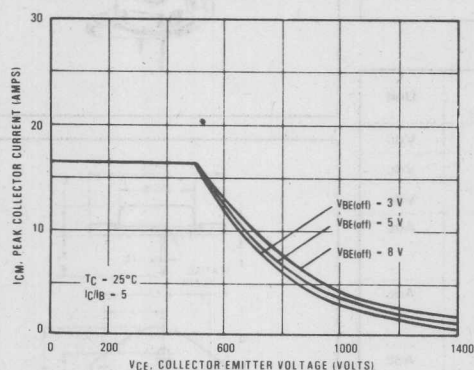
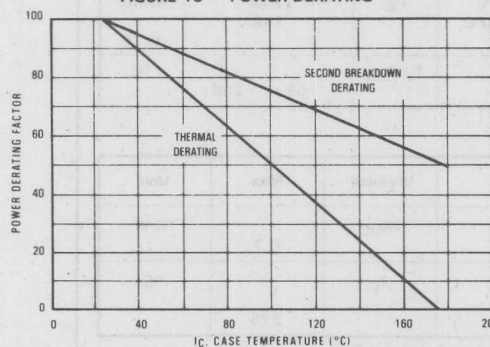


FIGURE 18 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.



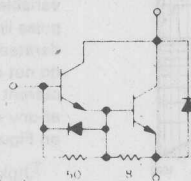
SWITCHMODE SERIES NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The BUT33 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times

800 nS Inductive Fall Time at 25°C (Typ)
2.0 μ S Inductive Storage Time at 25°C (Typ)

- Operating Temperature Range - 65 to 200°C



MAXIMUM RATINGS

Rating	Symbol		Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current			Adc
Continuous	I_C	56	
Peak (1)	I_{CM}	75	
Base Current			Adc
Continuous	I_B	12	
Peak (1)	I_{BM}	15	
Free Wheel Diode			Adc
Forward current	I_F	56	
Continuous			
Peak	I_{FM}	75	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250	Watts
(@ $T_C = 100^\circ\text{C}$)		140	
Derate above 25°C			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

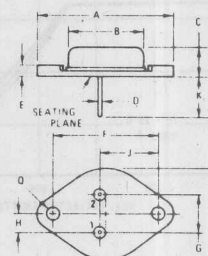
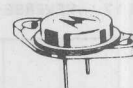
(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

56 AMPERES NPN SILICON POWER DARLINGTON TRANSISTORS

600 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



STYLE 1
PIN 1 BASE
PIN 2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37	1.550		
B	21.08	0.830		
C	6.35	0.250	0.300	
D	0.99	0.039	0.043	
E	3.43	0.135		
F	29.90	1.177	1.197	
G	10.67	0.420	0.440	
H	5.33	0.210	0.220	
J	10.64	0.419	0.435	
K	11.18	0.440	0.480	
L	3.84	0.151	0.161	
R	26.67	1.050		

CASE 197-01
MODIFIED TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	400	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.2 4.0	mA _{dc}
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	350	mA _{dc}

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	$RBSOA$		See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 20\text{ A}$, $V_{CE} = 5\text{ V}$) ($I_C = 36\text{ A}$, $V_{CE} = 5\text{ V}$)	h_{FE}	30 20	— —	— —	
Collector-Emitter Saturation Voltage ($I_C = 20\text{ A}$, $I_B = 1\text{ A}$) ($I_C = 36\text{ A}$, $I_B = 3.6\text{ A}$) ($I_C = 44\text{ A}$, $I_B = 4.4\text{ A}$) ($I_C = 56\text{ A}$, $I_B = 11.2\text{ A}$)	$V_{CE(sat)}$	— — — —	— — — —	2.0 2.5 3.0 5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 20\text{ A}$, $I_B = 1\text{ A}$) ($I_C = 36\text{ A}$, $I_B = 3.6\text{ A}$) ($I_C = 44\text{ A}$, $I_B = 4.4\text{ A}$)	$V_{BE(sat)}$	— — —	— — —	2.5 2.9 3.3	Vdc
Diode Forward Voltage ($I_F = 44\text{ A}$)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	$T_C = 25^\circ\text{C}$ See Table 1	$I_C = 36\text{ A}$ $I_B = 3.6\text{ A}$	t_s	—	2.0	3.3	μs
Fall Time			t_f	—	0.8	1.6	μs
Storage Time	$T_C = 100^\circ\text{C}$	$V_{BE(off)} = 5\text{ V}$	t_s	—	2.2	—	μs
Fall Time			t_f	—	0.8	—	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

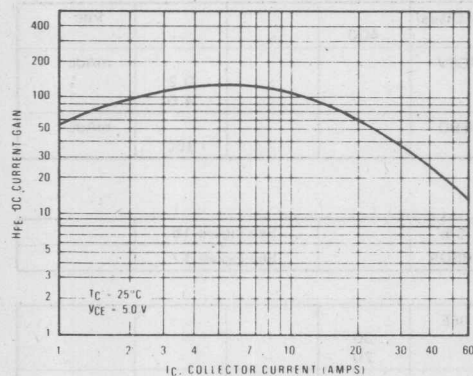


FIGURE 2 — COLLECTOR SATURATION REGION

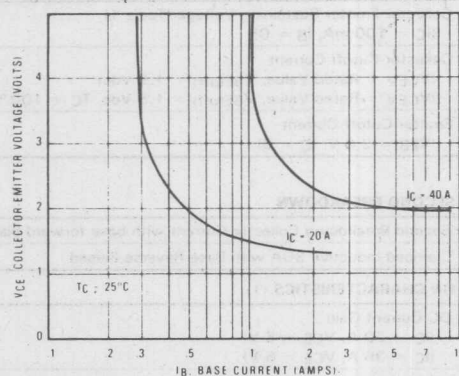


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

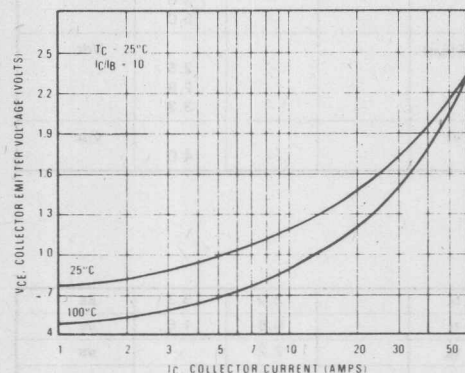


FIGURE 4 — BASE-EMITTER VOLTAGE

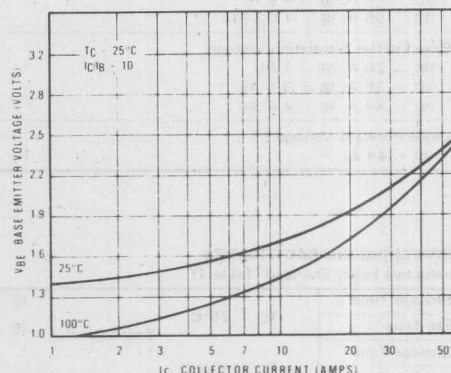
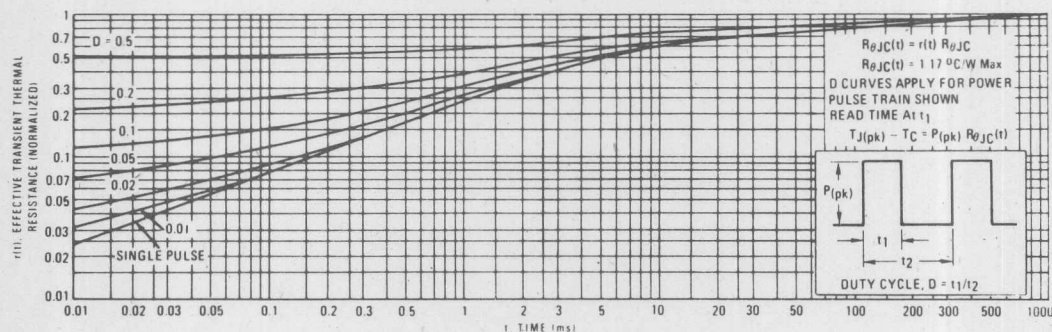


FIGURE 5 — THERMAL RESPONSE



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

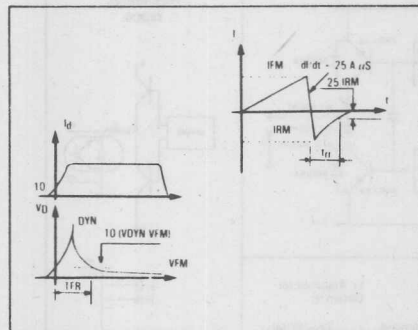


FIGURE 11 — FORWARD VOLTAGE

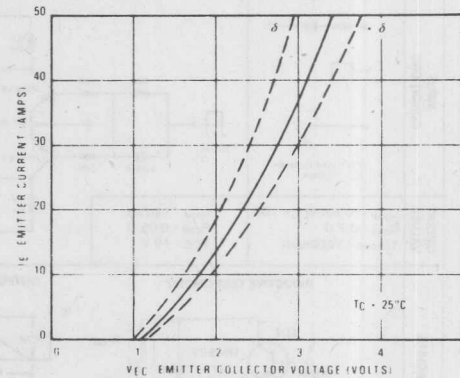


FIGURE 12 — FORWARD MODULATION VOLTAGE

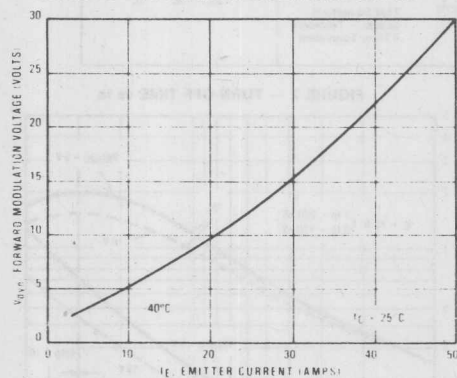


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

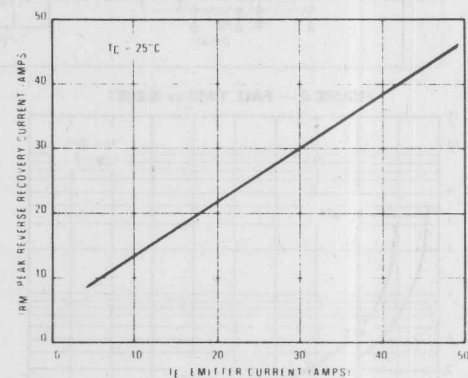


FIGURE 14 — FORWARD RECOVERY TIME

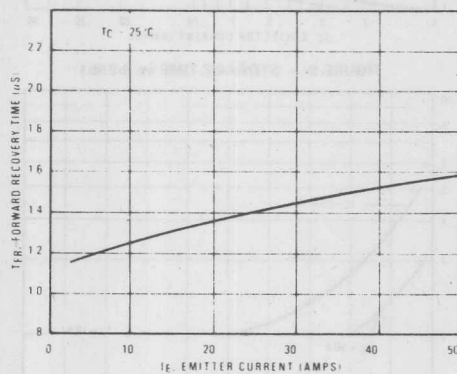
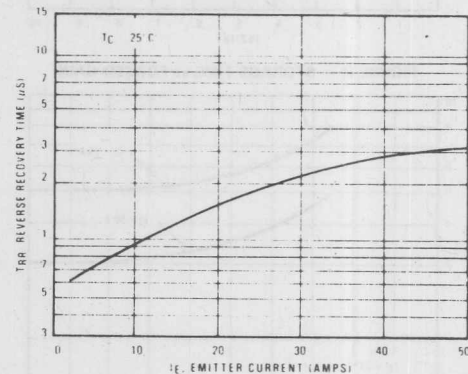


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 -- SAFE OPERATING AREA

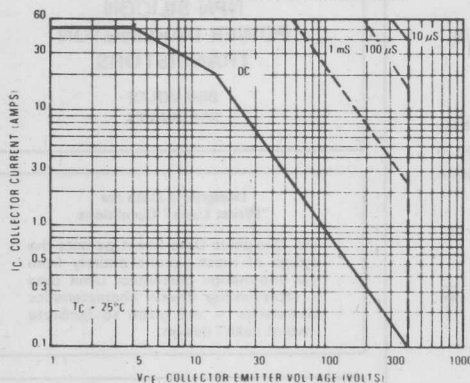


FIGURE 17 -- REVERSE BIAS SAFE OPERATING AREA

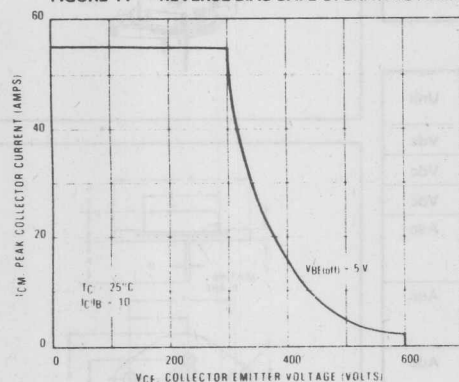
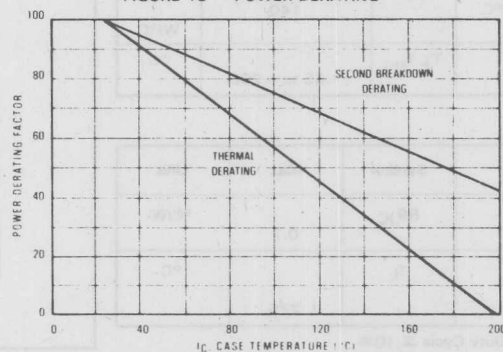


FIGURE 18 -- POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.



BUT 34

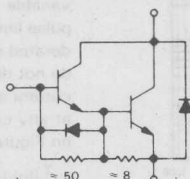
The BUT34 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times

0.7 μ S Inductive Fall Time at 25°C (Typ)

1.8 μ S Inductive Storage Time at 25°C (Typ)

- Operating Temperature Range – 65 to 200°C



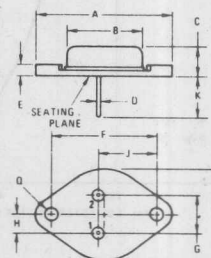
Rating	Symbol		Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current			Adc
– Continuous	I_C	50	
– Peak (1)	I_{CM}	75	
Base Current			Adc
– Continuous	I_B	10	
– Peak (1)	I_{BM}	15	
Free Wheel Diode:			Adc
Forward current – Continuous	I_F	50	
– Peak	I_{FM}	75	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	250	Watts
@ $T_C = 100^\circ C$		140	
Derate above $25^\circ C$			W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to +200	$^\circ C$

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test, Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

850 VOLTS
250 WATTS

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.02	0.039	0.041
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	18.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	-	1.050

CASE 197-01
MODIFIED TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	500	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.2 4.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	350	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 16\text{ A}$, $V_{CE} = 5\text{ V}$) ($I_C = 32\text{ A}$, $V_{CE} = 5\text{ V}$)	h_{FE}	30 15	— —	— —	
Collector-Emitter Saturation Voltage ($I_C = 16\text{ A}$, $I_B = 0.8\text{ A}$) ($I_C = 32\text{ A}$, $I_B = 3.2\text{ A}$) ($I_C = 40\text{ A}$, $I_B = 4\text{ A}$) ($I_C = 50\text{ A}$, $I_B = 10\text{ A}$)	$V_{CE(sat)}$	— — — —	— — — —	2.0 3.0 3.5 5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 16\text{ A}$, $I_B = 0.8\text{ A}$) ($I_C = 32\text{ A}$, $I_B = 3.2\text{ A}$) ($I_C = 40\text{ A}$, $I_B = 4\text{ A}$)	$V_{BE(sat)}$	— — —	— — —	2.5 2.9 3.3	Vdc
Diode Forward Voltage ($I_F = 40\text{ A}$)	V_f	—	—	4.0	Vdc

40°C

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	$T_C = 25^\circ\text{C}$	See Table 1 $I_C = 32\text{ A}$	t_s	—	1.8	3.0	μs
Fall Time			t_f	—	0.7	1.5	μs
Storage Time	$T_C = 100^\circ\text{C}$	$I_{B1} = 3.2\text{ A}$ $V_{BE(off)} = 5\text{ V}$	t_s	—	2.2	—	μs
Fall Time			t_f	—	0.8	—	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

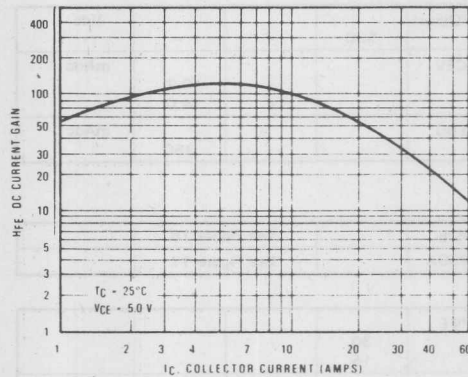


FIGURE 2 — COLLECTOR SATURATION REGION

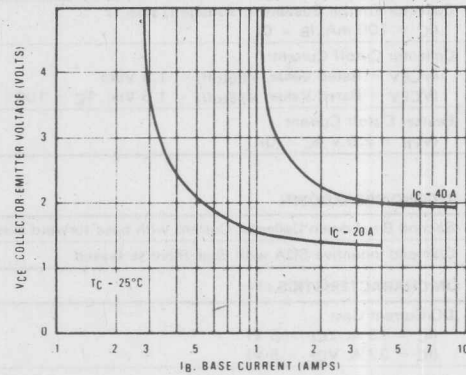


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

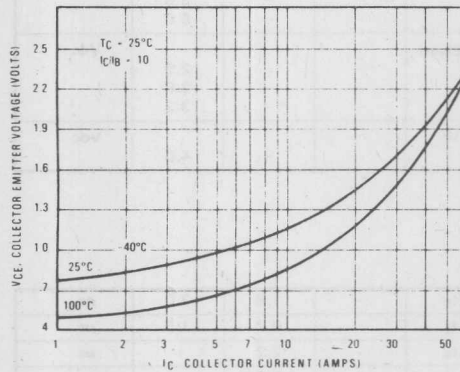


FIGURE 4 — BASE-EMITTER VOLTAGE

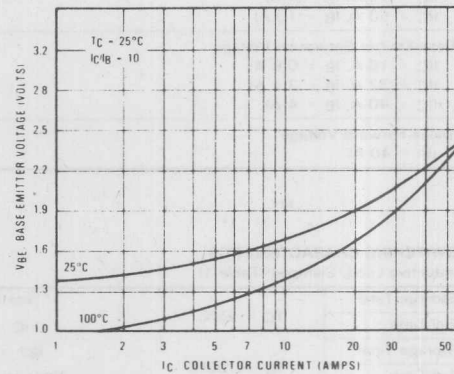


FIGURE 5 — THERMAL RESPONSE

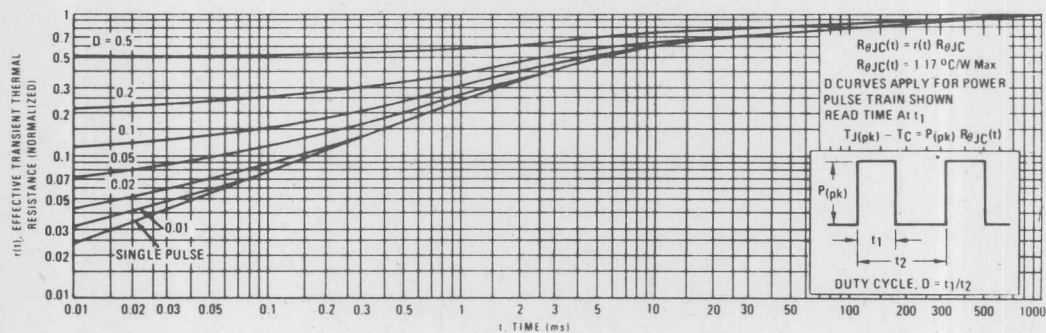


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

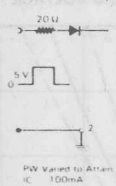
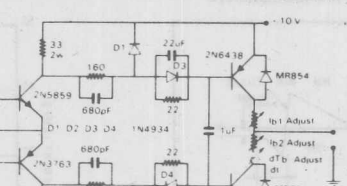
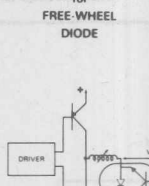
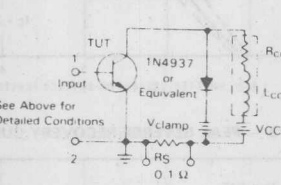
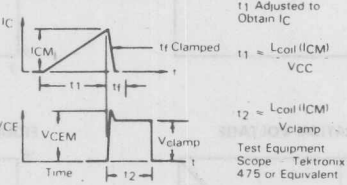
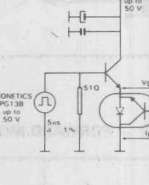
	VCE(sus)	RBSOA AND INDUCTIVE SWITCHING	TEST CIRCUIT for FREE-WHEEL DIODE
INPUT CONDITIONS	 <p>PW Varied to Attain I_C 100mA</p>		
CIRCUIT VALUES	$L_{coil} = 10\text{ mH}$ $V_{CC} = 10\text{ V}$ $R_{coil} = 0.7\ \Omega$ $V_{clamp} = V_{CE(sus)}$	$L_{coil} = 180\ \mu\text{H}$ $R_{coil} = 0.05\ \Omega$ $V_{CC} = 10\text{ V}$	
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p> t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil} I_{CM}}{V_{CC}}$ $t_2 \approx \frac{L_{coil} I_{CM}}{V_{clamp}}$ </p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	

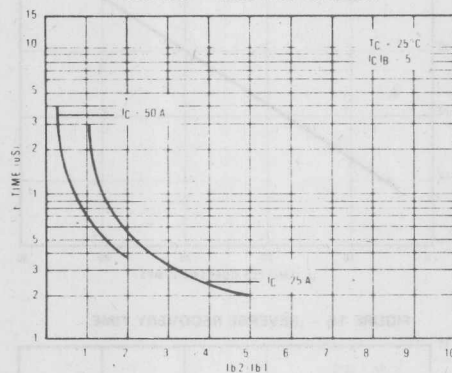
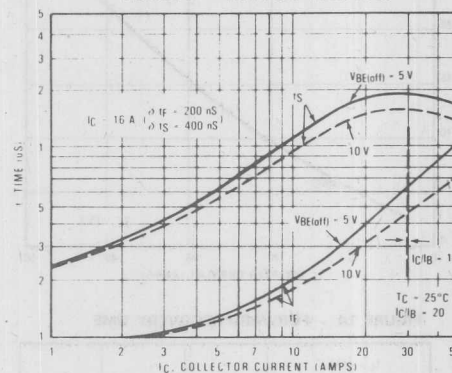
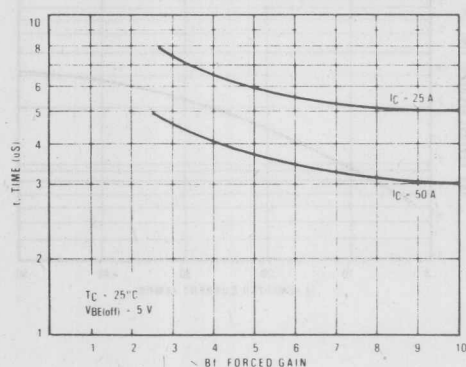
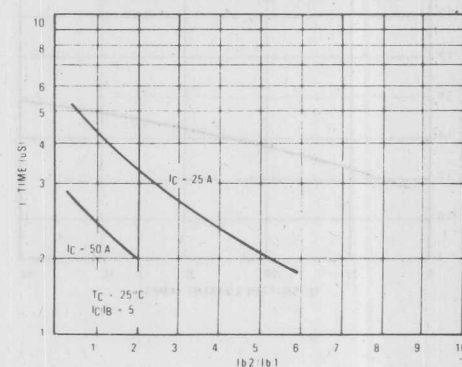
FIGURE 6 - FALL TIME vs I_{B2}/I_{B1} FIGURE 7 - TURN-OFF TIME vs I_C 

FIGURE 8 - STORAGE TIME vs FORCED GAIN

FIGURE 9 - STORAGE TIME vs I_{B2}/I_{B1} 

FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

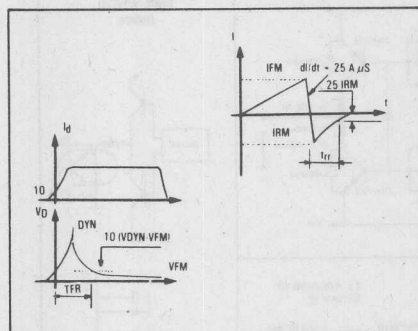


FIGURE 11 — FORWARD VOLTAGE

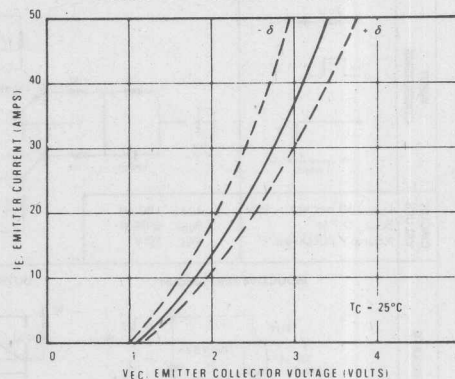


FIGURE 12 — FORWARD MODULATION VOLTAGE

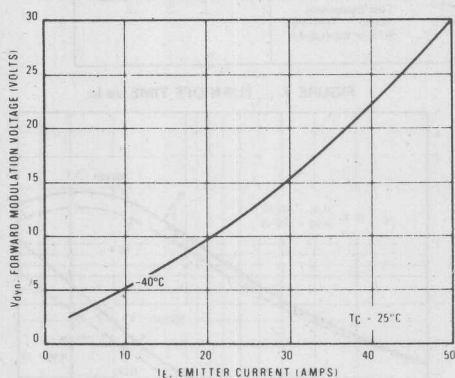


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

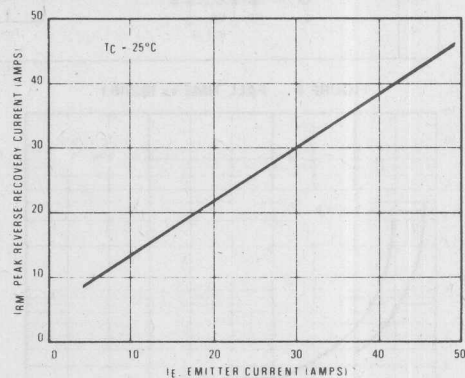


FIGURE 14 — FORWARD RECOVERY TIME

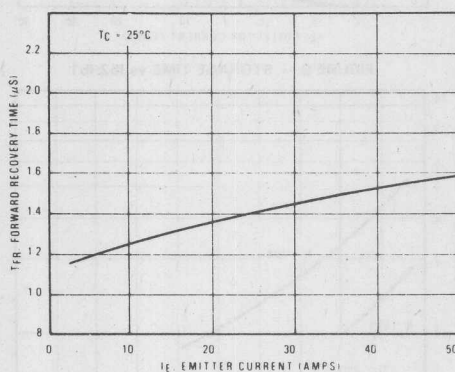
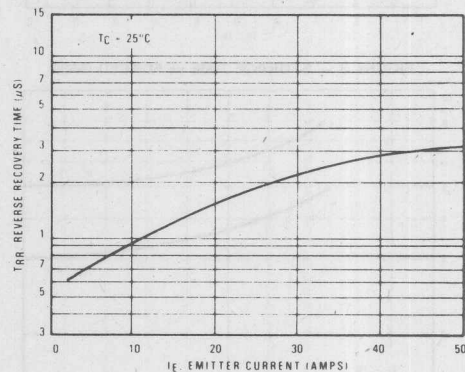


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

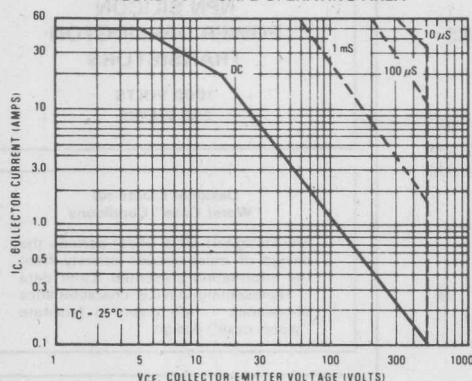


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA

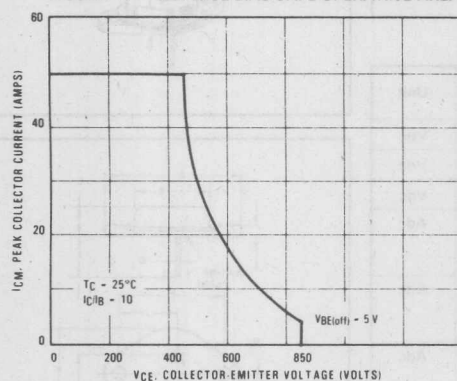
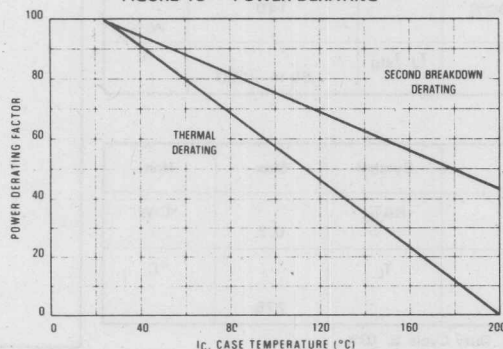


FIGURE 18 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_J(\text{pk})$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.



SWITCHMODE SERIES

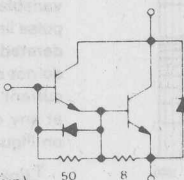
**NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE**

The BUT35 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times

550 nS Inductive Fall Time at 25°C (Typ)
2.5 μ S Inductive Storage Time at 25°C (Typ)

- Operating Temperature Range - 65 to 200°C



40 AMPERES

**NPN SILICON
POWER DARLINGTON
TRANSISTORS**

**1000 VOLTS
250 WATTS**

**Designer's Data for
"Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



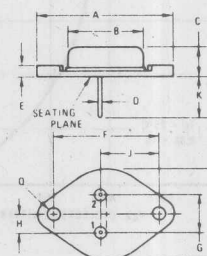
MAXIMUM RATINGS

Rating	Symbol		Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	700	Vdc
Collector-Emitter Voltage	V_{CEV}	1000	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current	I_C	40	Adc
- Continuous	I_{CM}	50	
Base Current	I_B	10	Adc
- Continuous	I_{BM}	20	
Free Wheel Diode:			
Forward current	I_F	40	Adc
Peak	I_{FM}	50	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250	Watts
@ $T_C = 100^\circ\text{C}$		140	
Derate above 25°C			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle \leq 10%.



STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		39.37		1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E		3.43		0.135
F	29.80	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R		26.67		1.050

**CASE 197-01
MODIFIED TO-3**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	700	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.2 4.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	350	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	$RBSOA$		See Figure 17	

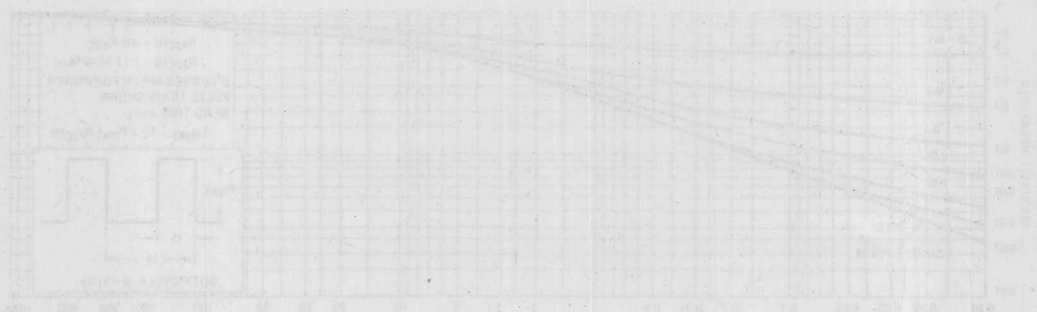
ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 12\text{ A}$, $V_{CE} = 5\text{ V}$) ($I_C = 24\text{ A}$, $V_{CE} = 5\text{ V}$)	h_{FE}	30 15	— —	— —	
Collector-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 0.6\text{ A}$) ($I_C = 24\text{ A}$, $I_B = 2.4\text{ A}$) ($I_C = 32\text{ A}$, $I_B = 3.2\text{ A}$) ($I_C = 40\text{ A}$, $I_B = 8\text{ A}$)	$V_{CE(sat)}$	— — — —	— — — —	2.0 3.0 3.5 5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 0.6\text{ A}$) ($I_C = 24\text{ A}$, $I_B = 2.4\text{ A}$) ($I_C = 32\text{ A}$, $I_B = 3.2\text{ A}$)	$V_{BE(sat)}$	— — —	— — —	2.5 2.9 3.3	Vdc
Diode Forward Voltage ($I_F = 32\text{ A}$)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	$T_C = 25^\circ\text{C}$	See Table 1	t_s	—	—	4.0	μs
Fall Time			t_f	—	—	1.2	μs
Storage Time	$T_C = 100^\circ\text{C}$	$I_{B1} = 2.4\text{ A}$ $V_{BE(off)} = 5\text{ V}$	t_s	—	2.8	—	μs
Fall Time			t_f	—	0.65	—	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

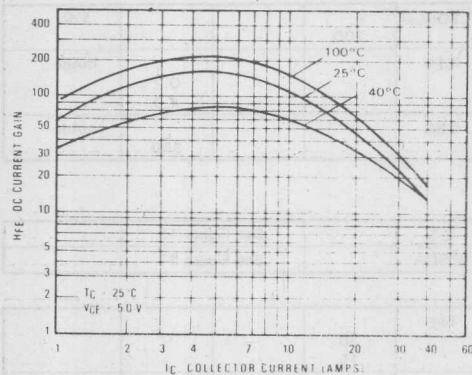


FIGURE 2 — COLLECTOR SATURATION REGION

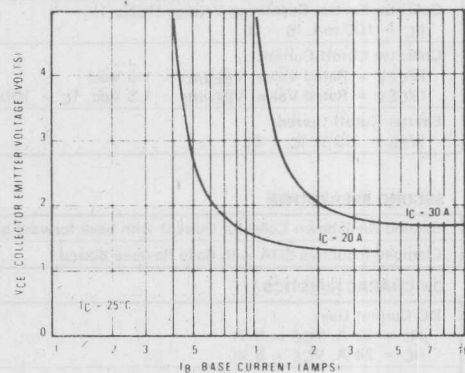


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

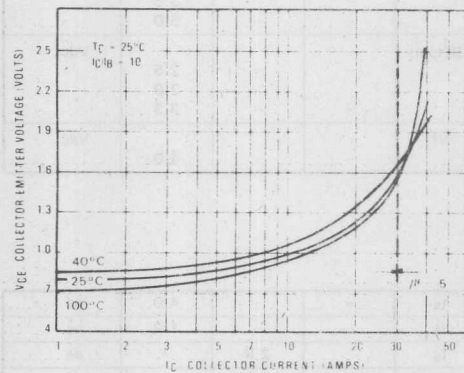


FIGURE 4 — BASE-EMITTER VOLTAGE

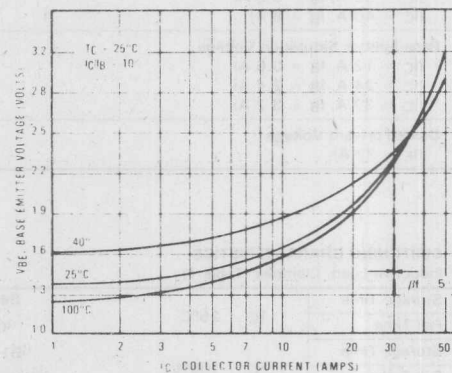
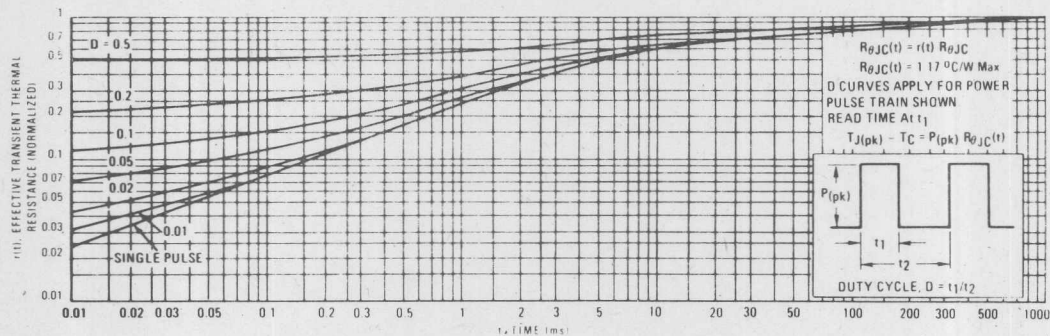


FIGURE 5 — THERMAL RESPONSE



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

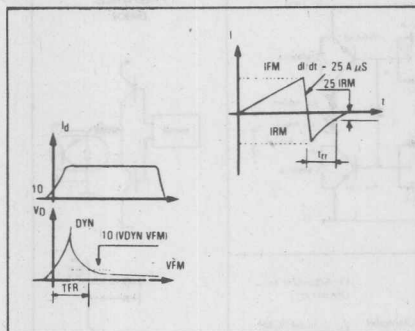


FIGURE 11 — FORWARD VOLTAGE

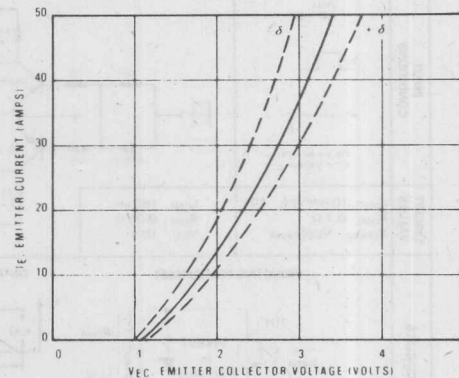


FIGURE 12 — FORWARD MODULATION VOLTAGE

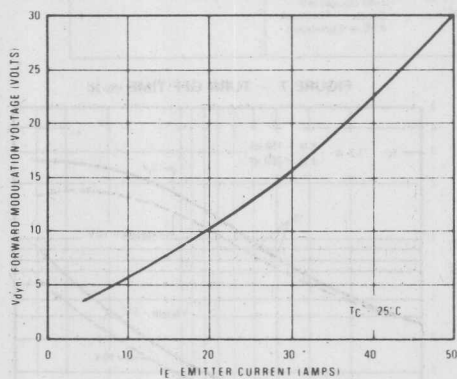


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

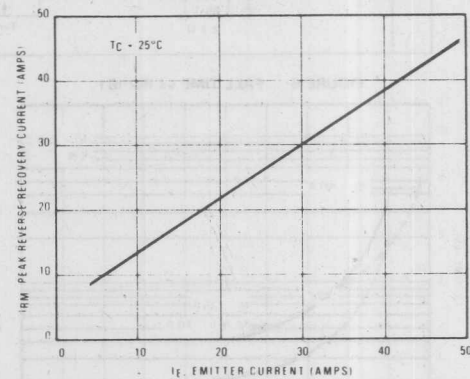


FIGURE 14 — FORWARD RECOVERY TIME

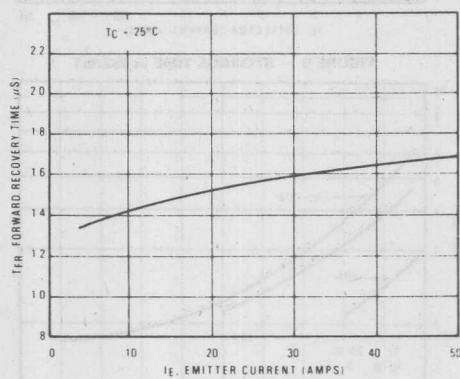
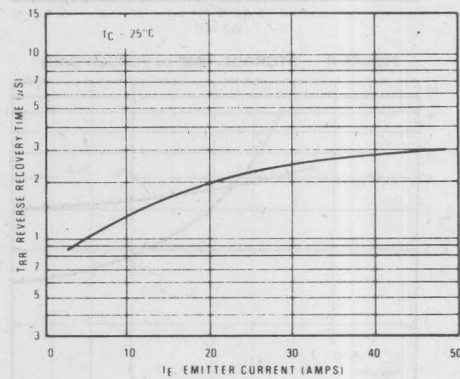


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

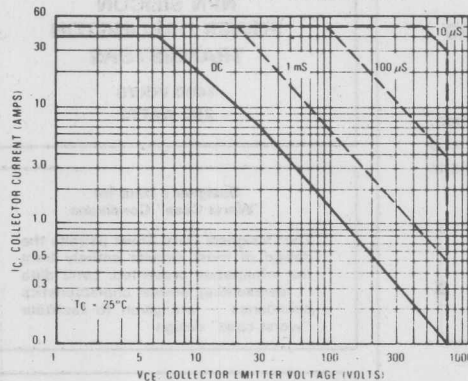


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA

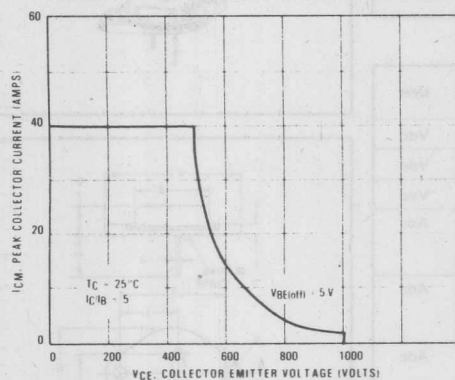
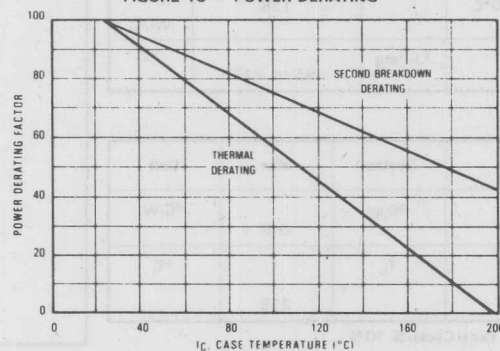


FIGURE 18 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

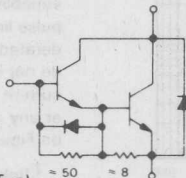
REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

SWITCHMODE SERIES **NPN SILICON POWER DARLINGTON TRANSISTORS** **WITH BASE-EMITTER SPEEDUP DIODE**

The BUT36 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 1.7 μ s Inductive Fall Time at 100°C (Typ)
 - 4.5 μ s Inductive Storage Time at 100°C (Typ)
- Operating Temperature Range - 65 to 175°C



MAXIMUM RATINGS

Rating	Symbol		Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	1000	Vdc
Collector-Emitter Voltage	V_{CEV}	1400	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current	I_C	24	Adc
- Continuous	I_{CM}	40	
- Peak (1)			
Base Current	I_B	15	Adc
- Continuous	I_{BM}	20	
- Peak (1)			
Free Wheel Diode:			Adc
Forward current - Continuous	I_F	24	
- Peak	I_{FM}	40	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250	Watts
Derate above 25°C @ $T_C = 100^\circ\text{C}$		125	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

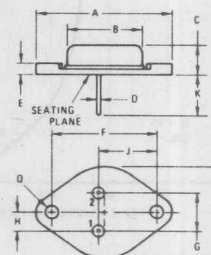
(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle \leq 10%.

24 AMPERES **NPN SILICON** **POWER DARLINGTON** **TRANSISTORS**

1400 VOLTS
250 WATTS

Designer's Data for **"Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



STYLE 1
 PIN 1 BASE
 2 EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	5.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	-	1.050

CASE 197-01
MODIFIED TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	1000	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.2 4.0	mA _{dc}
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	350	mA _{dc}

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	$RBSOA$		See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 8\text{ A}$, $V_{CE} = 5\text{ V}$) ($I_C = 16\text{ A}$, $V_{CE} = 5\text{ V}$)	h_{FE}	20 5	—	—	
Collector-Emitter Saturation Voltage ($I_C = 24\text{ A}$, $I_B = 12\text{ A}$)	$V_{CE(sat)}$	—	—	5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 16\text{ A}$, $I_B = 3.2\text{ A}$)	$V_{BE(sat)}$	—	—	3.3	Vdc
Diode Forward Voltage ($I_F = 24\text{ A}$)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	$T_C = 25^\circ\text{C}$	See Table 1 $I_C = 16\text{ A}$	t_s	—	—	6.0	μs
Fall Time			t_f	—	—	2.5	μs
Storage Time	$T_C = 100^\circ\text{C}$	$I_{B1} = 3.2\text{ A}$ $V_{BE(off)} = 5\text{ V}$	t_s	—	4.5	—	μs
Fall Time			t_f	—	1.7	—	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

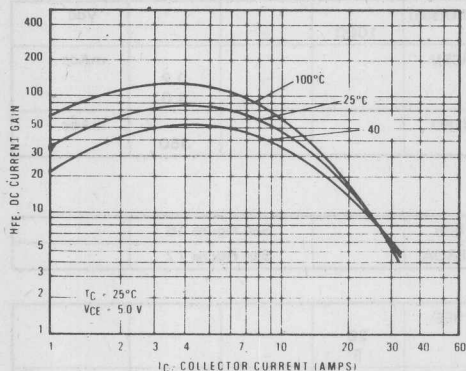


FIGURE 2 — COLLECTOR SATURATION REGION

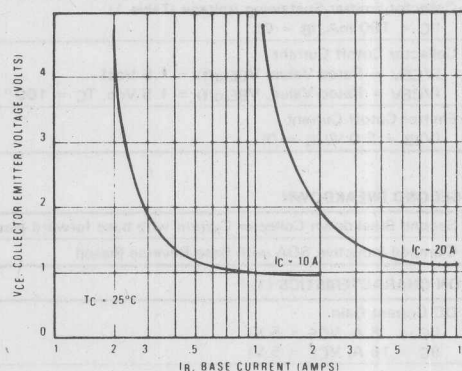


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

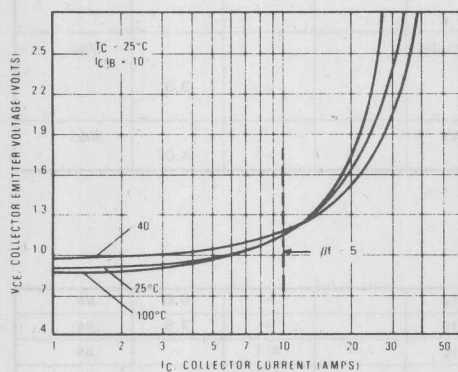


FIGURE 4 — BASE-EMITTER VOLTAGE

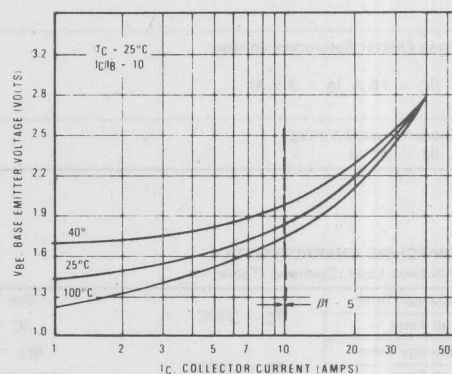


FIGURE 5 — THERMAL RESPONSE

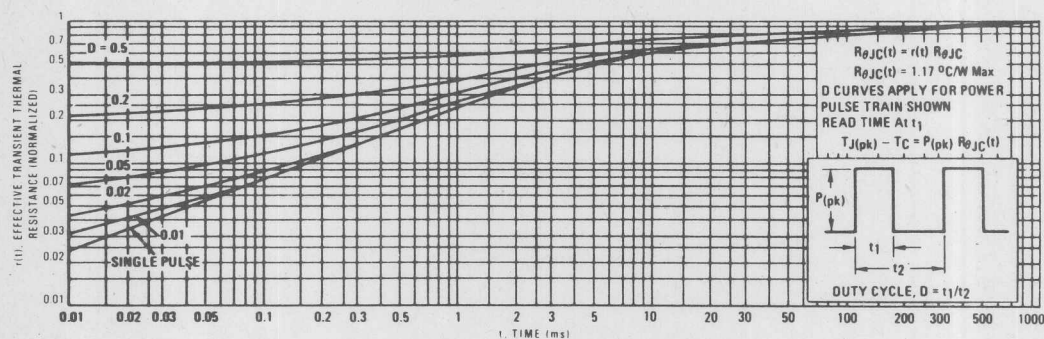


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	VCE(sus)	RBSOA AND INDUCTIVE SWITCHING		TEST CIRCUIT for FREE-WHEEL DIODE
INPUT CONDITIONS	 PW Varied to Attain IC = 100mA			
CIRCUIT VALUES	Lcoil = 10 mH VCC = 10V Rcoil = 0.7 Ω Vclamp = VCE(sus)	Lcoil = 180 μH Rcoil = 0.05 Ω VCC = 10 V		
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT See Above for Detailed Conditions		OUTPUT WAVEFORMS t1 Adjusted to Obtain IC $t_1 = L_{coil} / (I_{CM} - V_{CC})$ $t_2 = L_{coil} / (I_{CM} - V_{clamp})$ Test Equipment: Scope Tektronix 475 or Equivalent	

FIGURE 6 - FALL TIME vs IB2/IB1

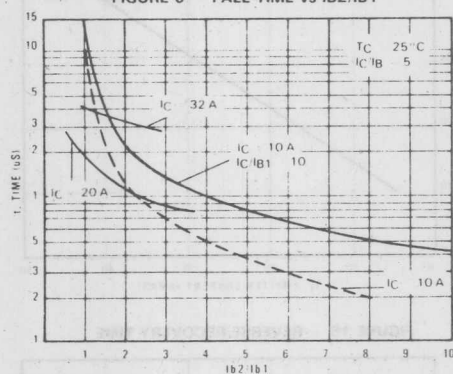


FIGURE 7 - TURN-OFF TIME vs IC

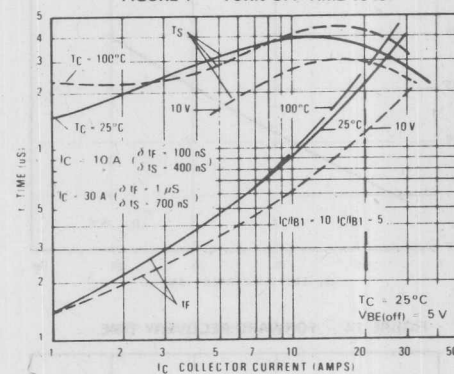


FIGURE 8 - STORAGE TIME vs FORCED GAIN

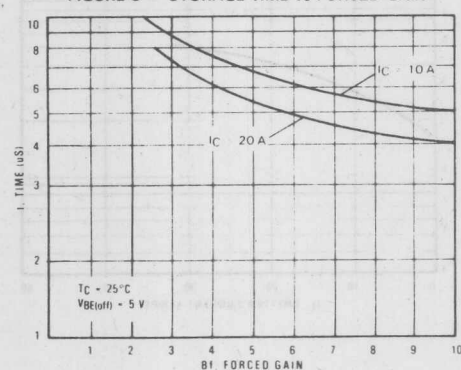
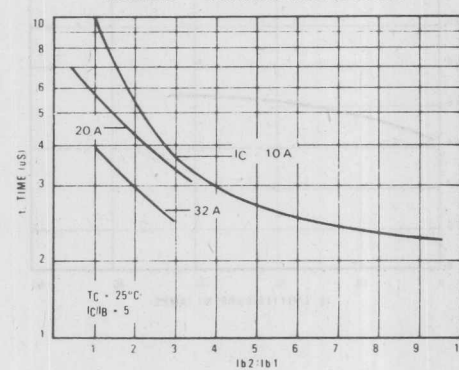


FIGURE 9 - STORAGE TIME vs IB2/IB1



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

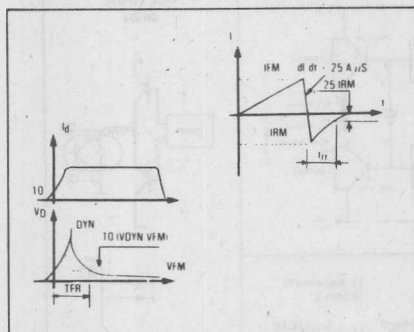


FIGURE 11 — FORWARD VOLTAGE

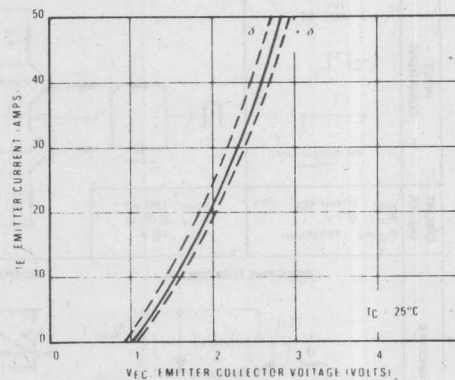


FIGURE 12 — FORWARD MODULATION VOLTAGE

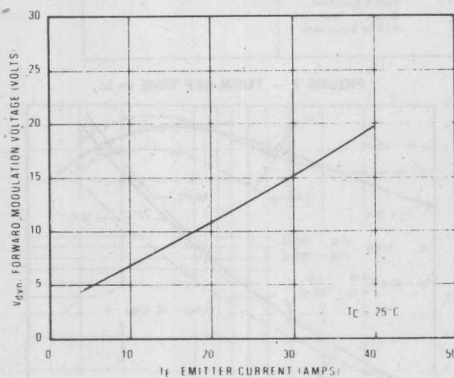


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

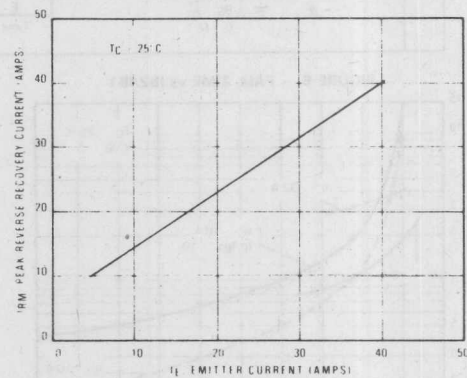


FIGURE 14 — FORWARD RECOVERY TIME

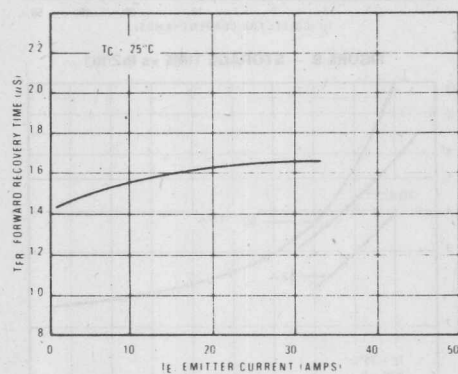
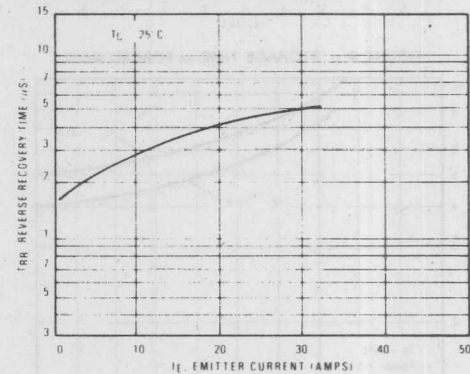


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

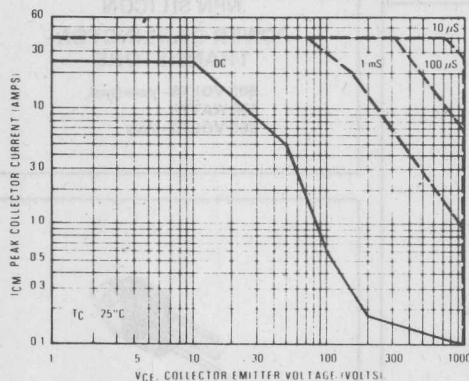


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA

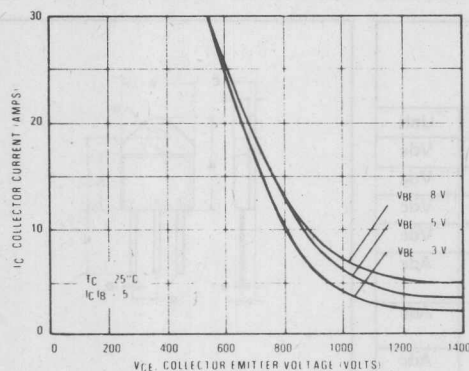
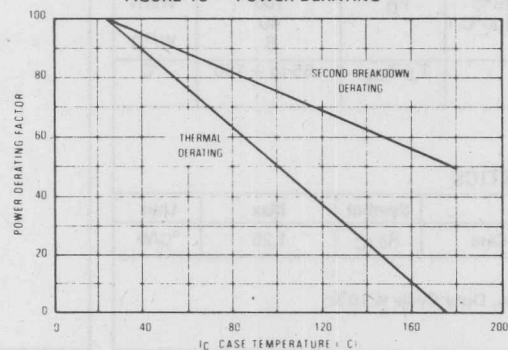


FIGURE 18 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

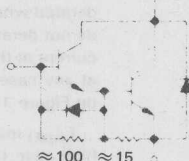
REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

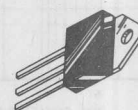
**MOTOROLA****BUT 50P****ADVANCE INFORMATION****SWITCHMODE[▲] SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS**

The BUT50P darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switch-mode applications such as :

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits


**8 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS**

500 VOLTS- $V_{CE0(sus)}$
100 WATTS
850 VOLTS- V_{CES}

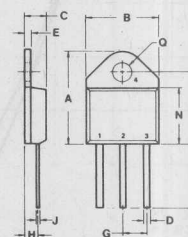
**MAXIMUM RATINGS**

Rating	Symbol	BUT50P	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	500	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	850	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	8	Vdc
Collector Current — Continuous	I_C	8	Adc
— Peak (1)	I_{CM}	16	
Base Current — Continuous	I_B	2	Adc
— Peak (1)	I_{BM}	4	
Free Wheel Diode :			
Forward Current — continous	I_F	8	Adc
— peak	I_{FM}	16	
Total Power Dissipation @ $T_C=25^{\circ}C$	P_D	100	Watts
@ $T_C=100^{\circ}C$		40	
Derate above $25^{\circ}C$.8	W/ $^{\circ}C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to + 150	$^{\circ}C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^{\circ}C/W$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.48	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.18	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

Case 340-01
TO-218AC

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 8.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc

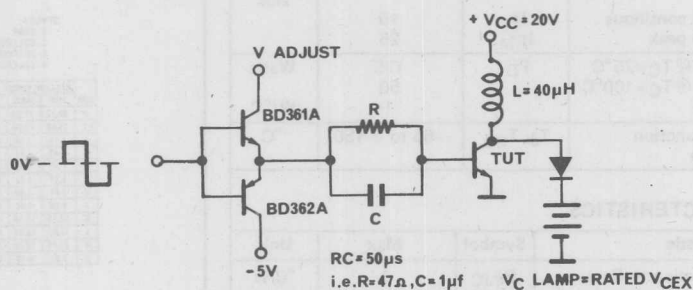
ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 2\text{ Adc}$, $V_{CE} = 5\text{ V}$)	h_{FE}	30	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 0.25\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 5\text{ Adc}$, $I_B = 0.25\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.0 3.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 0.25\text{ Adc}$) ($I_C = 5\text{ Adc}$, $I_B = 0.25\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage ($I_F = 5\text{ Adc}$)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped

Storage Time	($I_C = 5\text{ A}$, $I_{B1} = 0.25\text{ A}$, $V_{BE(off)} = 5\text{ V}$)	t_s	—	0.75	—	μs
Fall Time		t_f	—	0.10	—	μs

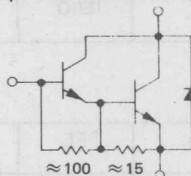
(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$ **SWITCHING TIMES TEST CIRCUIT**

ADVANCE INFORMATION

SWITCHMODE[▲] SERIES NPN SILICON POWER DARLINGTON TRANSISTORS

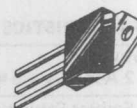
The BUT51P darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switch-mode applications such as :

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



15 AMPERES NPN SILICON POWER DARLINGTON TRANSISTORS

500 VOLTS- $V_{CE0(sus)}$
100 WATTS
850 VOLTS- V_{CES}



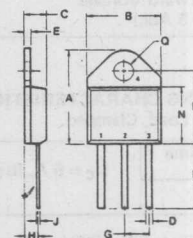
MAXIMUM RATINGS

Rating	Symbol	BUT51P	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	500	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	850	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	8	Vdc
Collector Current — Continuous	I_C	15	Adc
— Peak (1)	I_{CM}	25	
Base Current — Continuous	I_B	2.5	Adc
— Peak (1)	I_{BM}	5	
Free Wheel Diode :			
Forward Current — continous	I_F	15	Adc
— peak	I_{FM}	25	
Total Power Dissipation @ $T_C=25^\circ\text{C}$	P_D	125	Watts
@ $T_C=100^\circ\text{C}$		50	
Derate above 25°C		1	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to + 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	$^\circ\text{C/W}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.48	15.90	0.610	0.626
C	4.19	5.09	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
F	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.48	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

Case 340-01
TO-218AC

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	0.25 2.5	— —	— —	mAdc
Emitter Cutoff Current ($V_{EB} = 8.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc

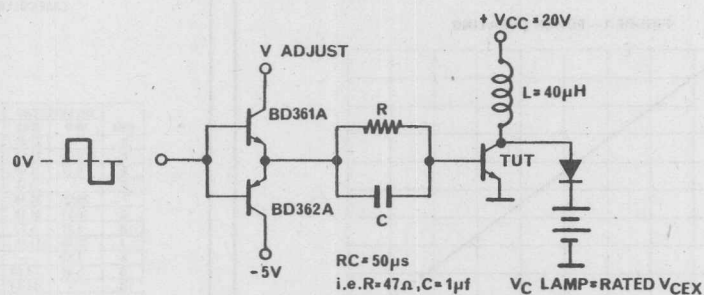
ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 5\text{ Adc}$, $V_{CE} = 5\text{ V}$)	h_{FE}	40	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 1.5\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 0.55\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.0 3.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 0.55\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage ($I_F = 10\text{ Adc}$)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped

Storage Time	($I_C = 10\text{ A}$, $I_{B1} = 0.5\text{ A}$, $V_{BE(off)} = 5\text{ V}$)	t_s	—	1.1	—	μs
Fall Time		t_f	—	0.16	—	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$ **SWITCHING TIMES TEST CIRCUIT**



MOTOROLA

BUV 10N

**SWITCHMODE^Δ SERIES
NPN SILICON POWER TRANSISTOR**

... designed for high current, high speed, high power applications.

- H_{FE} min.: 20 at $I_C = 10$ A
- T_F max. = $0.45 \mu s$ at $I_C = 15$ A
- Equivalent to BDY58

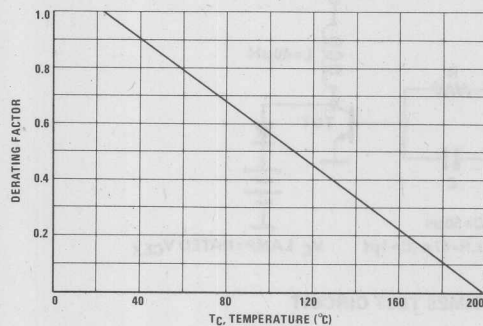
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	160	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	140	Vdc
Collector-Current — continuous	I_C	25	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	30	Apk
Base-Current continuous	I_B	6	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	175	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	$^\circ C/W$

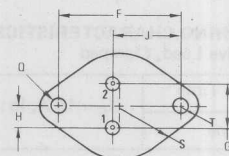
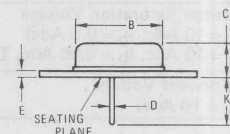
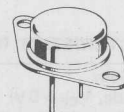
FIGURE 1 — POWER DERATING



25 AMPERES

**NPN SILICON
POWER
METAL TRANSISTOR**

**125 VOLTS
175 WATTS**



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

**CASE 1-03
(TO-3)**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 160\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 160\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.5 6	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 100\text{ V}$)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		0.5	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 0.5\text{ s}$) ($V_{CE} = 48\text{ V}$, $t = 0.5\text{ s}$)	$I_{S/b}$	8.75 1.0		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 10\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 20\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 1\text{ A}$) ($I_C = 20\text{ A}$, $I_B = 2\text{ A}$)	$V_{CE(sat)}$		1 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 1\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	10.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 15\text{ A}$, $I_{B1} = I_{B2} = 1.5\text{ A}$, ($V_{CC} = 75\text{ V}$, $R_C = 5\ \Omega$)	t_{on}	1.0	μs
Storage Time		t_s	1.55	
Fall Time		t_f	0.45	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA

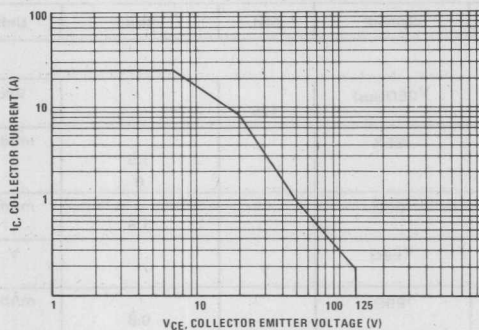


FIGURE 3 - "ON" VOLTAGES

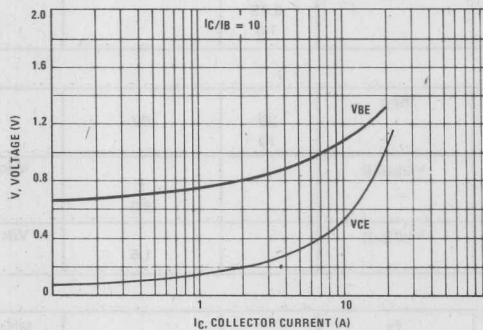
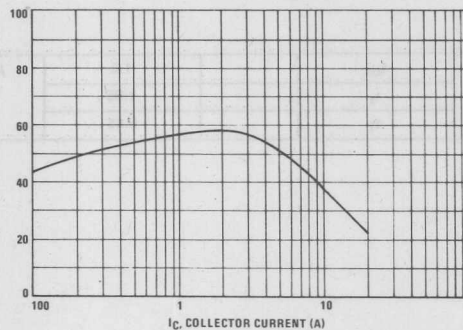


FIGURE 4 - DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 - RESISTIVE SWITCHING PERFORMANCE

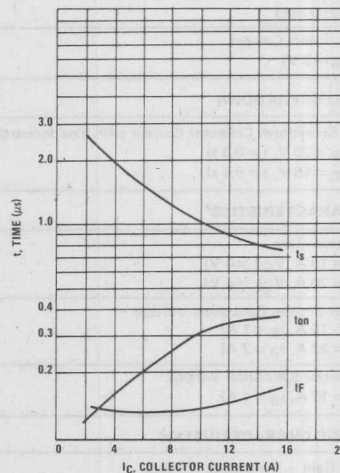
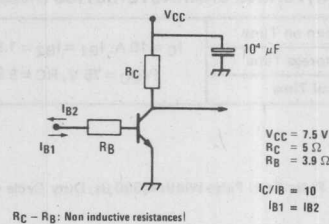


FIGURE 6 - SWITCHING TIMES TEST CIRCUIT





MOTOROLA

BUV 11

**SWITCHMODE^Δ SERIES
NPN SILICON POWER TRANSISTOR**

... designed for high current, high speed, high power applications.

- High DC current gain: $HFE \text{ min.} = 20$ at $I_C = 6 \text{ A}$
- Low $V_{CE(sat)}$, $V_{CE(sat)} \text{ max.} = 0.6 \text{ V}$ at $I_C = 6 \text{ A}$
- Very fast switching times:
 $T_F \text{ max.} = 0.8 \mu\text{s}$ at $I_C = 12 \text{ A}$

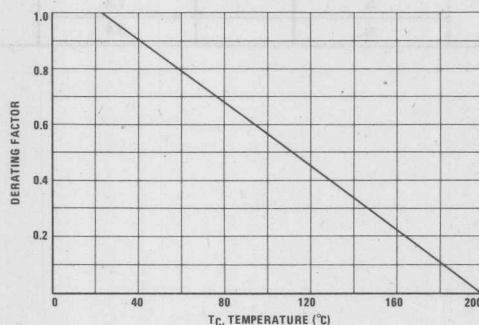
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector-Base Voltage	V_{CBO}	250	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5 \text{ V}$)	V_{CEX}	250	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	240	Vdc
Collector-Current — continuous	I_C	20	Adc
— peak ($p_w \leq 10 \text{ ms}$)	I_{CM}	25	Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C/W}$

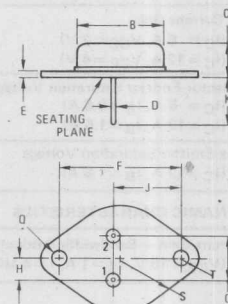
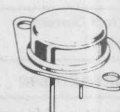
FIGURE 1 — POWER DERATING



20 AMPERES

**NPN SILICON
POWER
METAL TRANSISTOR**

**200 VOLTS
150 WATTS**



STYLE 1:
PIN 1: BASE
2: EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1: BASE
2: COLLECTOR
CASE: EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.5 6	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 160\text{ V}$)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	5.0 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 6\text{ A}$, $V_{CE} = 2\text{ V}$) ($I_C = 12\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 6\text{ A}$, $I_B = 0.6\text{ A}$) ($I_C = 12\text{ A}$, $I_B = 1.5\text{ A}$)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 1.5\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 12\text{ A}$, $I_{B1} = I_{B2} = 1.5\text{ A}$, ($V_{CC} = 150\text{ V}$, $R_C = 12.5\ \Omega$)	t_{on}	0.8	μs
Storage Time		t_s	1.8	
Fall Time		t_f	0.4	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

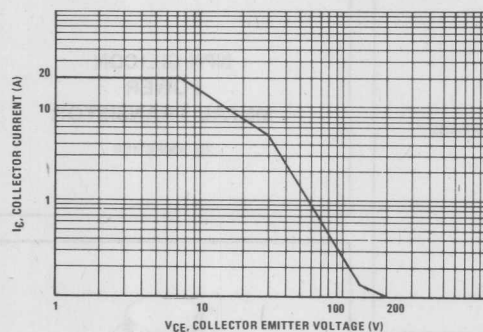


FIGURE 3 – "ON" VOLTAGES

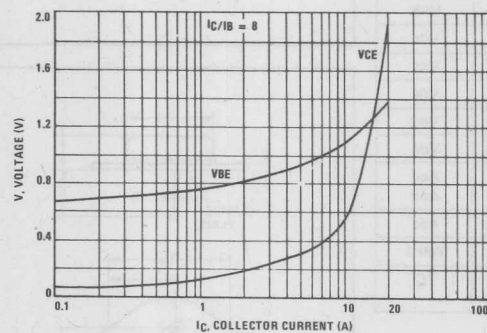
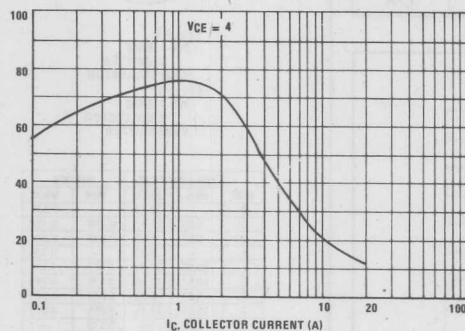


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – SWITCHING TIMES VERSUS COLLECTOR CURRENT

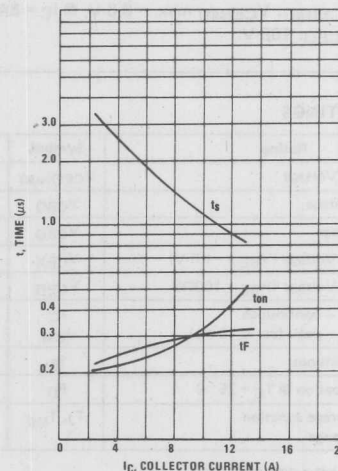
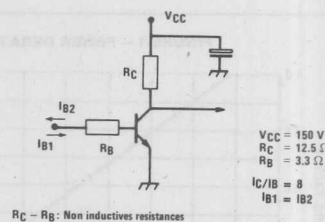


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



**MOTOROLA****BUV11N****NPN SILICON POWER METAL TRANSISTOR**

... designed for high speed, high current, high power applications.

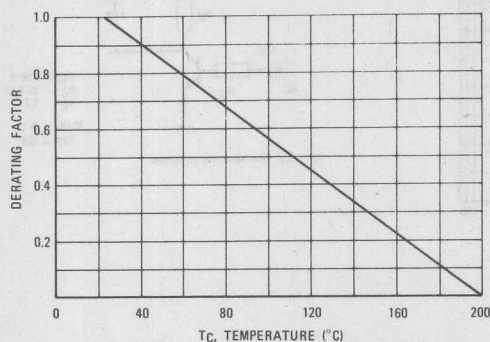
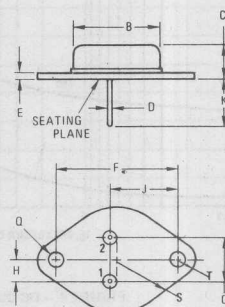
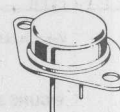
- High DC Current gain — H_{FE} min 20 @ $I_C = 8$ A
- Very fast switching times
 t_F max. = $0.25 \mu s$ @ $I_C = 15$ A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$ max. = 0.6 V, @ $I_C = 8$ A
- High V_{CEO} : 160 V.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	160	Vdc
Collector-Base Voltage	V_{CBO}	220	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	220	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	200	Vdc
Collector-Current — continuous	I_C	20	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	25	Apk
Base-Current continuous	I_B	5	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ C/W$

FIGURE 1 — POWER DERATING**NPN SILICON POWER METAL TRANSISTOR****20 AMPERES**

STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE-COLLECTOR

STYLE 2:
 PIN 1. BASE
 2. COLLECTOR
 CASE-EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	160		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.5 6.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 130\text{ V}$)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	5 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 8\text{ A}$, $V_{CE} = 2\text{ V}$) ($I_C = 15\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 0.8\text{ A}$) ($I_C = 15\text{ A}$, $I_B = 1.88\text{ A}$)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 15\text{ A}$, $I_B = 1.88\text{ A}$)	$V_{BE(sat)}$		1.8	Vdc

DYNAMIC CHARACTERISTICS

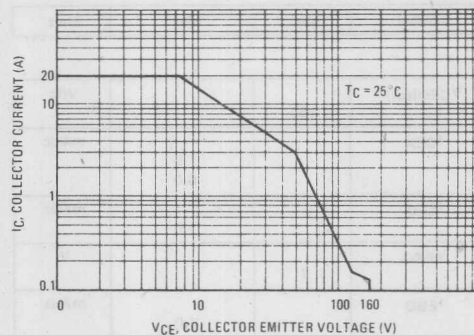
Current Gain — Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$(I_C = 15\text{ A}$, $I_{B1} = I_{B2} = 1.88\text{ A}$, $V_{CC} = 30\text{ V}$, $R_L \approx 2\Omega$)	t_{on}	1.2	μs
Storage Time		t_s	1.2	
Fall Time		t_f	0.25	

¹ Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 — "ON" VOLTAGES

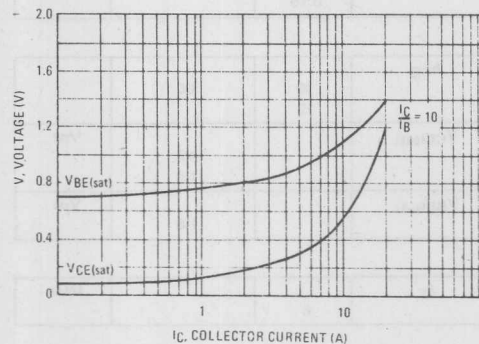


FIGURE 4 — DC CURRENT GAIN

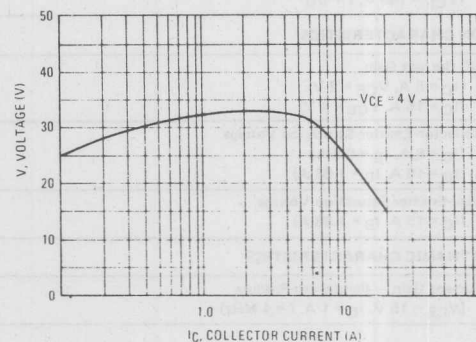


FIGURE 5 — RESISTIVE SWITCHING PERFORMANCE

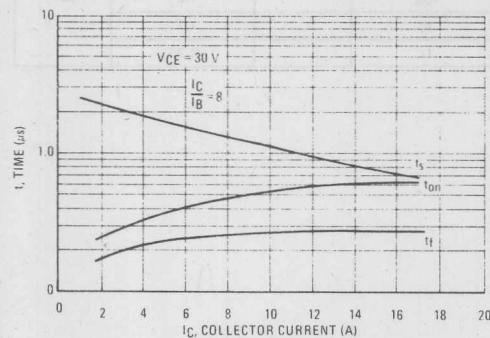
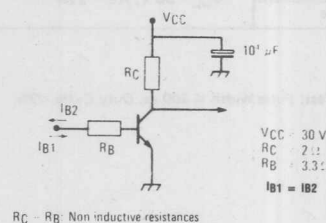


FIGURE 6 — SWITCHING TIMES TEST CIRCUIT



R_C, R_B — Non inductive resistances



MOTOROLA

BUV 12

**SWITCHMODE^Δ SERIES
NPN SILICON POWER TRANSISTOR**

... designed for high speed, high voltage, high power applications.

- High DC current gain:
HFE min. = 20 at $I_C = 5$ A
- Very fast switching times:
 T_S max. = 1.5 μ s at $I_C = 10$ A
 T_F max. = 0.5 μ s at $I_C = 10$ A

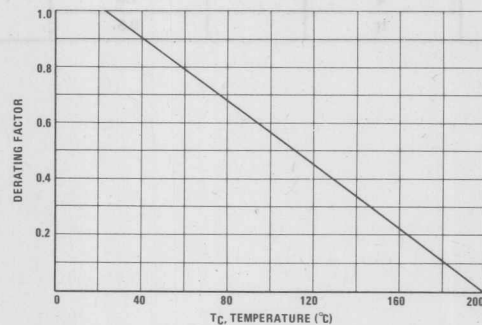
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector-Base Voltage	V_{CBO}	300	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	300	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	290	Vdc
Collector-Current — continuous	I_C	20	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	25	Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C/W}$

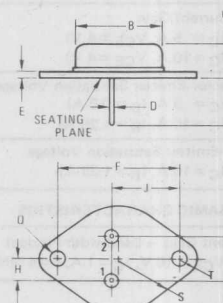
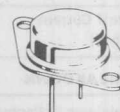
FIGURE 1 — POWER DERATING



20 AMPERES

**NPN SILICON
POWER
METAL TRANSISTOR**

**250 VOLTS
150 WATTS**



STYLE 1:
PIN 1: BASE
2: EMITTER
CASE: COLLECTOR
STYLE 2:
PIN 1: BASE
2: COLLECTOR
CASE: EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Biases: ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.5 6	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 200\text{ V}$)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	8.0 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 5\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 10\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 5\text{ A}$, $I_B = 0.5\text{ A}$) ($I_C = 10\text{ A}$, $I_B = 1.25\text{ A}$)	$V_{CE(sat)}$		1.0 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 1.25\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

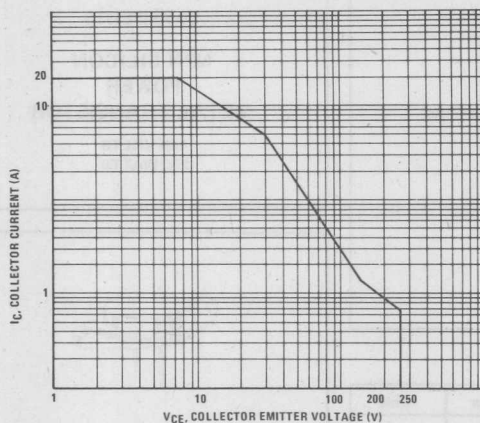
Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 10\text{ A}$, $I_{B1} = I_{B2} = 1.25\text{ A}$, ($V_{CC} = 150\text{ V}$, $R_C = 15\ \Omega$)	t_{on}	0.7	μs
Storage Time		t_s	1.5	
Fall Time		t_f	0.5	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 — "ON" VOLTAGES

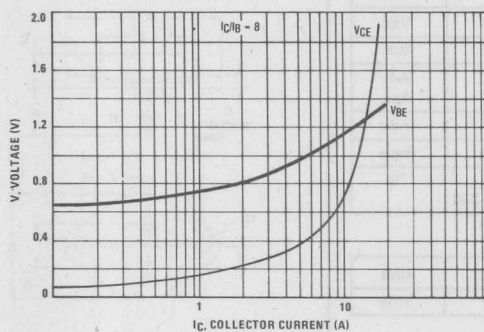


FIGURE 4 — DC CURRENT GAIN

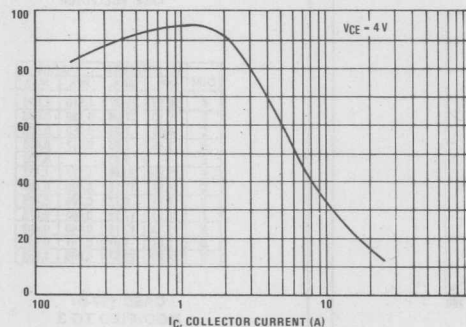


FIGURE 5 — RESISTIVE SWITCHING PERFORMANCE

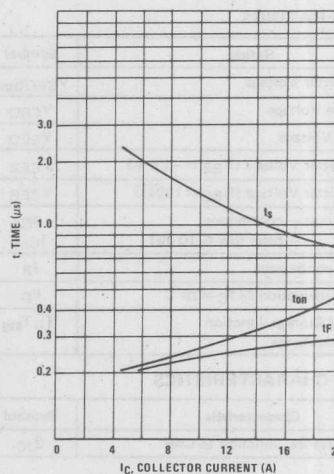
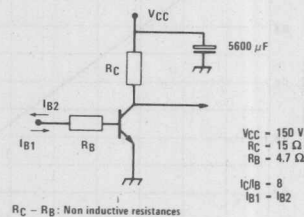


FIGURE 6 — SWITCHING TIMES TEST CIRCUIT



**MOTOROLA****BUV 20**

SWITCHMODE^Δ SERIES NPN SILICON POWER TRANSISTOR

... designed for high speed, high current, high power applications.

- High DC current gain:
HFE min. = 20 at $I_C = 25$ A
= 10 at $I_C = 50$ A
- Low $V_{CE(sat)}$:
 $V_{CE(sat)}$ max. = 0.6 V at $I_C = 25$ A
= 1.2 V at $I_C = 50$ A
- Very fast switching times:
 $T_F = 0.25 \mu s$ at $I_C = 50$ A

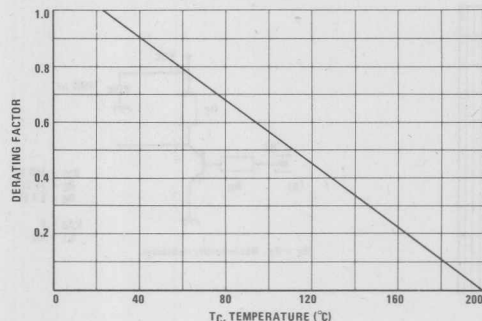
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	160	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	150	Vdc
Collector-Current — continuous	I_C	50	A dc
— peak ($p_w \leq 10$ ms)	I_{CM}	60	A pk
Base-Current continuous	I_B	10	A dc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ C/W$

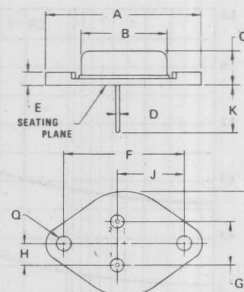
FIGURE 1 — POWER DERATING



50 AMPERES

NPN SILICON POWER METAL TRANSISTOR

125 VOLTS
250 WATTS



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Biases: ($V_{CE} = 140\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 140\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 100\text{ V}$)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 40\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	12 1.5		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 25\text{ A}$, $V_{CE} = 2\text{ V}$) ($I_C = 50\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 25\text{ A}$, $I_B = 2.5\text{ A}$) ($I_C = 50\text{ A}$, $I_B = 5\text{ A}$)	$V_{CE(sat)}$		0.6 1.2	Vdc
Base-Emitter Saturation Voltage ($I_C = 50\text{ A}$, $I_B = 5\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 50\text{ A}$, $I_{B1} = I_{B2} = 5\text{ A}$, ($V_{CC} = 30\text{ V}$, $R_C = 0.6\ \Omega$)	t_{on}	1.5	μs
Storage Time		t_s	1.2	
Fall Time		t_f	0.25	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA

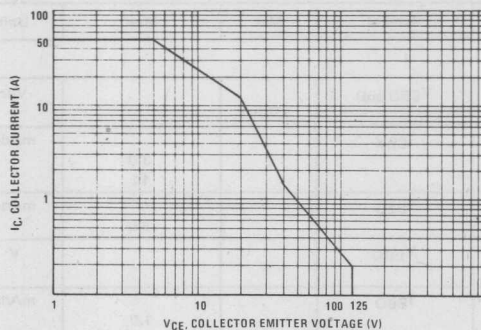


FIGURE 3 - "ON" VOLTAGES

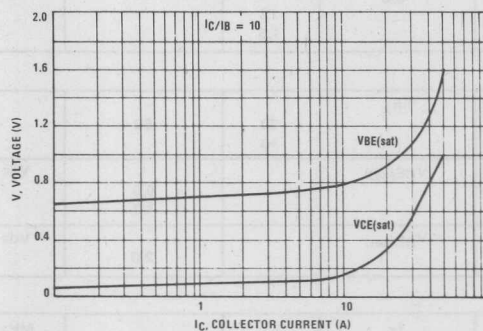
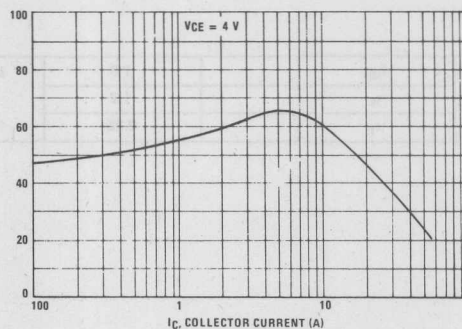


FIGURE 4 - DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 - RESISTIVE SWITCHING PERFORMANCE

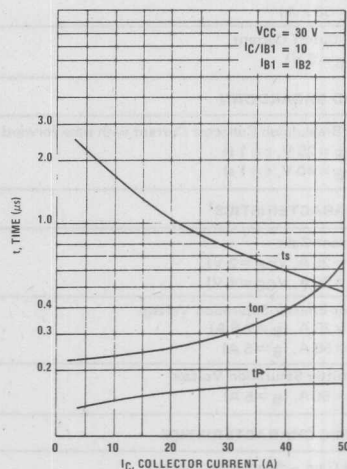
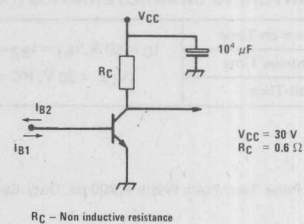


FIGURE 6 - SWITCHING TIMES TEST CIRCUIT



**MOTOROLA****BUV 21**

SWITCHMODE^Δ SERIES NPN SILICON POWER TRANSISTOR

... designed for high speed, high current, high power applications.

- High DC current gain:
HFE min. = 20 at $I_C = 12\text{ A}$
- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 0.6 V at $I_C = 8\text{ A}$
- Very fast switching times:
 T_F max. = 0.4 μs at $I_C = 25\text{ A}$

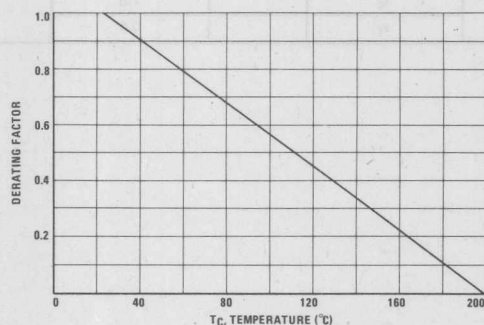
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector-Base Voltage	V_{CBO}	250	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5\text{ V}$)	V_{CEX}	250	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	240	Vdc
Collector-Current — continuous	I_C	40	Adc
— peak ($p_w \leq 10\text{ ms}$)	I_{CM}	50	Apk
Base-Current continuous	I_B	8	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C/W}$

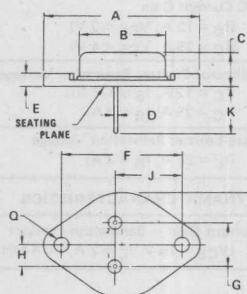
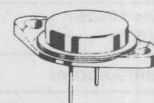
FIGURE 1 — POWER DERATING



40 AMPERES

NPN SILICON
POWER
METAL TRANSISTOR

200 VOLTS
250 WATTS



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.27	1.510	1.550
B	19.30	21.06	0.760	0.830
C	8.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.54	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.94	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Biases: ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 160\text{ V}$)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	12 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 12\text{ A}$, $V_{CE} = 2\text{ V}$) ($I_C = 25\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 1.2\text{ A}$) ($I_C = 25\text{ A}$, $I_B = 3\text{ A}$)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 25\text{ A}$, $I_B = 3\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

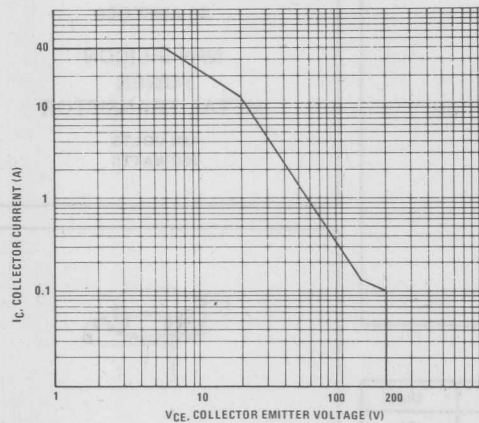
Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 25\text{ A}$, $I_{B1} = I_{B2} = 3\text{ A}$, ($V_{CC} = 100\text{ V}$, $R_C = 4\ \Omega$)	t_{on}	1.0	μs
Storage Time		t_s	1.8	
Fall Time		t_f	0.4	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 - "ON" VOLTAGES

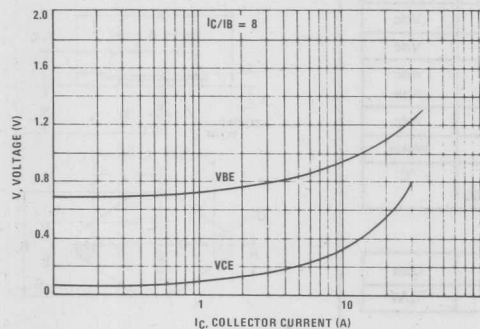


FIGURE 4 - DC CURRENT GAIN

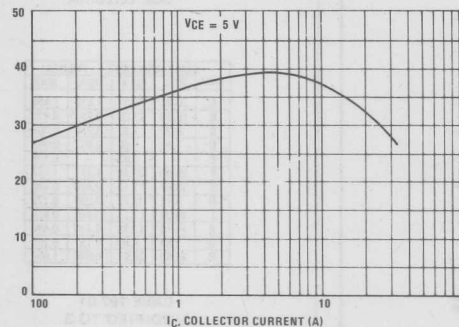


FIGURE 5 - RESISTIVE SWITCHING PERFORMANCE

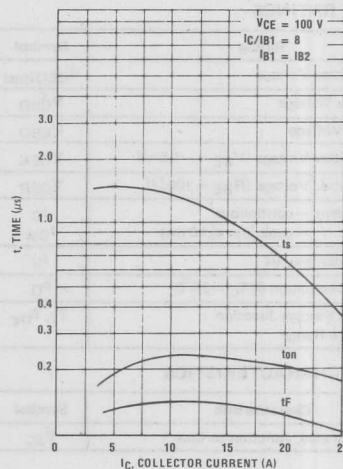
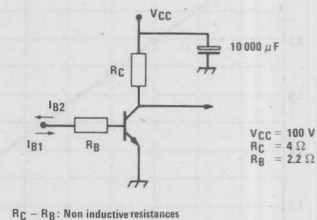


FIGURE 6 - SWITCHING TIMES TEST CIRCUIT



**MOTOROLA****BUV 21N**

**SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTOR**

... designed for high speed, high current, high power and low cost applications.

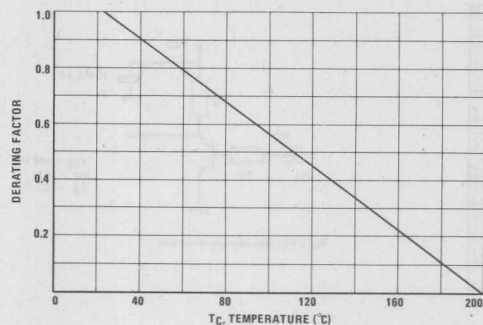
- High DC current gain: HFE min. = 15 at $I_C = 20$ A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$ max. = 1.0 V at $I_C = 20$ A
= 1.8 V at $I_C = 40$ A
- Very fast switching times:
 T_F max. = $0.2 \mu s$ at $I_C = 40$ A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	160	Vdc
Collector-Base Voltage	V_{CBO}	220	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	220	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	200	Vdc
Collector-Current — continuous	I_C	40	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	50	Apk
Base-Current continuous	I_B	10	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

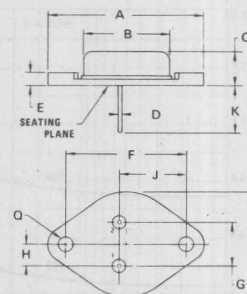
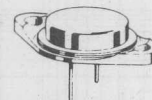
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ C/W$

FIGURE 1 — POWER DERATING**40 AMPERES**

**NPN SILICON
POWER
METAL TRANSISTOR**

**160 VOLTS
250 WATTS**



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CEO(sus)}$	160		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 130\text{ V}$)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 25\text{ V}$, $t = 0.5\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 0.5\text{ s}$)	$I_{S/b}$	10 0.3		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 20\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 40\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 10	60	
Collector-Emitter Saturation Voltage ($I_C = 20\text{ A}$, $I_B = 2\text{ A}$) ($I_C = 40\text{ A}$, $I_B = 5\text{ A}$)	$V_{CE(sat)}$		1.0 1.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 40\text{ A}$, $I_B = 5\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 40\text{ A}$, $I_{B1} = I_{B2} = 5\text{ A}$, ($V_{CC} = 30\text{ V}$, $R_C = 0.75\ \Omega$)	t_{on}	1.2	μs
Storage Time		t_s	1.0	
Fall Time		t_f	0.2	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

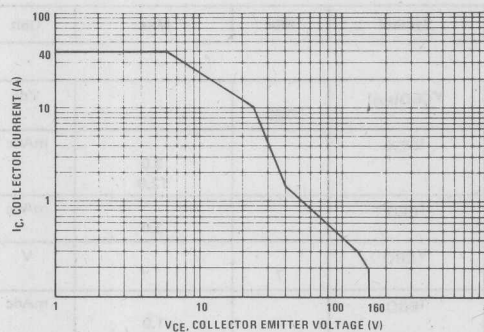


FIGURE 3 – "ON" VOLTAGES

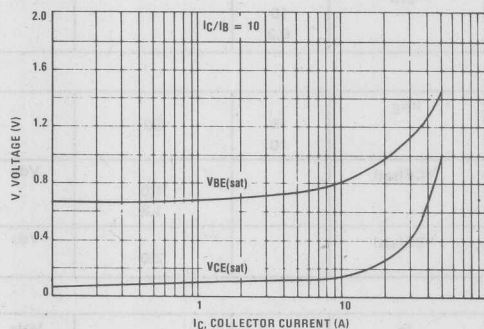
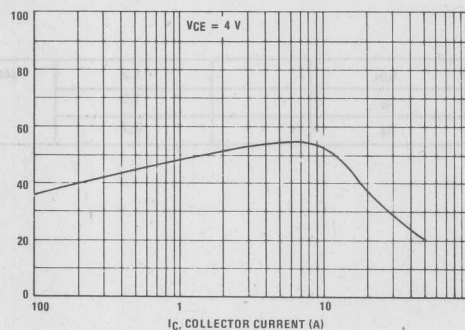


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$, $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

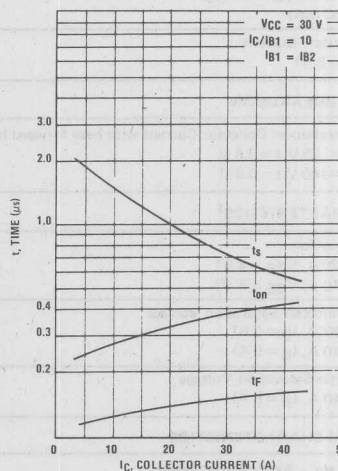
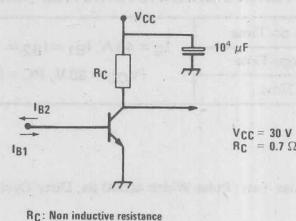


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



**MOTOROLA****BUV 22**

SWITCHMODE^Δ SERIES NPN SILICON POWER TRANSISTOR

... designed for high current, high speed, high power applications.

- High DC current gain: HFE min. = 20 at $I_C = 10$ A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$ max. = 1.0 V at $I_C = 10$ A
- Very fast switching times:
 T_F max. = 0.35 μ s at $I_C = 20$ A

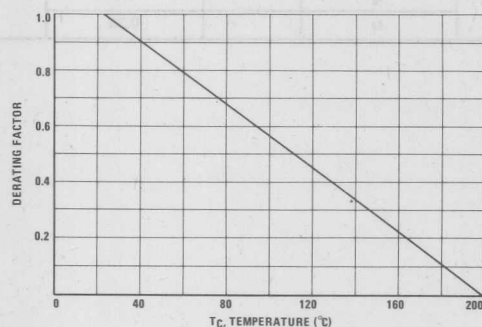
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	300	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	300	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	290	Vdc
Collector-Current — continuous	I_C	40	A dc
— peak ($p_w \leq 10$ ms)	I_{CM}	50	A pk
Base-Current continuous	I_B	8	A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C/W}$

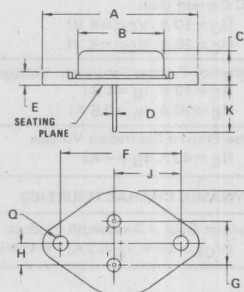
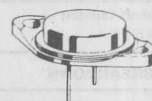
FIGURE 1 — POWER DERATING



40 AMPERES

NPN SILICON
POWER
METAL TRANSISTOR

250 VOLTS
250 WATTS



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.54	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.08	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 200\text{ V}$)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	12 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 10\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 20\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 1\text{ A}$) ($I_C = 20\text{ A}$, $I_B = 2.5\text{ A}$)	$V_{CE(sat)}$		1.0 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 40\text{ A}$, $I_B = 4\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

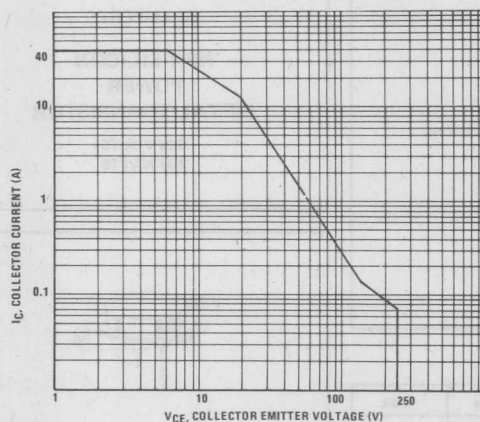
Current Gain — Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 20\text{ A}$, $I_{B1} = I_{B2} = 2.5\text{ A}$, ($V_{CC} = 100\text{ V}$, $R_C = 5\ \Omega$)	t_{on}	0.8	μs
Storage Time		t_s	1.1	
Fall Time		t_f	0.35	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 - "ON" VOLTAGES

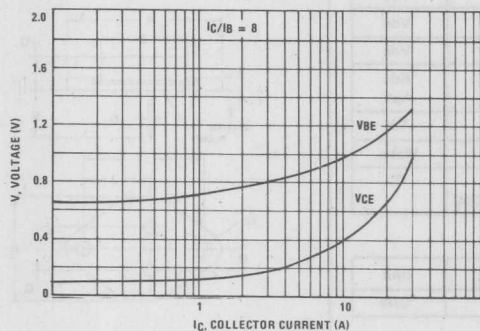


FIGURE 4 - DC CURRENT GAIN

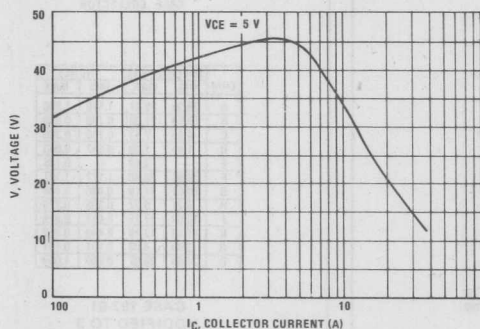


FIGURE 5 - RESISTIVE SWITCHING PERFORMANCE

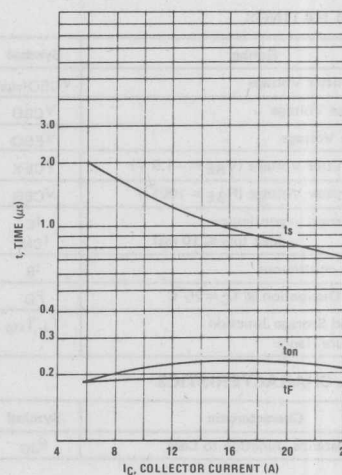
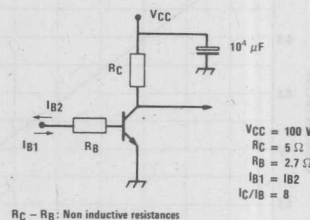


FIGURE 6 - SWITCHING TIMES TEST CIRCUIT



**MOTOROLA****BUV 23**

SWITCHMODE[▲] SERIES NPN SILICON POWER TRANSISTOR

... designed for high current, high speed, high power applications.

- High DC current gain: HFE min. = 15 at $I_C = 8$ A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 0.8 V at $I_C = 8$ A
- Very fast switching times:
 $T_F = 0.4 \mu s$ at $I_C = 16$ A

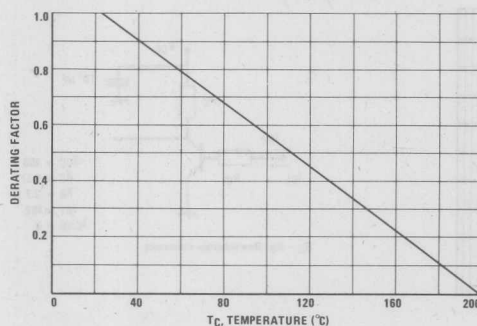
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	325	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	400	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	390	Vdc
Collector-Current — continuous	I_C	30	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	40	Apk
Base-Current continuous	I_B	6	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ C/W$

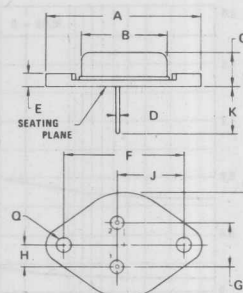
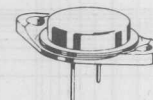
FIGURE 1 — POWER DERATING



30 AMPERES

NPN SILICON POWER METAL TRANSISTOR

325 VOLTS
250 WATTS



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	325		Vdc
Collector Cutoff Current at Reverse Biases: ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 260\text{ V}$)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	12 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 8\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 16\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 1.6\text{ A}$) ($I_C = 16\text{ A}$, $I_B = 3.2\text{ A}$)	$V_{CE(sat)}$		0.8 1.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 16\text{ A}$, $I_B = 3.2\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

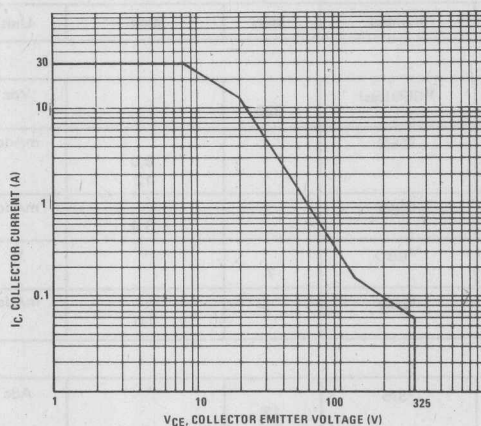
Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 16\text{ A}$, $I_{B1} = I_{B2} = 3.2\text{ A}$, ($V_{CC} = 100\text{ V}$, $R_C = 6.25\ \Omega$)	t_{on}	0.8	μs
Storage Time		t_s	1.8	
Fall Time		t_f	0.4	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

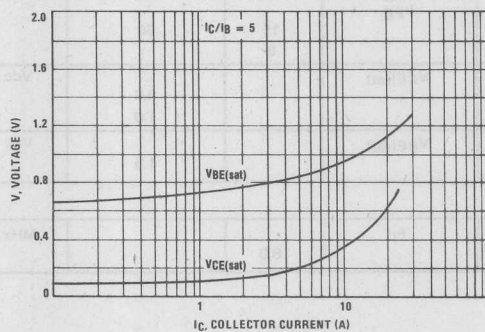


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

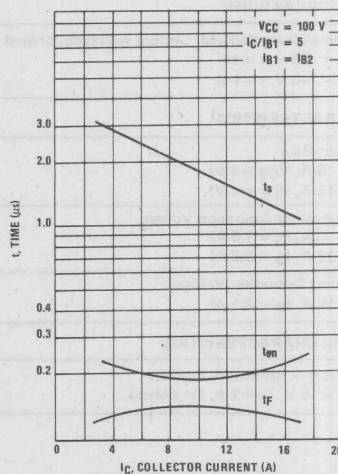


FIGURE 4 – DC CURRENT GAIN

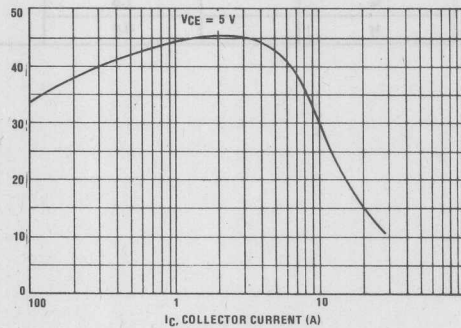
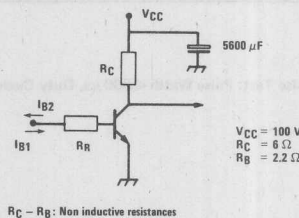


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT





MOTOROLA

BUV 24

SWITCHMODE^Δ SERIES NPN SILICON POWER TRANSISTOR

... designed for high current, high speed, high power applications.

- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 1.0 V at $I_C = 12$ A
- Very fast switching times:
 T_F max. = 0.9 μ s at $I_C = 12$ A

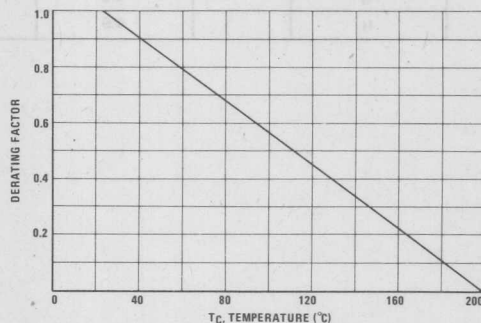
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Base Voltage	V_{CBO}	450	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	450	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	440	Vdc
Collector-Current — continuous	I_C	20	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	30	Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C/W}$

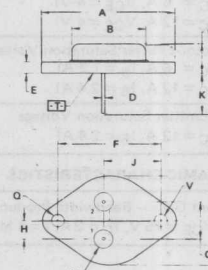
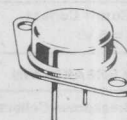
FIGURE 1 — POWER DERATING



20 AMPERES

NPN SILICON
POWER
METAL TRANSISTOR

400 VOLTS
250 WATTS



NOTES

1. DIMENSIONS D AND V ARE DATUMS
 2. T IS SEATING PLANE AND DATUM
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D
- FOR LEADS
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37	1.550		
B	21.08	0.830		
C	6.35	0.250		
D	0.97	0.038		
E	3.43	0.135		
F	30.15 BSC	1.187 BSC		
G	10.92 BSC	0.430 BSC		
H	9.46 BSC	0.371 BSC		
J	16.89 BSC	0.665 BSC		
K	11.18	0.440		
O	3.81	0.150		
R	26.67	1.050		
U	4.83	0.190		
V	3.81	0.150		

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	400		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 450\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 450\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 320\text{ V}$)	I_{CEO}		30	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	12 0.15		Adc
ON CHARACTERISTICS¹				
DC Current Gain ($I_C = 6\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 12\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage ($I_C = 6\text{ A}$, $I_B = 1.2\text{ A}$) ($I_C = 12\text{ A}$, $I_B = 2.4\text{ A}$)	$V_{CE(sat)}$		0.6 1.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 2.4\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 12\text{ A}$, $I_{B1} = I_{B2} = 2.4\text{ A}$, ($V_{CC} = 120\text{ V}$, $RC = 8.3\ \Omega$)	t_{on}		1.6	μs
Storage Time		t_s		3.0	
Fall Time		t_f		0.9	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA

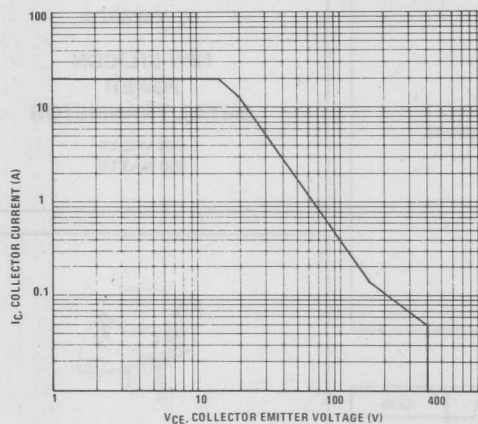


FIGURE 3 - "ON" VOLTAGES

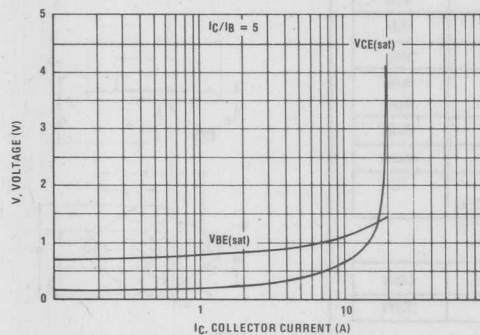
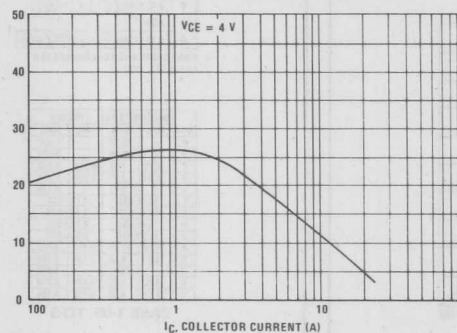


FIGURE 4 - DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$, $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 - RESISTIVE SWITCHING PERFORMANCE

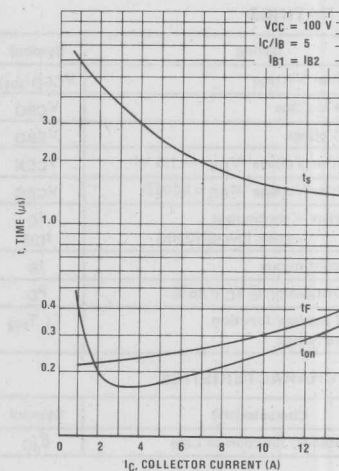
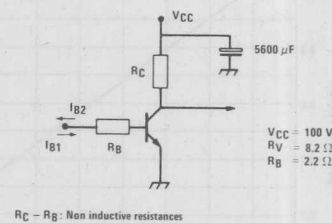


FIGURE 6 - SWITCHING TIMES TEST CIRCUIT



**MOTOROLA****BUV 25**

**SWITCHMODE^Δ SERIES
NPN SILICON POWER TRANSISTOR**

... designed for high current, high speed, high power applications.

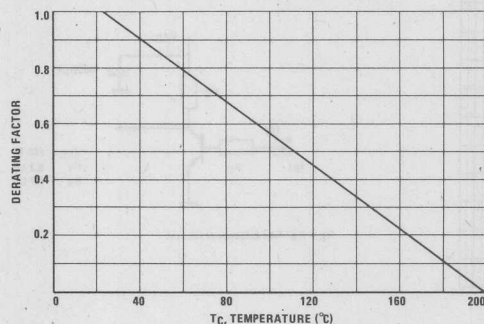
- Low $V_{CE(sat)}$: $V_{CE(sat)} \text{ max.} = 1 \text{ V}$ at $I_C = 8 \text{ A}$
- Very fast switching times:
 $T_F \text{ max.} = 1.0 \mu\text{s}$ at $I_C = 8 \text{ A}$

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector-Base Voltage	V_{CBO}	500	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5 \text{ V}$)	V_{CEX}	500	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	500	Vdc
Collector-Current — continuous	I_C	15	Adc
— peak ($p_w \leq 10 \text{ ms}$)	I_{CM}	20	Apk
Base-Current continuous	I_B	3	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

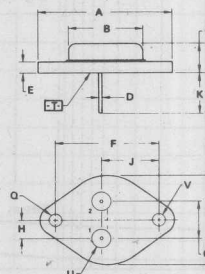
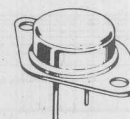
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C/W}$

FIGURE 1 — POWER DERATING**15 AMPERES**

**NPN SILICON
POWER
METAL TRANSISTOR**

**500 VOLTS
250 WATTS**



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
 2. \square IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE ϕ .
- FOR LEADS:
- ϕ ± 0.13 (0.005) \ominus T V \ominus
- ϕ ± 0.13 (0.005) \ominus T V \ominus Q \ominus
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.06	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	—	2.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$) $L = 25\text{ mH}$	$V_{CEO(sus)}$	500		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 500\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 500\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 400\text{ V}$)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	12 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 4\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 8\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage ($I_C = 4\text{ A}$, $I_B = 0.8\text{ A}$) ($I_C = 8\text{ A}$, $I_B = 1.6\text{ A}$)	$V_{CE(sat)}$		0.6 1.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 1.6\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 8\text{ A}$, $I_{B1} = I_{B2} = 1.6\text{ A}$, ($V_{CC} = 100\text{ V}$, $R_C = 12.5\ \Omega$)	t_{on}	1.8	μs
Storage Time		t_s	4.0	
Fall Time		t_f	1.0	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

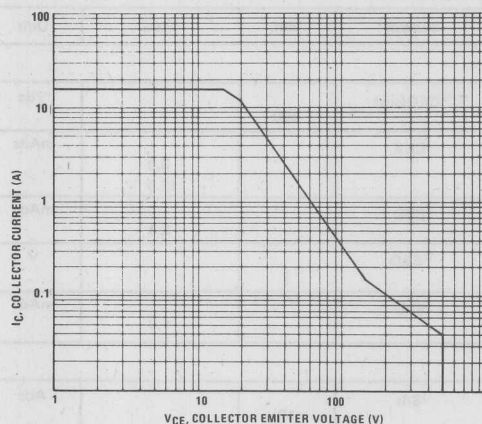


FIGURE 3 – "ON" VOLTAGES

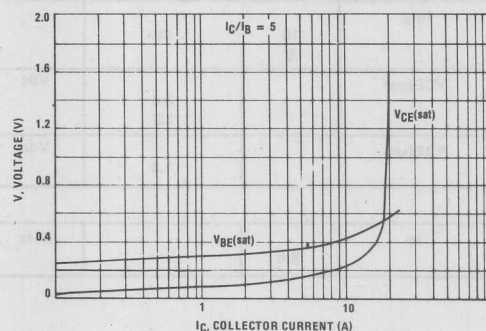
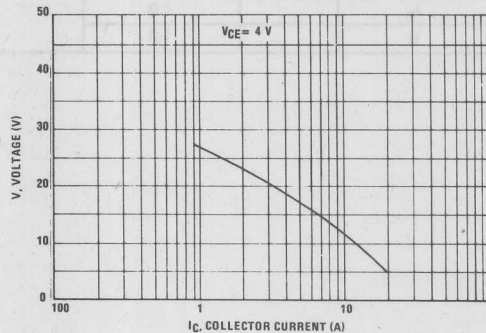


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

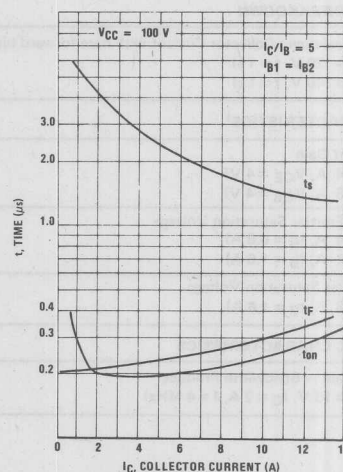
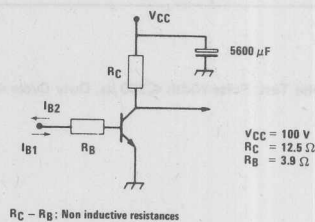


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



**MOTOROLA****BUX 13**

SWITCHMODE[▲] SERIES NPN SILICON POWER TRANSISTOR

... designed for high speed, high voltage, high power applications.

- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 1.5 V at $I_C = 8$ A
- Very fast switching times:
 T_F max. = 0.8 μ s at $I_C = 8$ A

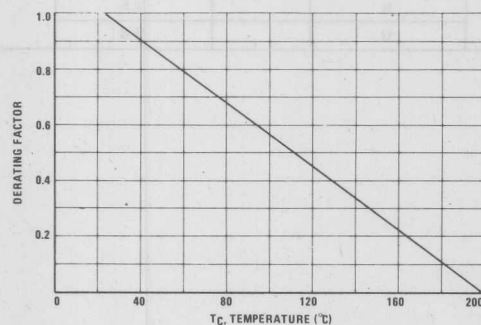
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	325	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	400	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	390	Vdc
Collector-Current — continuous	I_C	15	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	20	Apk
Base-Current continuous	I_B	3	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C/W}$

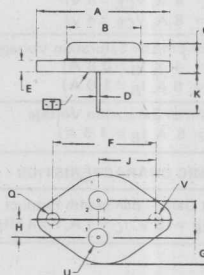
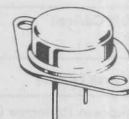
FIGURE 1 — POWER DERATING



15 AMPERES

NPN SILICON POWER METAL TRANSISTOR

325 VOLTS
150 WATTS



NOTES

1. DIMENSIONS D AND V ARE DATUMS
2. \square IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D.

$\varnothing \pm .13$ (0.005) \varnothing T V \varnothing

FOR LEADS

$\varnothing \pm .13$ (0.005) \varnothing T V \varnothing \varnothing

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37	1.550		
B	21.08	0.830		
C	6.35	0.250	0.300	
D	0.93	0.038	0.043	
E	3.43	0.135		
F	30.15 BSC	1.187 BSC		
G	10.92 BSC	0.430 BSC		
H	5.46 BSC	0.215 BSC		
J	16.89 BSC	0.665 BSC		
K	11.18	0.440	0.480	
Q	3.81	0.150	0.165	
R	26.67	1.050		
U	4.83	0.190	0.210	
V	3.81	0.150	0.165	

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	325		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.5 6.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 260\text{ V}$)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	5 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 4\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 8\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage ($I_C = 4\text{ A}$, $I_B = 0.8\text{ A}$) ($I_C = 8\text{ A}$, $I_B = 1.6\text{ A}$)	$V_{CE(sat)}$		0.8 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 1.6\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain - Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 8\text{ A}$, $I_{B1} = I_{B2} = 1.6\text{ A}$, ($V_{CC} = 150\text{ V}$, $RC = 18.7\ \Omega$)	t_{on}	1.2	μs
Storage Time		t_s	2.5	
Fall Time		t_f	0.8	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA

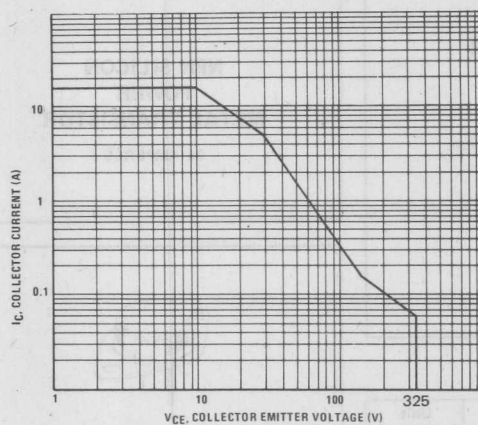


FIGURE 3 - "ON" VOLTAGES

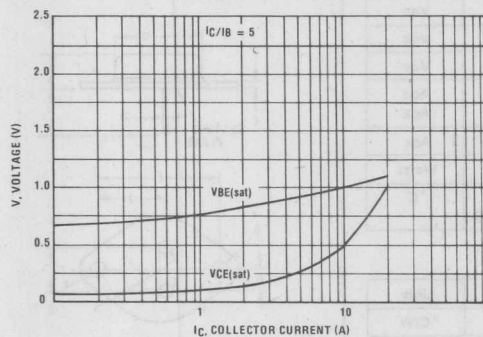
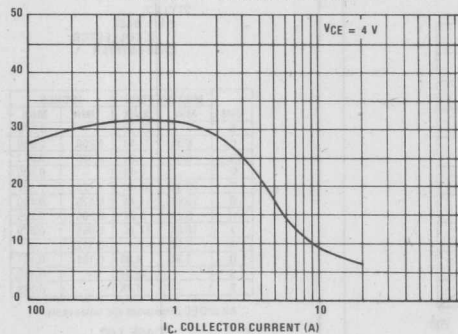


FIGURE 4 - DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 - RESISTIVE SWITCHING PERFORMANCE

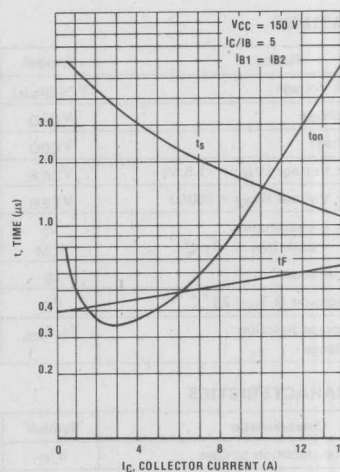
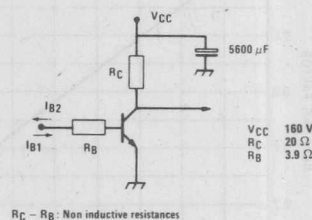


FIGURE 6 - SWITCHING TIMES TEST CIRCUIT



**MOTOROLA****BUX39****NPN SILICON POWER METAL TRANSISTOR**

... designed for high speed, high current, high power application.

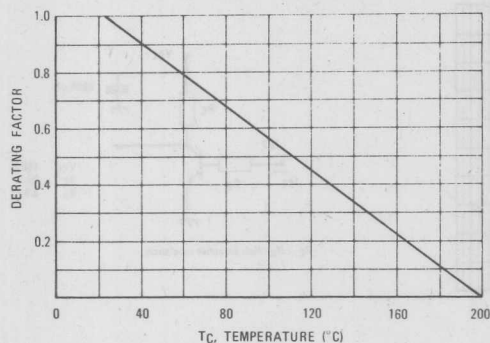
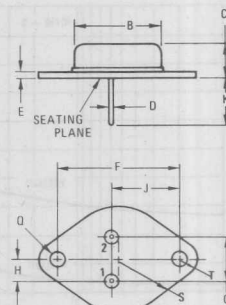
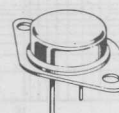
- High current gain — bandwidth product F_t min. = 8.0 MHz
 - High DC current gain H_{FE} min. 15 @ $I_C = 12$ A.
- Very fast switching times
 t_f max. = 0.25 μ s @ $I_C = 20$ A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	90	Vdc
Collector-Base Voltage	V_{CBO}	120	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	120	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	110	Vdc
Collector-Current — continuous	I_C	30	Adc
— peak (pw ≤ 10 ms)	I_{CM}	40	Apk
Base-Current continuous	I_B	6	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ\text{C/W}$

FIGURE 1 — POWER DERATING**NPN SILICON POWER METAL TRANSISTOR****30 AMPERES**

STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE-COLLECTOR

STYLE 2:
 PIN 1. BASE
 2. COLLECTOR
 CASE-EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	90		Vdc
Collector-Emitter Cutoff Current at Reverse Bias Voltage ($V_{CE} = 120\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 120\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)			1 5	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 70\text{ V}$)	I_{CEO}		1	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 45\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	1 4		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 12\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 20\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 1.2\text{ A}$) ($I_C = 20\text{ A}$, $I_B = 2.5\text{ A}$)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 20\text{ A}$, $I_B = 2.5\text{ A}$)	$V_{BE(sat)}$		2.5	Vdc

DYNAMIC CHARACTERISTICS

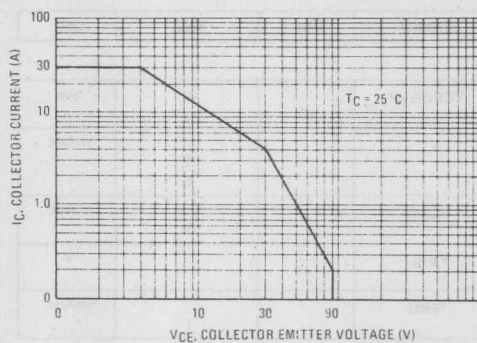
Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 20\text{ A}$, $I_{B1} = I_{B2} = 2.5\text{ A}$, $V_{CE} = 30\text{ V}$, $RC = 1.5\Omega$	t_{on}	1.2	μs
Storage Time		t_s	1.0	
Fall Time		t_f	0.25	

¹ Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

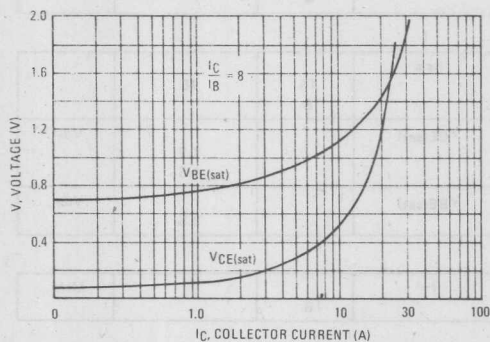


FIGURE 4 – DC CURRENT GAIN

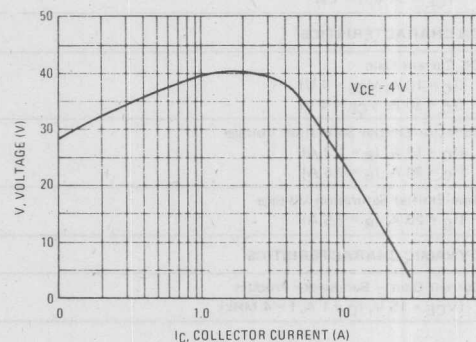


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

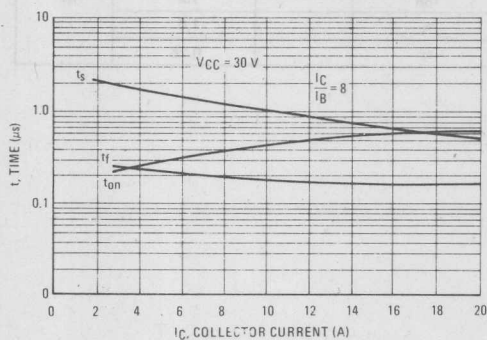
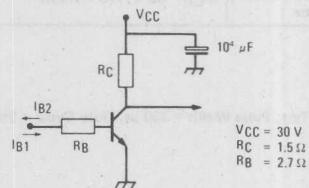


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



$R_C - R_B$: Non inductive resistances

**SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTOR**

... designed for high speed, high current, high power applications.

- High D.C. current gain:
HFE min.: 15 at $I_C = 10$ A
- Very fast switching times:
 T_F max. = 0.25 μ s at $I_C = 15$ A

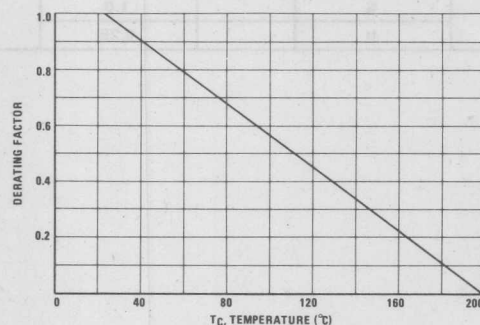
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	160	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	150	Vdc
Collector-Current — continuous	I_C	20	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	28	Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ\text{C/W}$

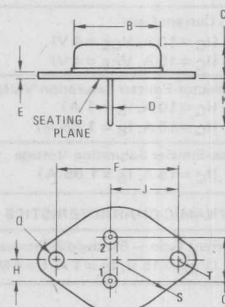
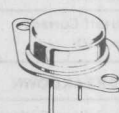
FIGURE 1 — POWER DERATING



20 AMPERES

**NPN SILICON
POWER
METAL TRANSISTOR**

**125 VOLTS
120 WATTS**



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 160\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 160\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 100\text{ V}$)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 50\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	4.0 1.0		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 10\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 15\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 1\text{ A}$) ($I_C = 15\text{ A}$, $I_B = 1.88\text{ A}$)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 15\text{ A}$, $I_B = 1.88\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 15\text{ A}$, $I_{B1} = I_{B2} = 1.88\text{ A}$, ($V_{CC} = 30\text{ V}$, $R_C = 2\ \Omega$)	t_{on}	1.2	μs
Storage Time		t_s	1.0	
Fall Time		t_f	0.25	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA

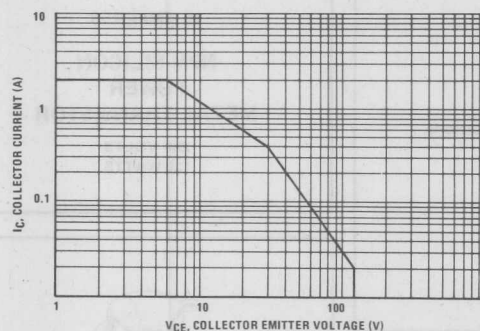


FIGURE 3 - "ON" VOLTAGES

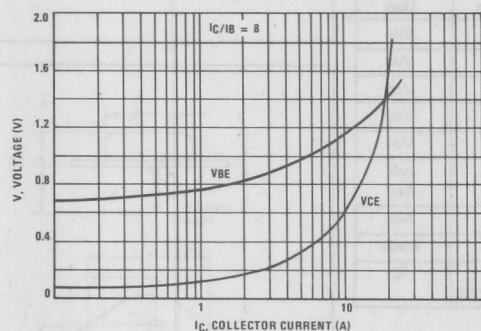


FIGURE 4 - DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 - RESISTIVE SWITCHING PERFORMANCE

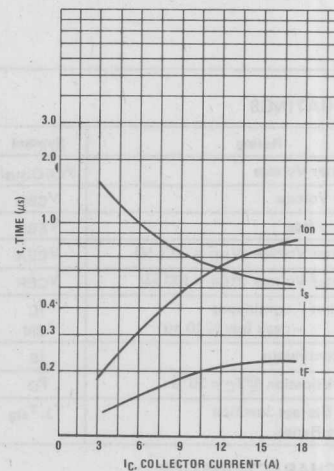
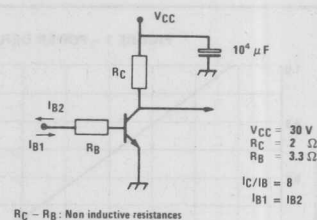


FIGURE 6 - SWITCHING TIMES TEST CIRCUIT





MOTOROLA

BUX 41

SWITCHMODE[®] SERIES NPN SILICON POWER TRANSISTOR

... designed for high speed, high current, high power applications.

- Very fast switching times:
 $T_F \text{ max.} = 0.4 \mu\text{s at } I_C = 8 \text{ A}$

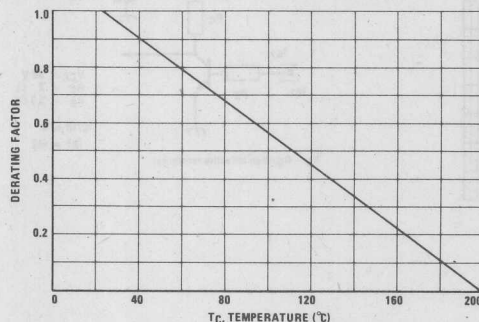
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector-Base Voltage	V_{CBO}	250	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5 \text{ V}$)	V_{CEX}	250	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	240	Vdc
Collector-Current — continuous	I_C	15	Adc
— peak ($p_w \leq 10 \text{ ms}$)	I_{CM}	20	Apk
Base-Current continuous	I_B	3	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ\text{C/W}$

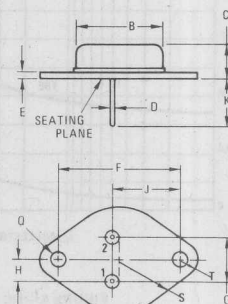
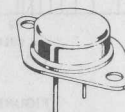
FIGURE 1 — POWER DERATING



15 AMPERES

NPN SILICON POWER METAL TRANSISTOR

200 VOLTS
120 WATTS



STYLE 1:
PIN 1. BASE
PIN 2. EMITTER
CASE-COLLECTOR
STYLE 2:
PIN 1. BASE
PIN 2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Biases: ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 160\text{ V}$)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 135\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	4.0 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 5\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 8\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 5\text{ A}$, $I_B = 0.5\text{ A}$) ($I_C = 8\text{ A}$, $I_B = 1\text{ A}$)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 1\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 8\text{ A}$, $I_{B1} = I_{B2} = 1\text{ A}$, ($V_{CC} = 150\text{ V}$, $R_C = 18.75\ \Omega$)	t_{on}	0.6	μs
Storage Time		t_s	1.5	
Fall Time		t_f	0.4	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

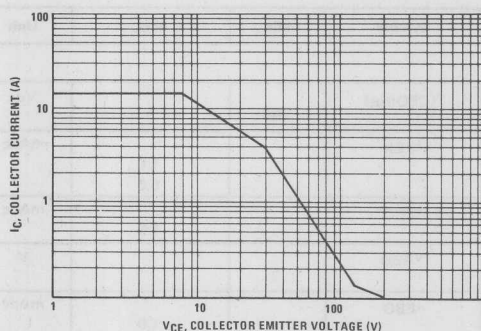


FIGURE 3 – "ON" VOLTAGES

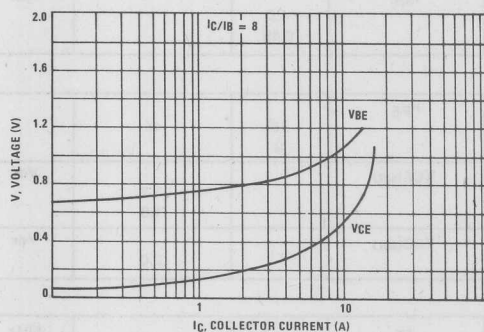
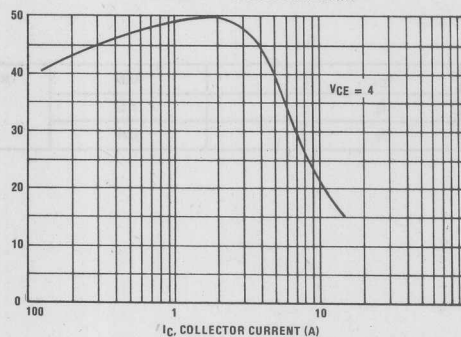


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

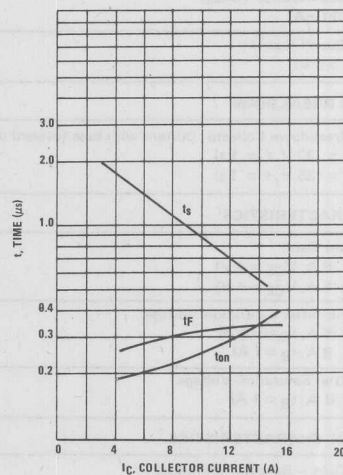
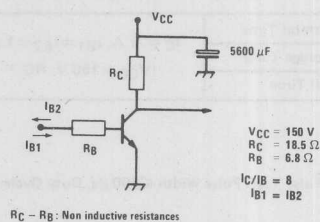


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



**MOTOROLA****BUX 41N**

**SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTOR**

... designed for high speed, high current, high power applications.

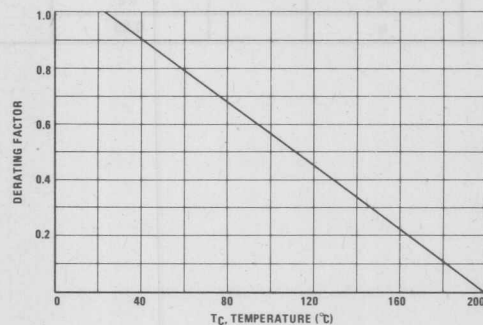
- High DC current gain:
HFE min. = 15 at $I_C = 8$ A
- Very fast switching times:
 T_F max. = $0.25 \mu s$ at $I_C = 12$ A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	160	Vdc
Collector-Base Voltage	V_{CBO}	220	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	220	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	200	Vdc
Collector-Current — continuous	I_C	18	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	25	Apk
Base-Current continuous	I_B	3.6	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

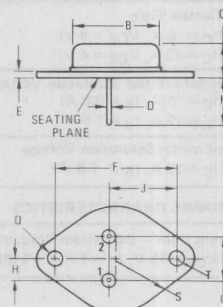
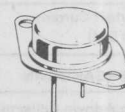
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ C/W$

FIGURE 1 — POWER DERATING**18 AMPERES**

**NPN SILICON
POWER
METAL TRANSISTOR**

**160 VOLTS
120 WATTS**



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	160		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 130\text{ V}$)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 100\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	4 0.27		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 8\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 12\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 0.8\text{ A}$) ($I_C = 12\text{ A}$, $I_B = 1.5\text{ A}$)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 1.5\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
--	-------	-----	--	-----

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 12\text{ A}$, $I_{B1} = I_{B2} = 1.5\text{ A}$, ($V_{CC} = 30\text{ V}$, $R_C = 2.5\ \Omega$)	t_{on}	1.2	μs
Storage Time		t_s	1.2	
Fall Time		t_f	0.25	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA

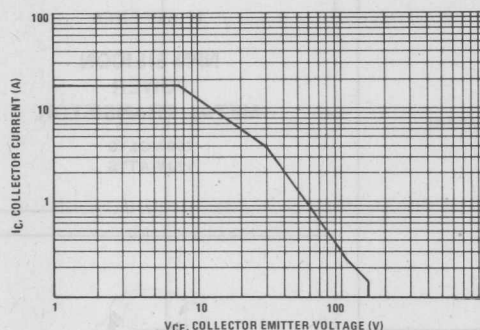


FIGURE 3 - "ON" VOLTAGES

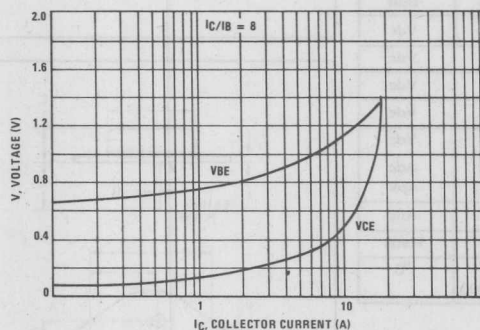
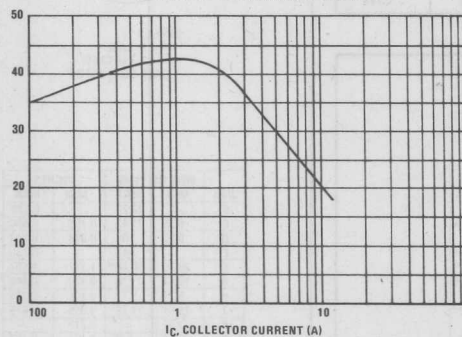


FIGURE 4 - DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 - RESISTIVE SWITCHING PERFORMANCE

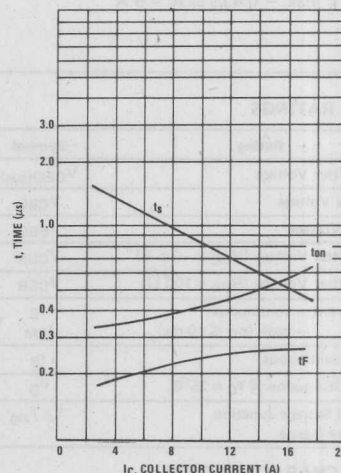
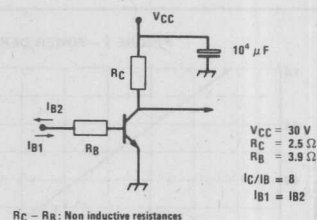


FIGURE 6 - SWITCHING TIMES TEST CIRCUIT





MOTOROLA

BUX 42

**SWITCHMODE^Δ SERIES
NPN SILICON POWER TRANSISTOR**

... designed for high speed, high voltage, high power applications.

- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 1.2 V at $I_C = 4$ A
- Very fast switching times:
 T_F max. = 0.4 μ s at $I_C = 6$ A

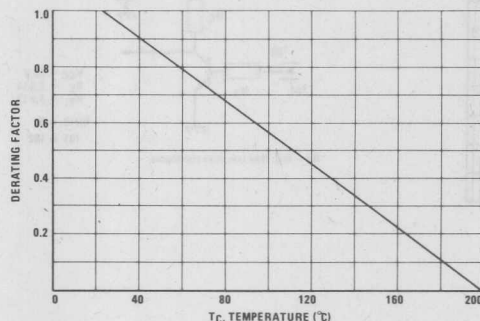
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	250	Vdc
Collector-Base Voltage	V_{CBO}	300	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	300	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	290	Vdc
Collector-Current — continuous	I_C	12	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	15	Apk
Base-Current continuous	I_B	2.4	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ\text{C/W}$

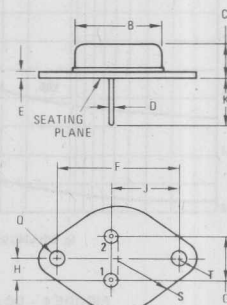
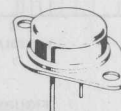
FIGURE 1 — POWER DERATING



12 AMPERES

**NPN SILICON
POWER
METAL TRANSISTOR**

**250 VOLTS
120 WATTS**



STYLE 1:
PIN 1: BASE
PIN 2: EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Biases: ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 200\text{ V}$)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 135\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	4.0 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 4\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 6\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 4\text{ A}$, $I_B = 0.4\text{ A}$) ($I_C = 6\text{ A}$, $I_B = 0.75\text{ A}$)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 6\text{ A}$, $I_B = 0.75\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

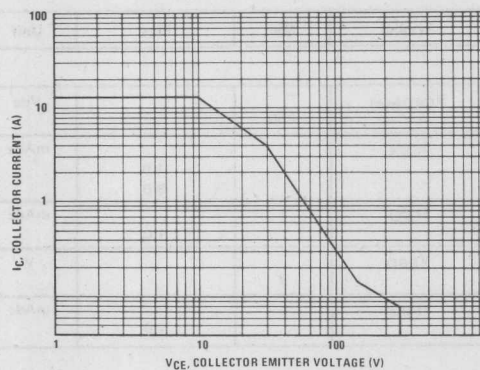
Current Gain — Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 6\text{ A}$, $I_{B1} = I_{B2} = 0.75\text{ A}$, ($V_{CC} = 150\text{ V}$, $R_C = 25\ \Omega$)	t_{on}	0.6	μs
Storage Time		t_s	2.0	
Fall Time		t_f	0.4	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 - "ON" VOLTAGES

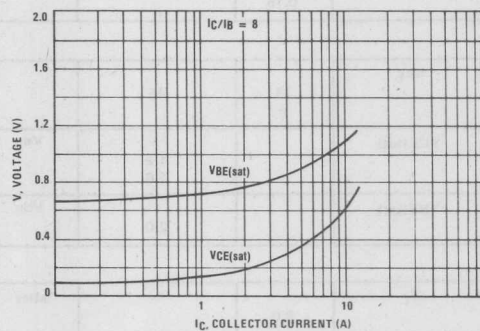


FIGURE 4 - DC CURRENT GAIN

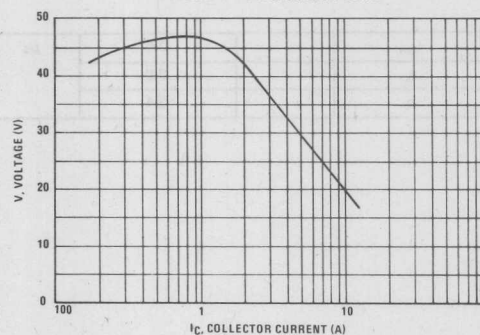


FIGURE 5 - RESISTIVE SWITCHING PERFORMANCE

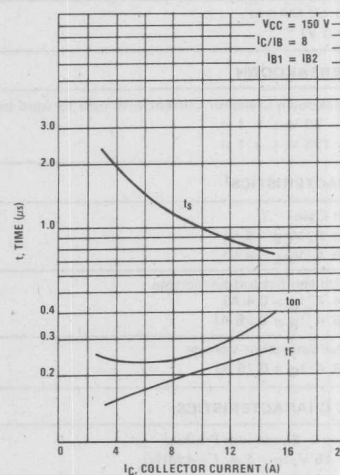
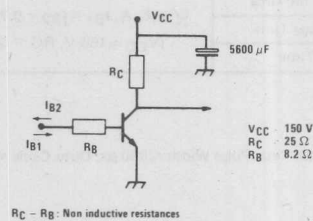


FIGURE 6 - SWITCHING TIMES TEST CIRCUIT





MOTOROLA

BUX 43

**SWITCHMODE^Δ SERIES
NPN SILICON POWER TRANSISTOR**

... designed for high speed, high voltage, high power applications.

- $V_{CE(sat)}$ max. = 1.6 V at $I_C = 6$ A
- Very fast switching times:
 T_F max. = 0.90 μ s at $I_C = 5$ A

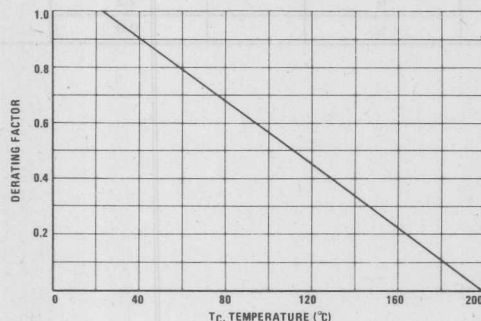
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	325	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	400	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	360	Vdc
Collector-Current — continuous	I_C	10	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	12	Apk
Base-Current continuous	I_B	2	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ\text{C/W}$

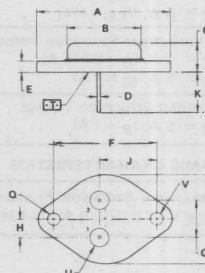
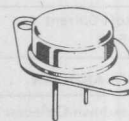
FIGURE 1 — POWER DERATING



10 AMPERES

**NPN SILICON
POWER
METAL TRANSISTOR**

**325 VOLTS
120 WATTS**



- NOTES
1. DIMENSIONS Q AND V ARE DATUMS
 2. \square IS SEATING PLANE AND DATUM
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
- FOR LEADS:
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.37	1.00	0.015	0.040
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	325		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.0 5.0	mA _{dc}
Collector-Emitter Cutoff Current ($V_{CE} = 260\text{ V}$)	I_{CEO}		1.0	mA _{dc}
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mA _{dc}

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 135\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	4.0 0.15		A _{dc}
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 3\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 5\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage ($I_C = 3\text{ A}$, $I_B = 0.375\text{ A}$) ($I_C = 5\text{ A}$, $I_B = 1\text{ A}$)	$V_{CE(sat)}$		1.0 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 5\text{ A}$, $I_B = 1\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 5\text{ A}$, $I_{B1} = I_{B2} = 1\text{ A}$, ($V_{CC} = 150\text{ V}$, $R_C = 30\ \Omega$)	t_{on}	1.0	μs
Storage Time		t_s	2.2	
Fall Time		t_f	0.9	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA

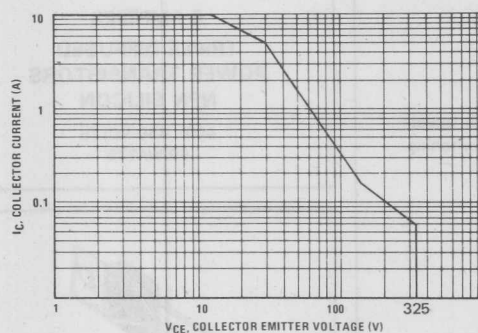


FIGURE 3 — "ON" VOLTAGES

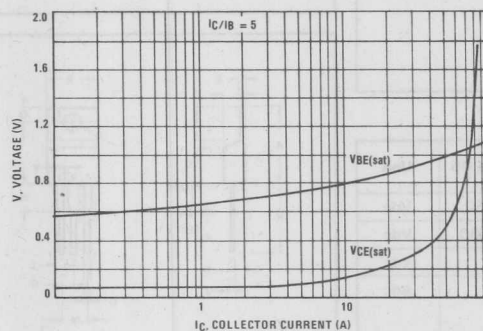
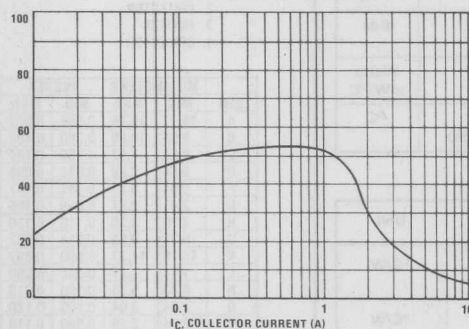


FIGURE 4 — DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$, $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 — RESISTIVE SWITCHING PERFORMANCE

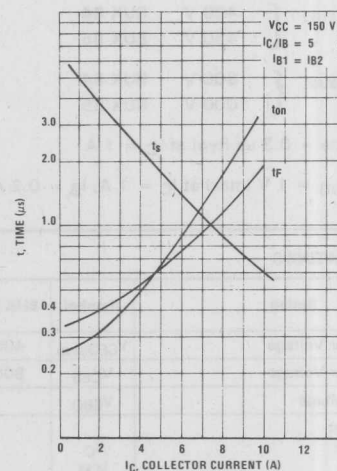
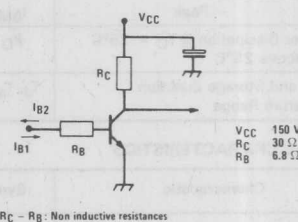


FIGURE 6 — SWITCHING TIMES TEST CIRCUIT





MOTOROLA

**BUX 84
BUX 85**

**SWITCHMODE
NPN SILICON POWER TRANSISTORS**

The BUX 84/85 are designed for high voltage, high speed power switching applications like converters, inverters, switching regulators, motor control systems.

SPECIFICATIONS FEATURES:

- $V_{CE(sus)}$ $\left\{ \begin{array}{ll} 400 \text{ V} & \text{BUX 84} \\ 450 \text{ V} & \text{BUX 85} \end{array} \right.$
- $V_{CES(sus)}$ $\left\{ \begin{array}{ll} 800 \text{ V} & \text{BUX 84} \\ 1000 \text{ V} & \text{BUX 85} \end{array} \right.$
- Fall time = 0.3 us (typ) at $I_C = 1 \text{ A}$
- $V_{CE(sat)} = 1 \text{ V (max)}$ at $I_C = 1 \text{ A}$, $I_B = 0.2 \text{ A}$

MAXIMUM RATINGS

Rating	Symbol	BUX 84	BUX 85	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CES}	800	1000	Vdc
Emitter Base Voltage	V_{EBO}	5		Vdc
Collector Current				Adc
– Continuous	I_C	2		
– Peak (1)	I_{CM}	3.0		
Base Current				Adc
– Continuous	I_B	0.75		
– Peak (1)	I_{BM}	1.0		
Reverse Base Current:				Adc
– Peak	I_{BM}	1		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	50		Watts
Derate above 25°C		400		mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		$^\circ\text{C}$

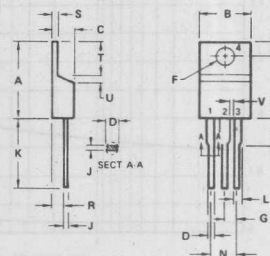
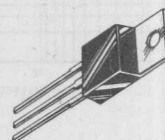
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient:	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

**2 AMPERES
TRIPLE DIFFUSED
POWER TRANSISTORS
NPN SILICON**

**400 - 450 VOLTS
50 WATTS**



STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

**CASE 221A-02
TO 220AB**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage ($I_C = 100\text{ mAdc}$, $L = 25\text{ mH}$) See fig. 1	BUX 84	400	—	—	Vdc
	BUX 85	450	—	—	
Collector Cutoff Current ($V_{CES} = \text{Rated Value}$) ($V_{CES} = \text{Rated Value}$, $T_C = 125^\circ\text{C}$)	ICES	—	—	0.2	mAdc
		—	—	1.5	
Emitter Cutoff Current ($V_{EB} = 5\text{ Vdc}$, $I_C = 0$)	IEBO	—	—	1	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 0.1\text{ Adc}$, $V_{CE} = 5\text{ V}$)	hFE	—	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 0.3\text{ Adc}$, $I_B = 30\text{ mAdc}$) ($I_C = 1\text{ Adc}$, $I_B = 200\text{ mAdc}$)	VCE(sat)	—	—	0.8	Vdc
		—	—	1	
Base-Emitter Saturation Voltage ($I_C = 1\text{ Adc}$, $I_B = 0.2\text{ Adc}$)	VBE(sat)	—	—	1.1	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product ($I_C = 500\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ MHz}$)	fT	—	—	—	MHz
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SWITCHING CHARACTERISTICS

Turn-on Time	$V_{CC} = 250\text{ Vdc}$, $I_C = 1\text{ A}$ $I_{B1} = 0.2\text{ A}$, $I_{B2} = 0.4\text{ A}$ See fig. 2	ton	—	0.3	0.5	μs
Storage Time		ts	—	2	3.5	μs
Fall Time		tf	—	0.3	—	μs
Fall Time	Same above cond. at $T_C = 95^\circ\text{C}$	tf	—	—	1.4	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

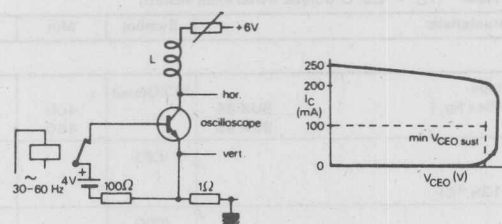
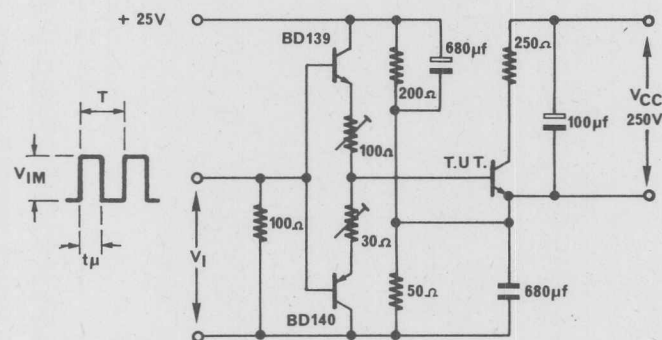
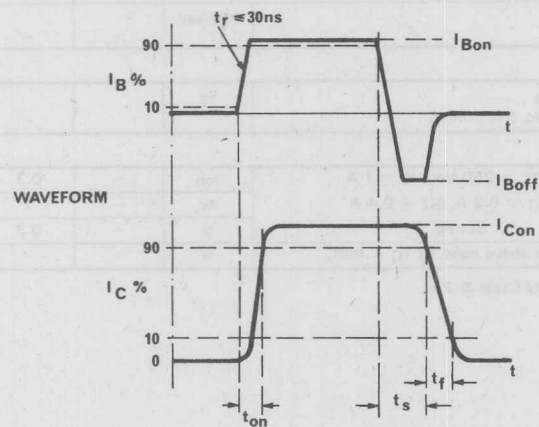
FIGURE 1 - TEST CIRCUIT FOR $V_{CE0\text{ sust}}$ 

FIGURE 2 - SWITCHING TIMES / TEST CIRCUIT



**MOTOROLA****MJ6502
MJ6503****Designers' Data Sheet****SWITCHMODE[▲]SERIES
PNP SILICON POWER TRANSISTORS**

The MJ6502 and MJ6503 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

100 ns Inductive Fall Time @ 25°C (Typ)

125 ns Inductive Crossover Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

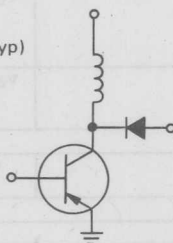
100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads

Switching Times with Inductive Loads

Saturation Voltages

Leakage Currents

**MAXIMUM RATINGS**

Rating	Symbol	MJ6502	MJ6503	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	400	Vdc
Collector-Emitter Voltage	V_{CEV}	300	450	Vdc
Emitter Base Voltage	V_{EB}	6.0	6.0	Vdc
Collector Current — Continuous	I_C	8.0	8.0	Adc
Peak (1)	I_{CM}	16	16	
Base Current — Continuous	I_B	4.0	4.0	Adc
Peak (1)	I_{BM}	8.0	8.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125	125	Watts
@ $T_C = 100^\circ\text{C}$		71.5	71.5	
Derate above 25°C		0.714	0.714	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

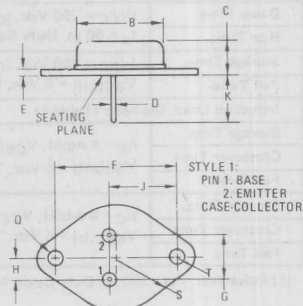
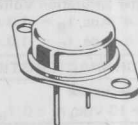
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering	T_L	275	°C
Purposes: 1/8" from Case for 5 Seconds			

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

8 AMPERES**PNP SILICON
POWER TRANSISTORS****250 and 400 VOLTS****Designer's Data for
"Worst Case" Conditions**

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	*1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 10\text{ mA}$, $I_B = 0$)	MJ6502 MJ6503 $V_{CEO(sus)}$	250 400	— —	— —	Vdc	
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	0.5 2.5	mAdc	
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	3.0	mAdc	
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc	
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12				
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13				
ON CHARACTERISTICS (1)						
DC Current Gain ($I_C = 2.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	15	—	—	—	
Collector-Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 3.0\text{ Adc}$) ($I_C = 4\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.5 5.0 2.5	Vdc	
Base-Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 4\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc	
DYNAMIC CHARACTERISTICS						
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	100	—	400	pF	
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 4.0\text{ A}$, $I_{B1} = 1.0\text{ A}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2\%$)	t_d	—	0.025	0.1	μs
Rise Time		t_r	—	0.100	0.5	μs
Storage Time		t_s	—	0.60	2.0	μs
Fall Time		t_f	—	0.11	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$(I_C = 4\text{ A(pk)}$, $V_{CE(pk)} = 250\text{ Vdc}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	0.8	3.0	μs
Crossover Time		t_c	—	0.4	1.5	μs
Fall Time		t_{fi}	—	0.1	—	μs
Storage Time		t_{sv}	—	0.5	—	μs
Crossover Time	$(I_C = 4\text{ A(pk)}$, $V_{CE(pk)} = 250\text{ Vdc}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_c	—	0.125	—	μs
Fall Time		t_{fi}	—	0.1	—	μs

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

FIGURE 1 — DC CURRENT GAIN

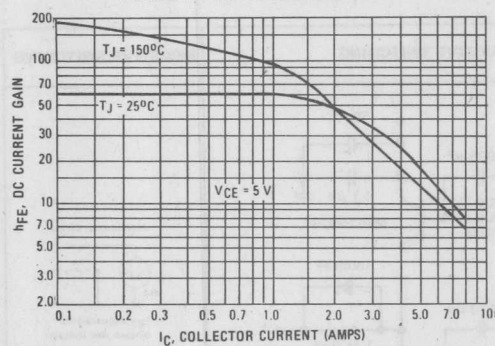


FIGURE 2 — COLLECTOR SATURATION REGION

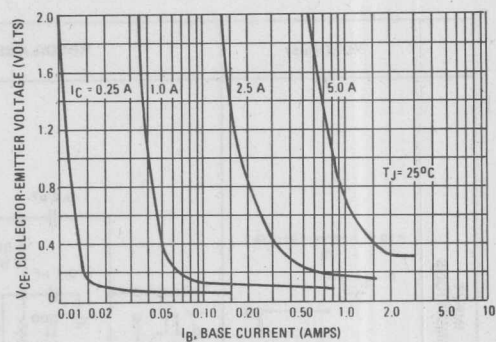


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

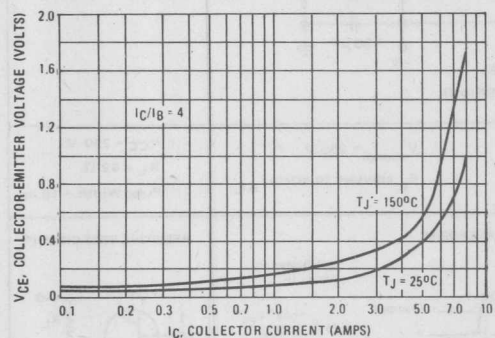


FIGURE 4 — BASE-EMITTER VOLTAGE

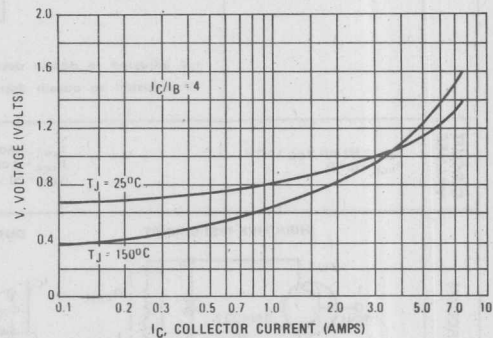


FIGURE 5 — COLLECTOR CUTOFF REGION

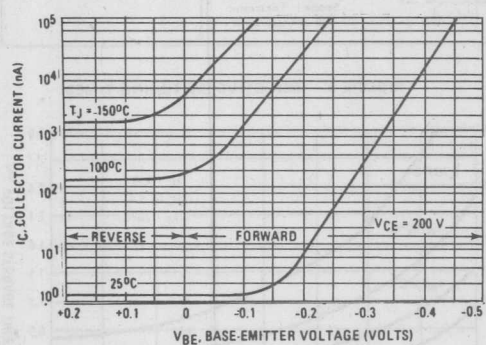


FIGURE 6 — CAPACITANCE

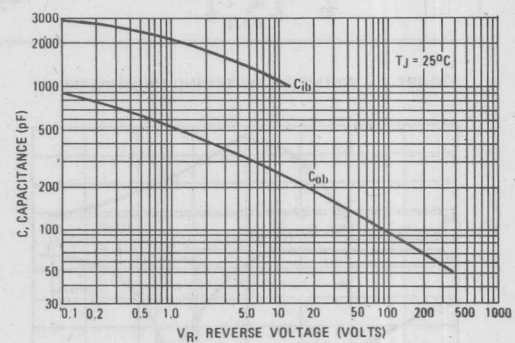


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

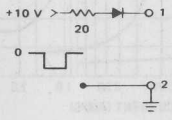
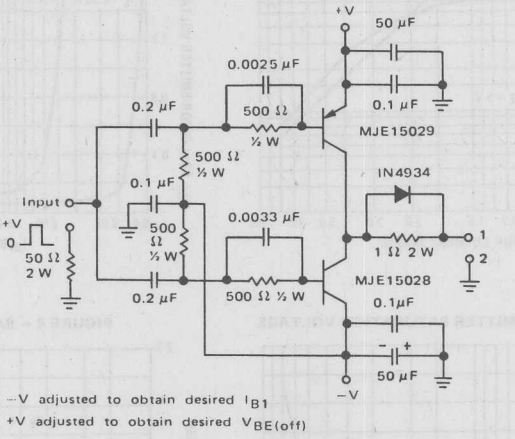
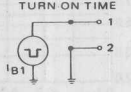
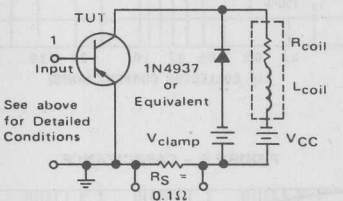
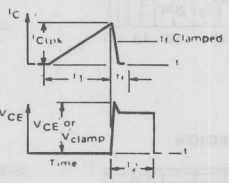
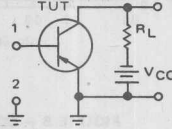
	V _{CE0(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>	 <p>—V adjusted to obtain desired I_{B1} +V adjusted to obtain desired $V_{BE(off)}$</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 250 \text{ V}$ R_B adjusted to attain I_{B1}	$V_{CC} = 250 \text{ V}$ $R_L = 62 \Omega$ Pulse Width = 10 μs
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$</p> <p>$t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

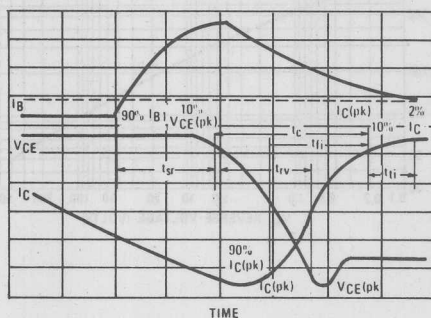
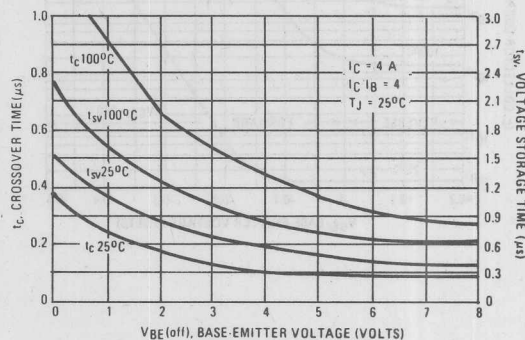


FIGURE 8 — INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CE} (pk)
- t_{rv} = Voltage Rise Time, 10–90% V_{CE} (pk)
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{CE} (pk) to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 9 – TURN - ON SWITCHING TIMES

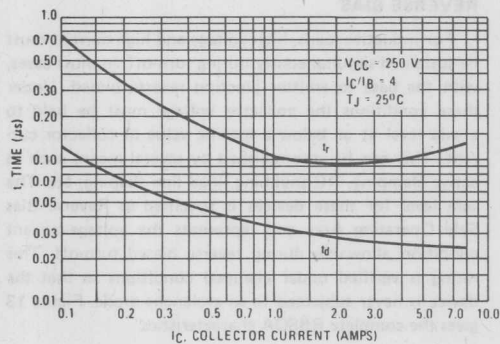


FIGURE 10 – TURN - OFF SWITCHING TIMES

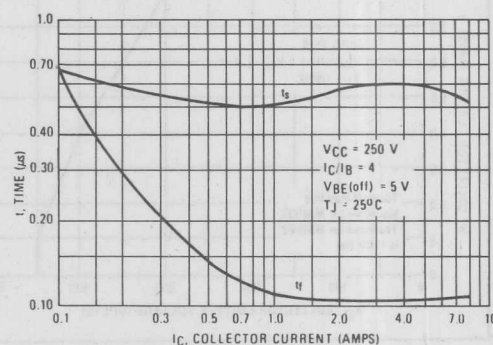
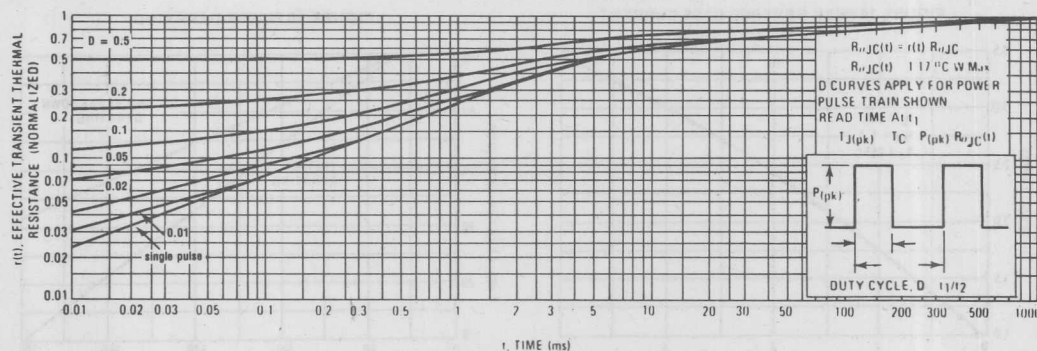


FIGURE 11 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

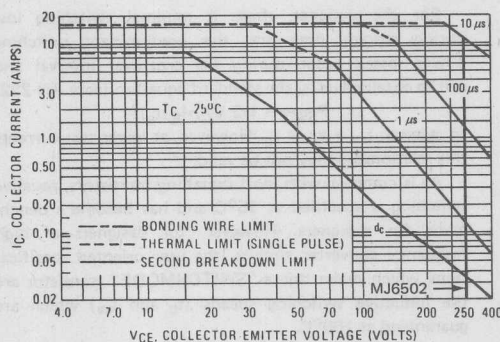


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA

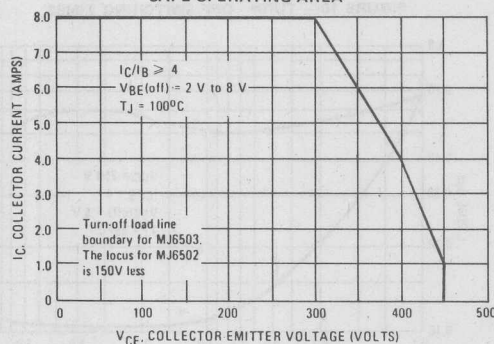
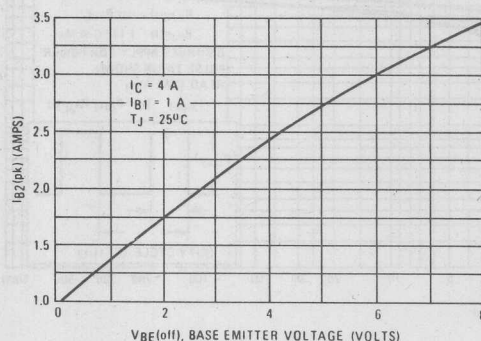


FIGURE 14 PEAK REVERSE BASE CURRENT



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

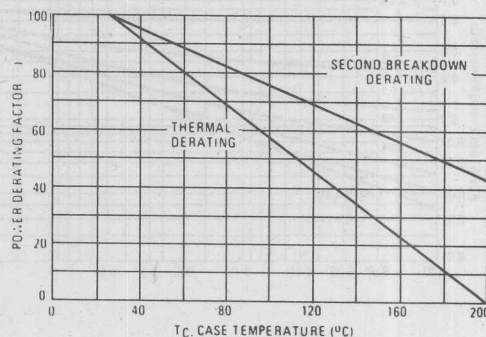
The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 15 POWER DERATING



**MOTOROLA****MJ8500
MJ8501****Designers' Data Sheet****SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTORS**

The MJ8500 and MJ8501 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

300 ns Inductive Fall Time — 25°C (Typ)
500 ns Inductive Crossover Time — 25°C (Typ)
900 ns Inductive Storage Time — 25°C (Typ)

Operating Temperature Range —65 to +200°C**100°C Performance Specified for:**

Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	MJ8500	MJ8501	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous	I_C	2.5	2.5	Adc
Peak (1)	I_{CM}	5.0	5.0	
Base Current — Continuous	I_B	2.0	2.0	Adc
Peak (1)	I_{RM}	4.0	4.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125	125	Watts
@ $T_C = 100^\circ\text{C}$		71	71	
Derate above 25°C		0.71	0.71	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering	T_L	275	°C

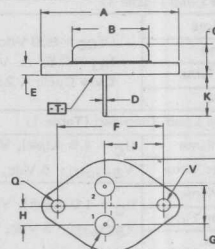
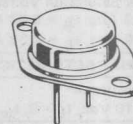
(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

2.5 AMPERE**NPN SILICON
POWER TRANSISTORS**

700 and 800 VOLTS
125 WATTS

**Designer's Data for
"Worst Case" Conditions**

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D:

$\pm 0.13 (0.005) \text{ T V } \odot$

FOR LEADS:

$\pm 0.13 (0.005) \text{ T V } \odot \text{ Q } \odot$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.27	—	1.550	—
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.23	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ8500 MJ8501 $V_{CEO(sus)}$	700 800	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^{\circ}\text{C}$)	I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^{\circ}\text{C}$)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 7.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.5	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$) ($I_C = 2.5\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$, $T_C = 100^{\circ}\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$) ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$, $T_C = 100^{\circ}\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	50	—	250	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	$(V_{CC} = 500\text{ Vdc}$, $I_C = 1.0\text{ A}$, $I_{B1} = 0.33\text{ A}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.045	0.20 μs
Rise Time		t_r	—	0.2	2.0 μs
Storage Time		t_s	—	1.0	4.0 μs
Fall Time		t_f	—	0.5	2.0 μs
Inductive Load, Clamped (Table 1)					
Storage Time	$(I_C = 1.0\text{ A(pk)}$, $V_{clamp} = 500\text{ Vdc}$, $I_{B1} = 0.33\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^{\circ}\text{C}$)	t_{sv}	—	1.3	4.0 μs
Crossover Time		t_c	—	0.6	2.0 μs
Storage Time		t_{sv}	—	0.9	— μs
Crossover Time		t_c	—	0.5	— μs
Fall Time	$(I_C = 1.0\text{ A(pk)}$, $V_{clamp} = 500\text{ Vdc}$, $I_{B1} = 0.33\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 25^{\circ}\text{C}$)	t_{fi}	—	0.3	— μs

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

FIGURE 1 – DC CURRENT GAIN

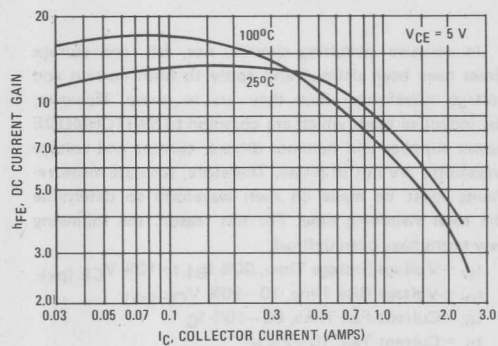


FIGURE 2 – COLLECTOR SATURATION REGION

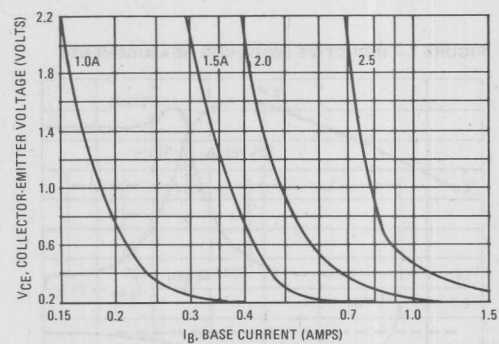


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

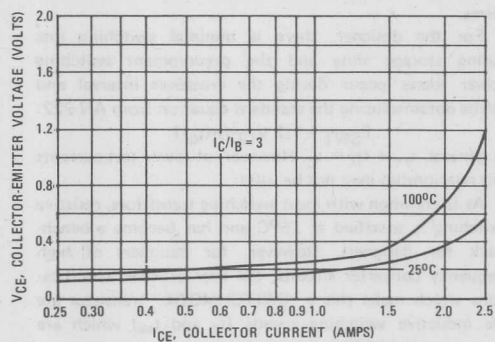


FIGURE 4 – BASE-EMITTER VOLTAGE

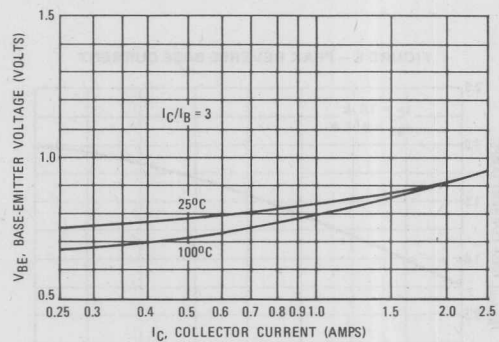


FIGURE 5 – COLLECTOR CUTOFF REGION

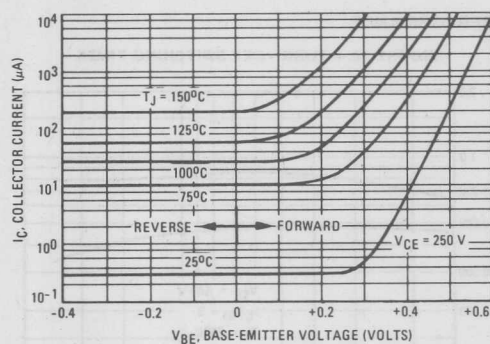


FIGURE 6 – CAPACITANCE

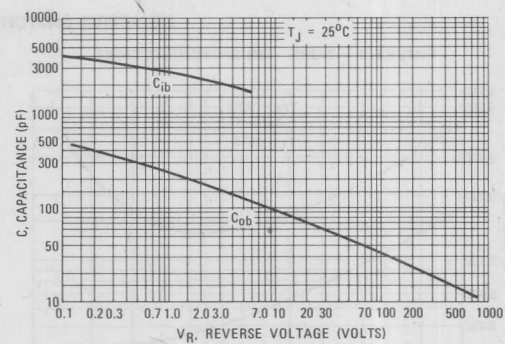


FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

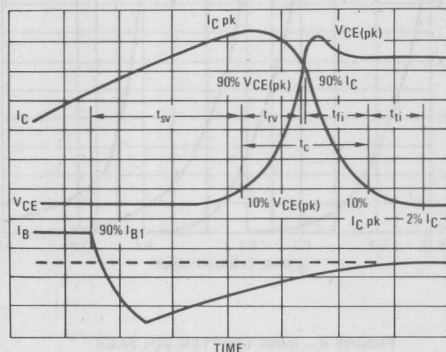
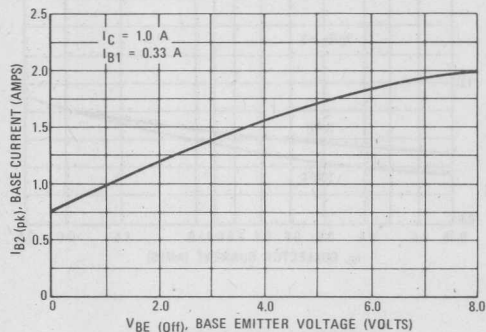
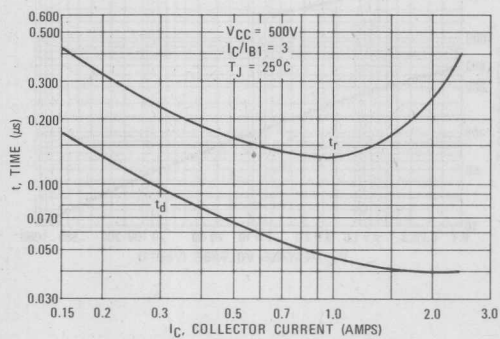


FIGURE 8 — PEAK REVERSE BASE CURRENT



RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN - ON SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$

t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 10 — TURN - OFF SWITCHING TIMES

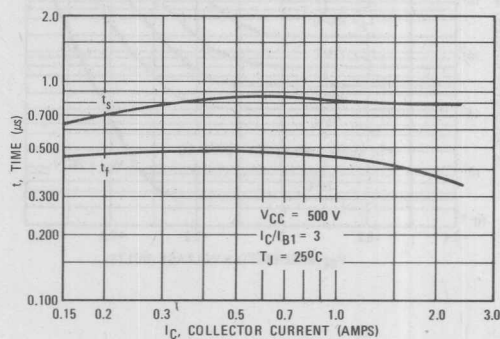


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

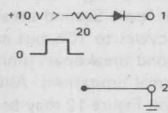
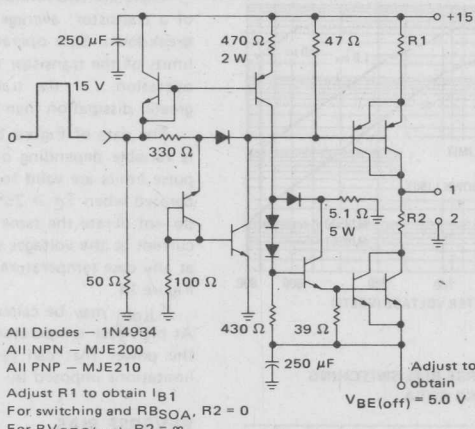
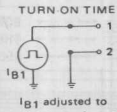
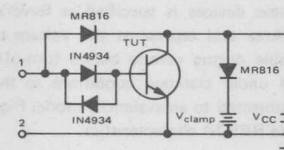
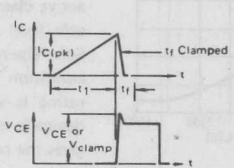
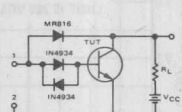
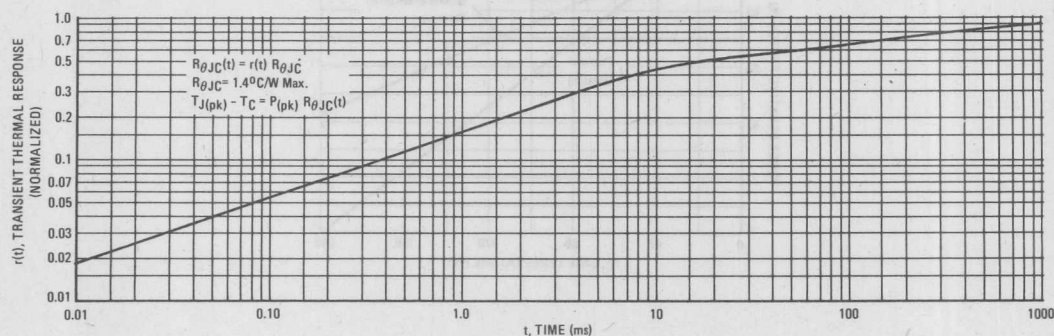
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>+10 V $\xrightarrow{20}$ 0</p> <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>	 <p>All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞</p> <p>Adjust to obtain $V_{BE(off)} = 5.0 \text{ V}$</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 500 \text{ V}$	$V_{CC} = 500 \text{ V}$ $R_L = 500 \Omega$ Pulse Width = $10 \mu\text{s}$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope – Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 	

FIGURE 11 – THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

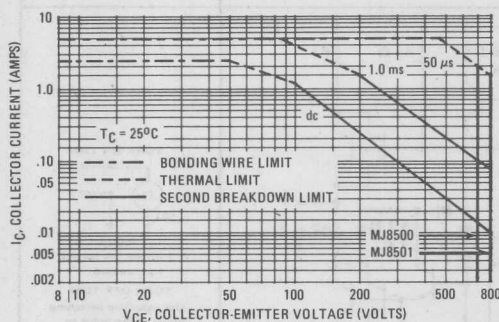
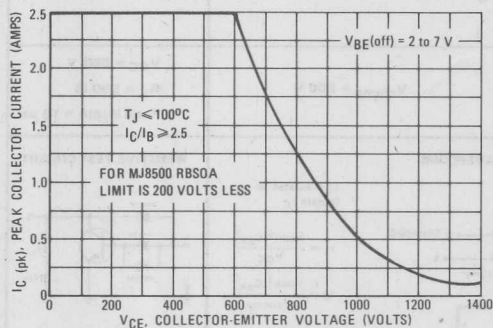
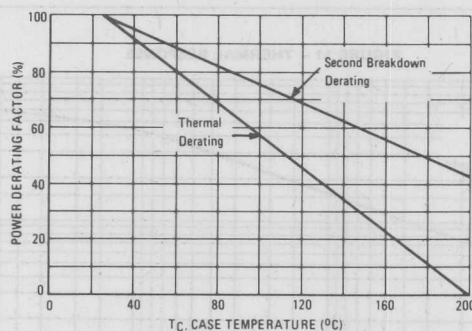
FIGURE 12 — MAXIMUM FORWARD BIAS
SAFE OPERATING AREAFIGURE 13 — RBSOA, REVERSE BIAS SWITCHING
SAFE OPERATING AREA

FIGURE 14 — POWER DERATING



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(pk)$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.



MOTOROLA

MJ8502 MJ8503

Designers' Data Sheet

SWITCHMODE[▲] SERIES NPN SILICON POWER TRANSISTORS

The MJ8502 and MJ8503 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

- 150 ns Inductive Fall Time—25°C (Typ)
- 400 ns Inductive Crossover Time—25°C (Typ)
- 1200 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range —65 to +200°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	MJ8502	MJ8503	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous	I_C	5.0	5.0	Adc
Peak (1)	I_{CM}	10	10	
Base Current — Continuous	I_B	4.0	4.0	Adc
Peak (1)	I_{BM}	8.0	8.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	150	Watts
@ $T_C = 100^\circ\text{C}$		86	86	
Derate above 25°C		0.85	0.85	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.16	°C/W
Maximum Lead Temperature for Soldering	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

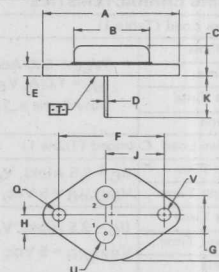
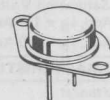
5.0 AMPERE

NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. \overline{T} IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\phi \pm 0.13 (0.005) \text{ T V } \phi$$

FOR LEADS:

$$\phi \pm 0.13 (0.005) \text{ T V } \phi \text{ Q } \phi$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.18	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.18	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ8502 MJ8503 $V_{CEO(sus)}$	700 800	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 7.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 1.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.5	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 2.5\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 2.5\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 2.5\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 2.5\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	60	—	300	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 500 A _{dc} , I _C = 2.5 A, I _{B1} = 1.0 A, V _{BE(off)} = 5.0 V _{dc} , t _p = 50 μs, Duty Cycle ≤ 2.0%)	t _d	—	0.040	0.20	μs
Rise Time		t _r	—	0.125	2.0	μs
Storage Time		t _s	—	1.2	4.0	μs
Fall Time		t _f	—	0.65	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I _C = 2.5 A(pk), V _{clamp} = 500 V _{dc} , I _{B1} = 1.0 A, V _{BE(off)} = 5 V _{dc} , T _C = 100°C)	t _{sv}	—	1.6	5.0	μs
Crossover Time		t _c	—	0.60	2.0	μs
Storage Time	(I _C = 2.5 A(pk), V _{clamp} = 500 V _{dc} , I _{B1} = 1.0 A, V _{BE(off)} = 5 V _{dc} , T _C = 25°C)	t _{sv}	—	1.2	—	μs
Crossover Time		t _c	—	0.4	—	μs
Fall Time		t _{fi}	—	0.15	—	μs

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

FIGURE 1 — DC CURRENT GAIN

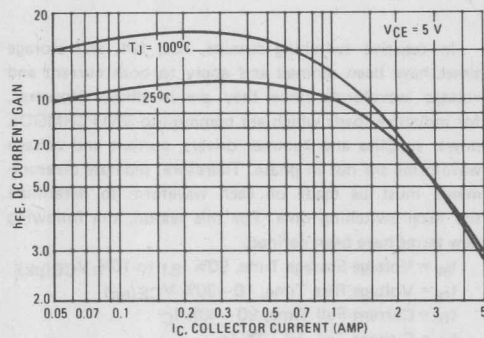


FIGURE 2 — COLLECTOR SATURATION REGION

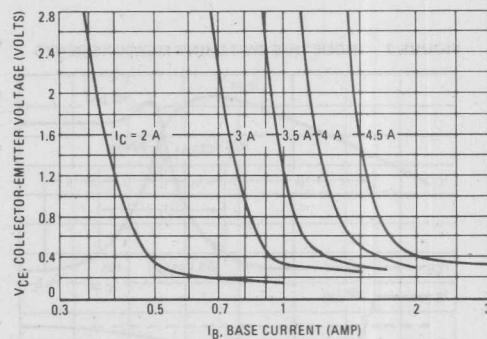


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

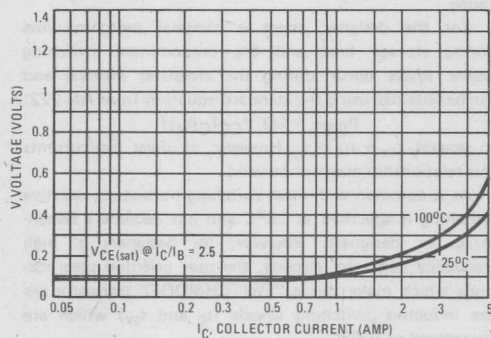


FIGURE 4 — BASE-EMITTER VOLTAGE

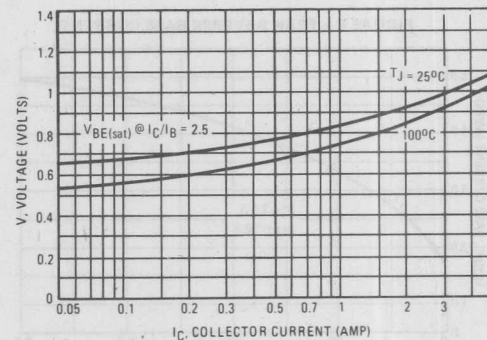


FIGURE 5 — COLLECTOR CUTOFF REGION

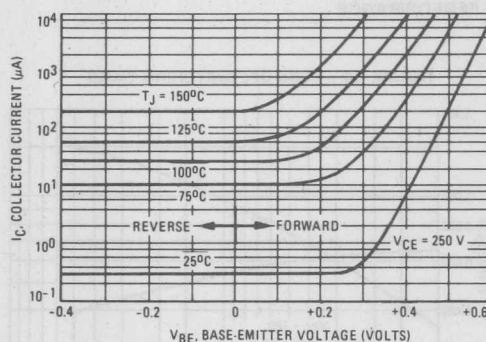


FIGURE 6 — CAPACITANCE

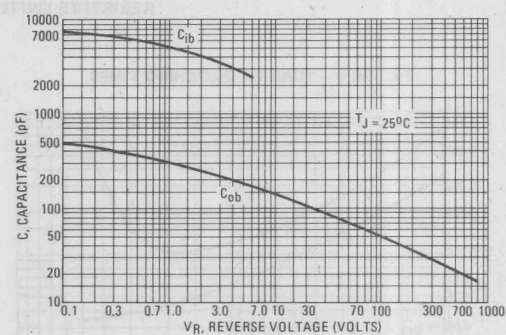


FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

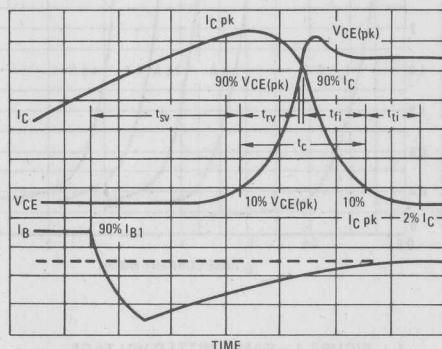
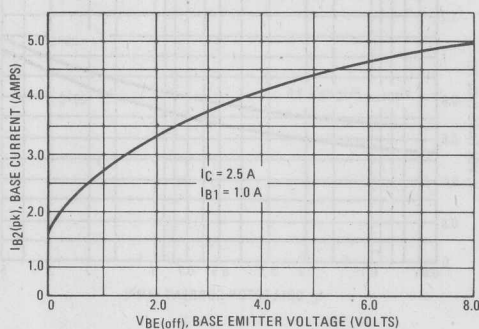


FIGURE 8 — PEAK REVERSE BASE CURRENT



RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN-ON SWITCHING TIMES

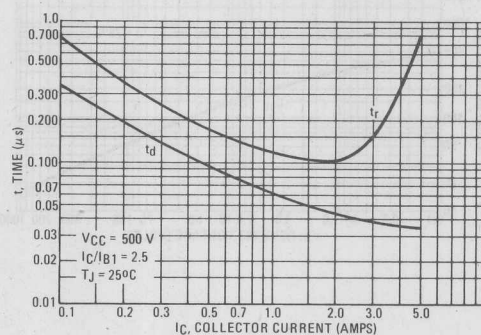
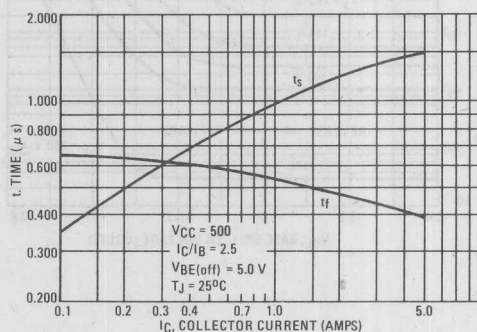


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t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

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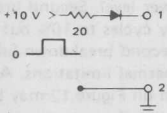
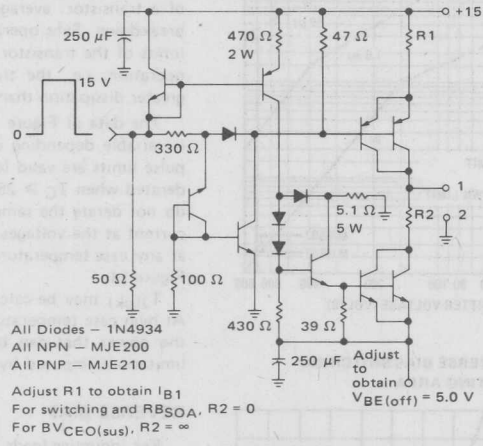
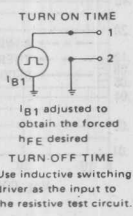
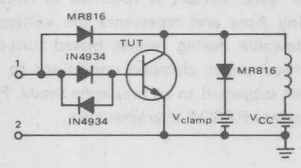
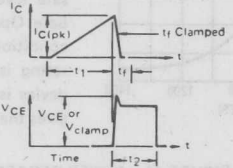
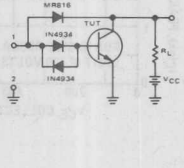
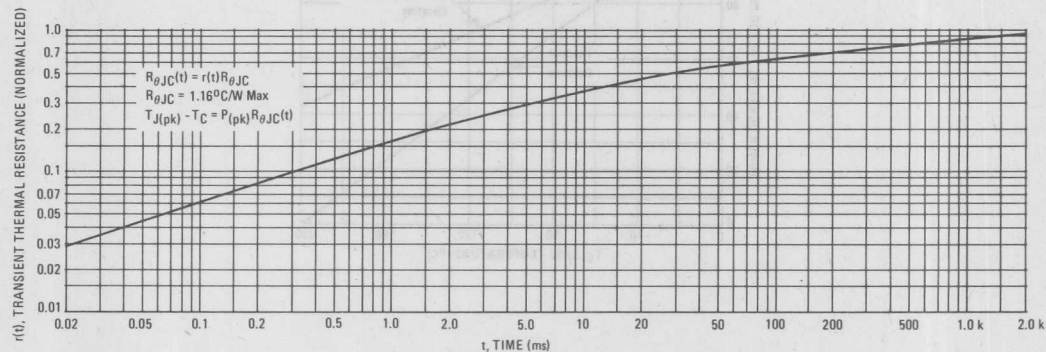
	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>	 <p>All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and R_{BSOA}, R2 = 0 For BV_{CEO(sus)}, R2 = ∞ Adjust to obtain V_{BE(off)} = 5.0 V</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	L _{coil} = 80 mH V _{CC} = 10 V R _{coil} = 0.7 Ω	L _{coil} = 180 μH R _{coil} = 0.05 Ω V _{CC} = 20 V V _{clamp} = 500 V	V _{CC} = 500 V R _L = 200 Ω Pulse Width = 10 μs
TEST CIRCUITS	 <p>INDUCTIVE TEST CIRCUIT</p>	 <p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C t₁ = $\frac{L_{coil}(I_{Cpk})}{V_{CC}}$ t₂ = $\frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent</p>	 <p>RESISTIVE TEST CIRCUIT</p>

FIGURE 11 – THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

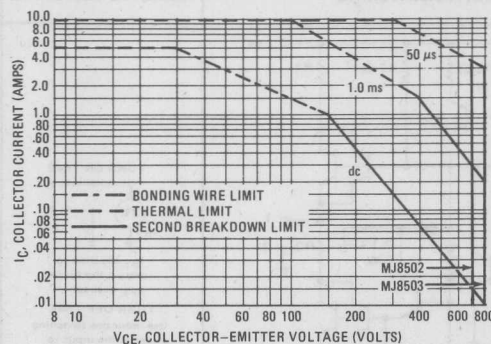
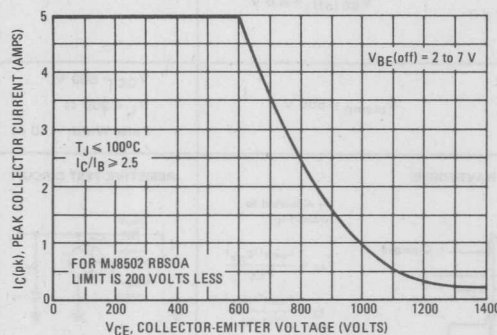


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



FORWARD BIAS

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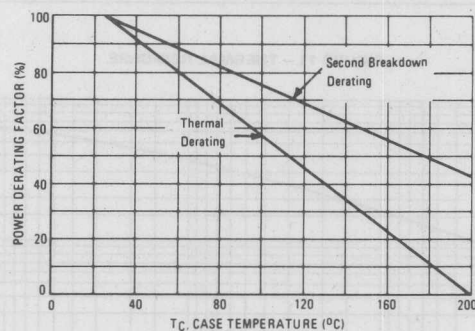
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FIGURE 14 — POWER DERATING



**MOTOROLA****MJ8504
MJ8505****Designers' Data Sheet****SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTORS**

The MJ8504 and MJ8505 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

75 ns Inductive Fall Time -25°C (typ)

150 ns Inductive Crossover Time -25°C (typ)

1.25 μs Inductive Storage Time -25°C (typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

Reverse-Biased SOA with Inductive Loads

Switching Times with Inductive Loads

Saturation Voltages

Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	MJ8504	MJ8505	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current - Continuous	I_C	10	10	Adc
Peak (1)	I_{CM}	15	15	Adc
Base Current - Continuous	I_B	8	8	Adc
Peak (1)	I_{BM}	12	12	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175	175	Watts
@ $T_C = 100^\circ\text{C}$		100	100	
Derate above 25°C		1.0	1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

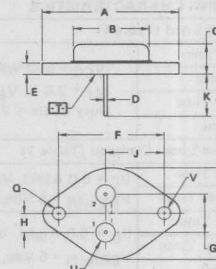
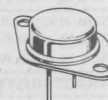
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering	T_L	275	°C
Purposes: 1/8" from Case for 5 Seconds			

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

10 AMPERE

**NPN SILICON
POWER TRANSISTORS**700 and 800 VOLTS
175 WATTS**Designer's Data for
"Worst Case" Conditions**

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.

**NOTES:**

1. DIMENSIONS Q AND V ARE DATUMS.
2. \square IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

 $\pm 0.13 (0.005) \text{ } \odot \text{ } T \text{ } V \text{ } \odot$

FOR LEADS:

 $\pm 0.13 (0.005) \text{ } \odot \text{ } T \text{ } V \text{ } \odot \text{ } Q \text{ } \odot$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	35.37	—	1.550	—
B	21.08	—	0.830	—
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	26.67	—	1.050	—
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ8504 MJ8505 $V_{CEO(sus)}$	700 800	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 7.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 1.5\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.5	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 4.0\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	90	—	450	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	$(V_{CC} = 500\text{ Vdc}$, $I_C = 5.0\text{ A}$, $I_{B1} = 2.0\text{ A}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.050	0.20 μs
Rise Time		t_r	—	0.175	2.0 μs
Storage Time		t_s	—	1.25	4.0 μs
Fall Time		t_f	—	0.60	2.0 μs
Inductive Load, Clamped (Table 1)					
Storage Time	$(I_C = 5.0\text{ A(pk)}$, $V_{clamp} = 500\text{ Vdc}$, $I_{B1} = 2.0\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	1.75	5.5 μs
Crossover Time		t_c	—	0.400	2.0 μs
Storage Time		t_{sv}	—	1.25	— μs
Crossover Time		t_c	—	0.150	— μs
Fall Time	$(I_C = 5.0\text{ A(pk)}$, $V_{clamp} = 500\text{ Vdc}$, $I_{B1} = 2.0\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_{fi}	—	0.075	— μs

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

FIGURE 1 — DC CURRENT GAIN

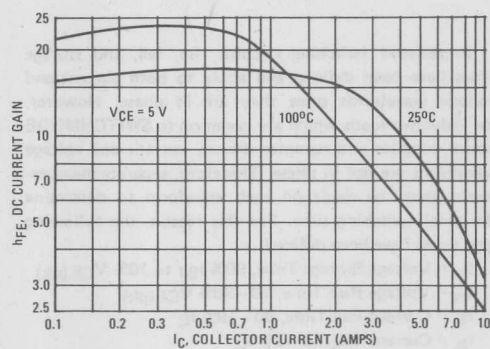


FIGURE 2 — COLLECTOR SATURATION REGION

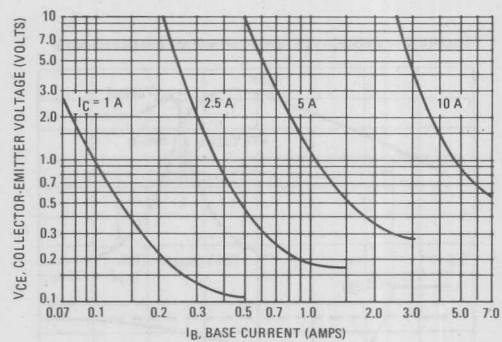


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

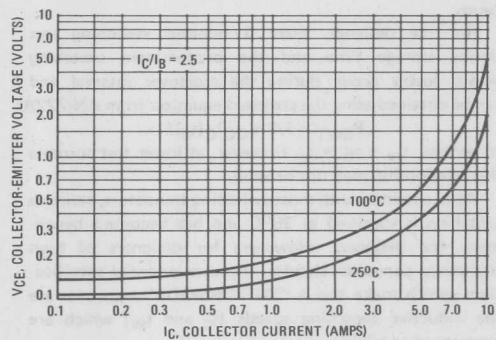


FIGURE 4 — BASE-EMITTER VOLTAGE

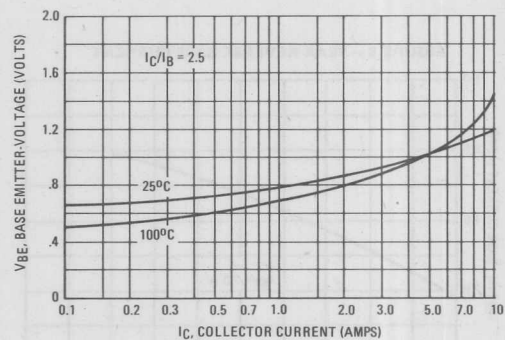


FIGURE 5 — COLLECTOR CUTOFF REGION

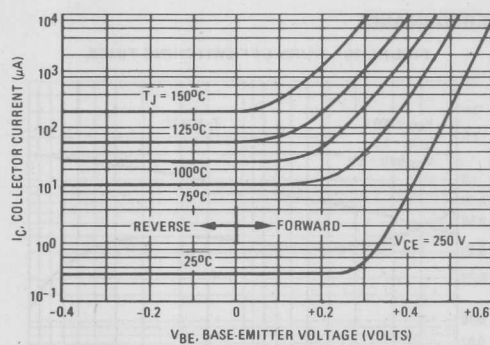


FIGURE 6 — CAPACITANCE

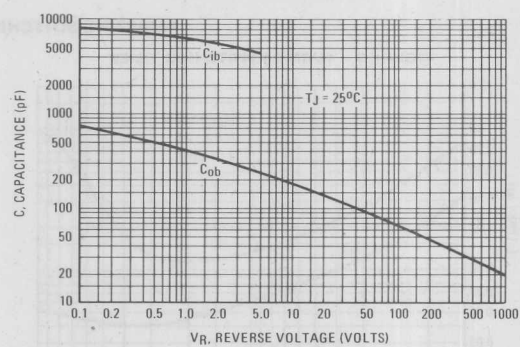


FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

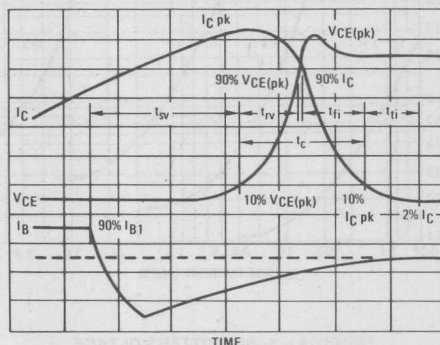
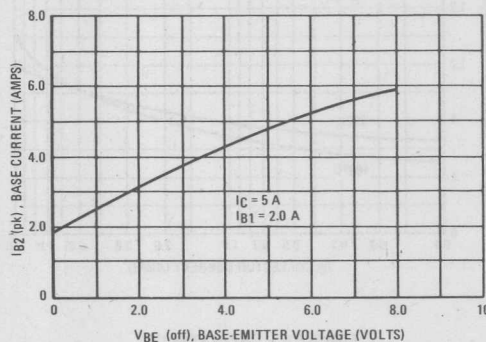
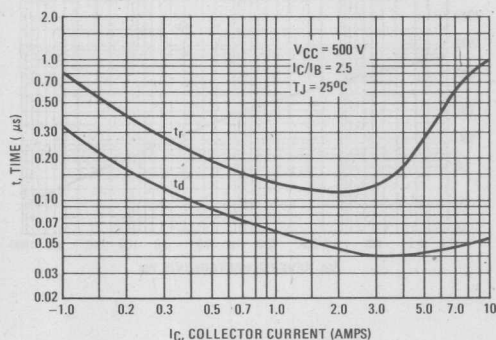


FIGURE 8 – PEAK REVERSE BASE CURRENT



RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$

t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 10 – TURN-OFF SWITCHING TIMES

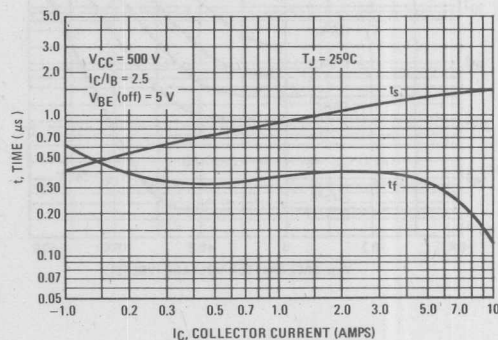


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

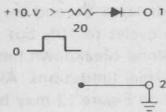
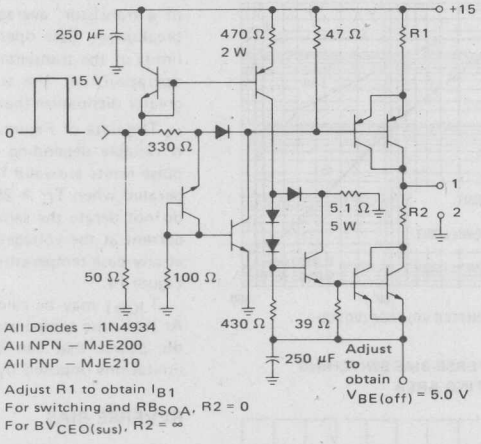
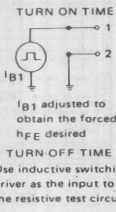
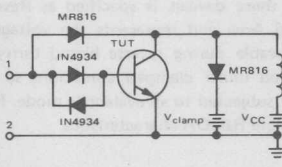
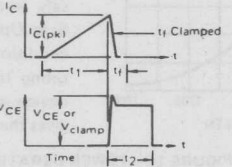
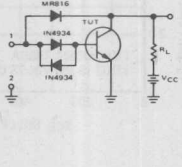
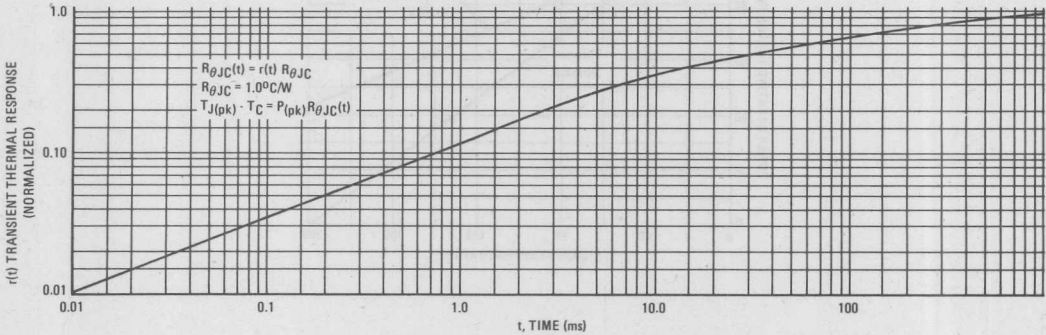
	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>	 <p>All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and R_{BSOA}, R2 = 0 For BV_{CEO(sus)}, R2 = ∞ Adjust to obtain 0 V_{BE(off)} = 5.0 V</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	L _{coil} = 80 mH V _{CC} = 10 V R _{coil} = 0.7 Ω	L _{coil} = 180 μH R _{coil} = 0.05 Ω V _{CC} = 20 V V _{clamp} = 500 V	V _{CC} = 500 V R _L = 100 Ω Pulse Width = 10 μs
TEST CIRCUITS	 <p>INDUCTIVE TEST CIRCUIT</p>	 <p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent</p>	 <p>RESISTIVE TEST CIRCUIT</p>

FIGURE 11 – THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

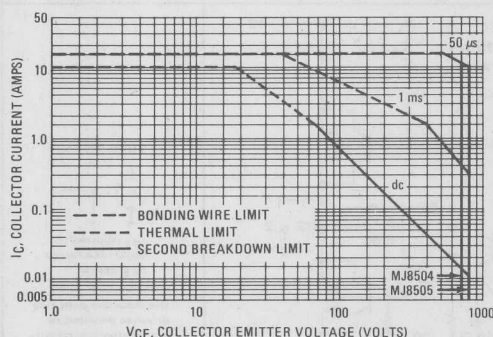


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA

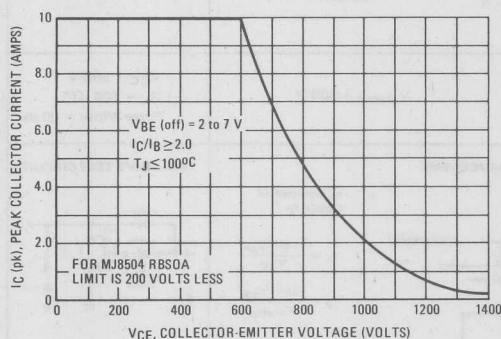
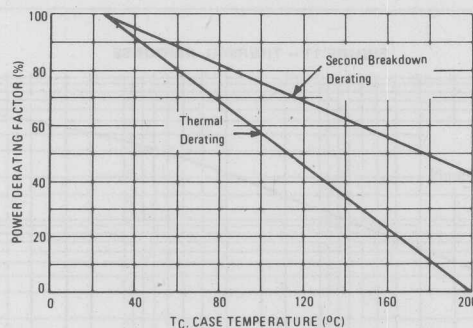


FIGURE 14 — POWER DERATING



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

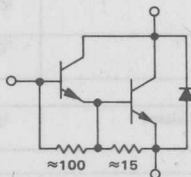
Designers' Data Sheet

SWITCHMODE^Δ SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10000 and MJ10001 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times With Inductive Loads –
210 ns Inductive Fall Time (Typ)
Saturation Voltages
Leakage Currents



MAXIMUM RATINGS

Rating	Symbol	MJ10000	MJ10001	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous	I_C	20		Adc
– Peak (1)	I_{CM}	30		
Base Current – Continuous	I_B	2.5		Adc
– Peak (1)	I_{BM}	5		
Total Power Dissipation @ $T_C = 25^{\circ}C$	P_D	175		Watts
@ $T_C = 100^{\circ}C$		100		
Derate above $25^{\circ}C$		1		W/ $^{\circ}C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^{\circ}C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	$^{\circ}\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^{\circ}\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

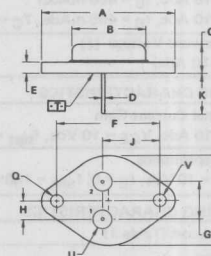
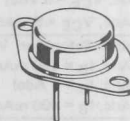
20 AMPERE
NPN SILICON

POWER DARLINGTON TRANSISTORS

350 and 400 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers[▲] Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



NOTES

- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
 2. $\boxed{-T-}$ IS SEATING PLANE AND DATUM
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$\frac{H}{D}$	0.13 (0.005) M	T	V M
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FOR LEADS:

4. DIMENSIONS AND TOLERANCES PER
ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
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Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 250\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	$V_{\text{CEO(sus)}}$	350 400	— —	— —	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) $I_C = 2\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$ $I_C = 10\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$	$V_{\text{CEX(sus)}}$	400 450 275 325	— — — —	— — — —	Vdc
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$) ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	0.25 5	mAdc
Collector Cutoff Current ($V_{\text{CE}} = \text{Rated } V_{\text{CEV}}$, $R_{\text{BE}} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current ($V_{\text{EB}} = 8\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	150	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{\text{S/b}}$	See Figure 11			Adc
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ON CHARACTERISTICS (2)

DC Current Gain ($I_C = 5\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$)	h_{FE}	50 40	— —	600 400	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$) ($I_C = 20\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{CE(sat)}}$	— — —	— — —	1.9 3 2	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$) ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{BE(sat)}}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage (1) ($I_F = 10\text{ Adc}$)	V_f	—	3	5	Vdc

DYNAMIC CHARACTERISTICS

Small-Signal Current Gain ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 10\text{ Vdc}$, $f_{\text{test}} = 1\text{ MHz}$)	$ h_{\text{fe}} $	10	—	—	—
Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	100	—	325	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)					
Delay Time ($V_{\text{CC}} = 250\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{\text{B1}} = 400\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2\%$)	t_d	—	0.12	0.2	μs
Rise Time	t_r	—	0.20	0.6	μs
Storage Time	t_s	—	1.5	3.5	μs
Fall Time	t_f	—	1.1	2.4	μs
Inductive Load, Clamped (Table 1)					
Storage Time ($I_C = 10\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 400\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	3.5	5.5	μs
Crossover Time	t_c	—	1.5	3.7	μs
Storage Time ($I_C = 10\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 400\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_{sv}	—	1.0	—	μs
Crossover Time	t_c	—	0.7	—	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

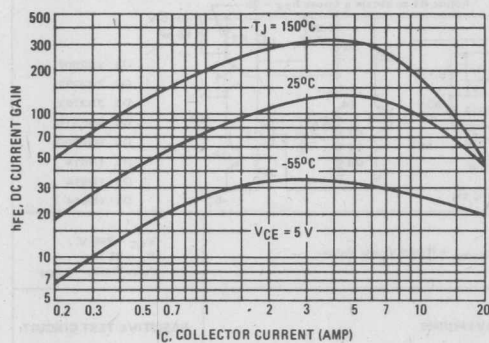


FIGURE 2 — COLLECTOR SATURATION REGION

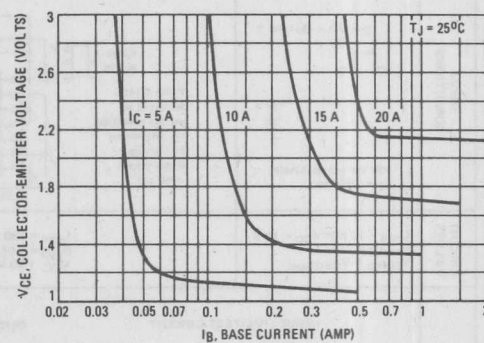


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGES

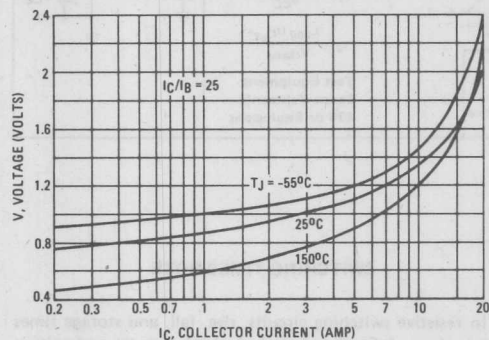


FIGURE 4 — BASE-EMITTER VOLTAGE

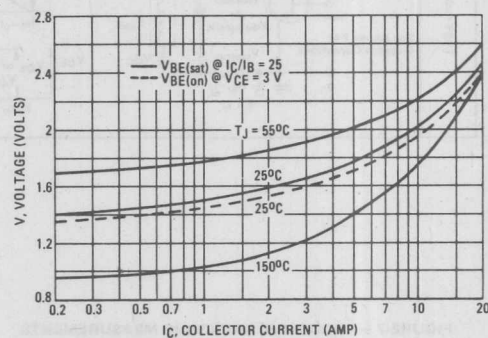


FIGURE 5 — COLLECTOR CUTOFF REGION

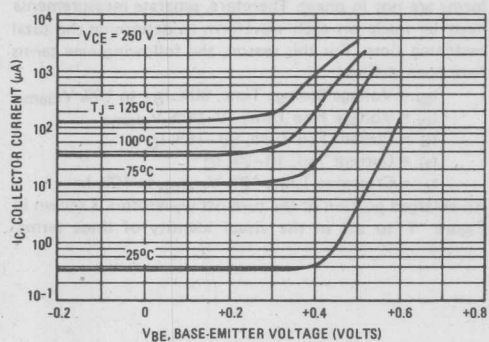


FIGURE 6 — OUTPUT CAPACITANCE

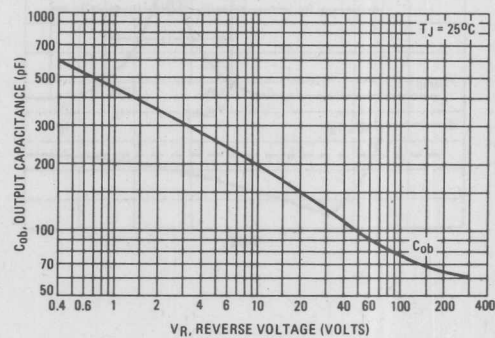
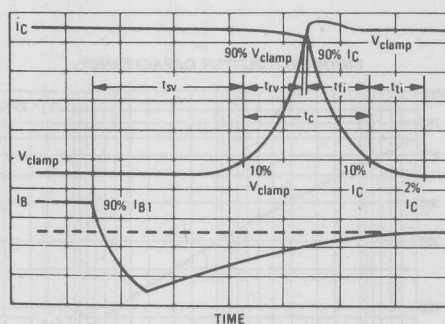


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	<p>$V_{CE0(sus)}$</p> <p>PW Varied to Attain $I_C = 250 \text{ mA}$</p>	<p>$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING</p> <p>Adjust $R1$ to obtain a forced $h_{FE} = 25$</p> <p>Duty Cycle $< 3\%$</p>	<p>RESISTIVE SWITCHING</p> <p>Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914</p>
INPUT CONDITIONS	<p>$L_{coil} = 10 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CE0(sus)}$</p>	<p>$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$</p> <p>$V_{clamp} = \text{Rated } V_{CEX} \text{ Value}$</p>	<p>$V_{CC} = 250 \text{ V}$ $R_L = 25 \Omega$ Pulse Width = $50 \mu\text{s}$</p>
CIRCUIT VALUES			
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> <p>t_1 Clamped t_1 Unclamped $\approx t_2$</p> <p>$t_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope-Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

SWITCHING TIMES NOTE

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS



In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{Clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

 t_c = Crossover Time, 10% V_o

enlarged portion of the turn-off waveforms is shown in Fig. 10. The

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

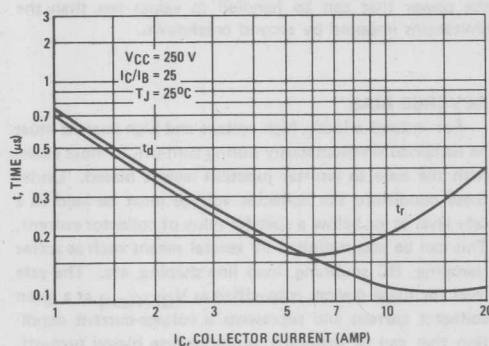


FIGURE 9 — TURN-OFF TIME

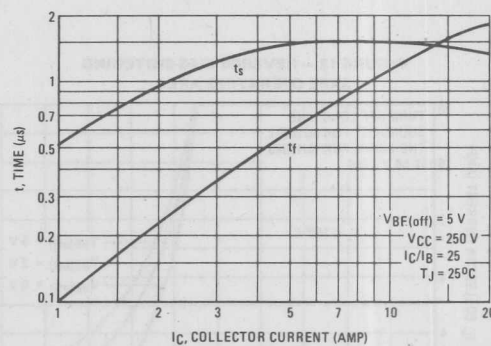
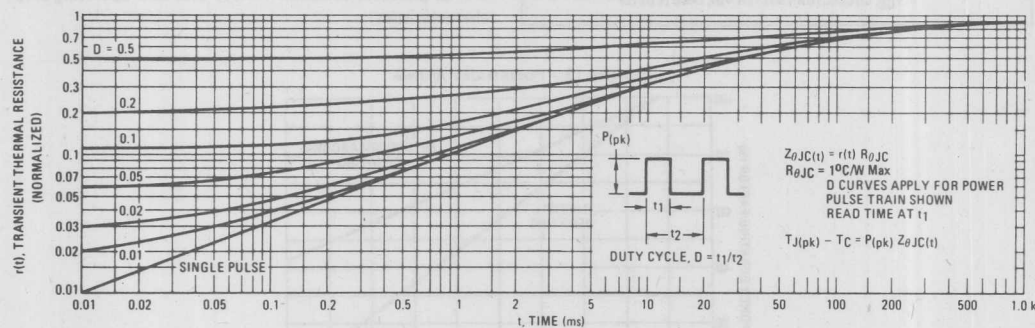
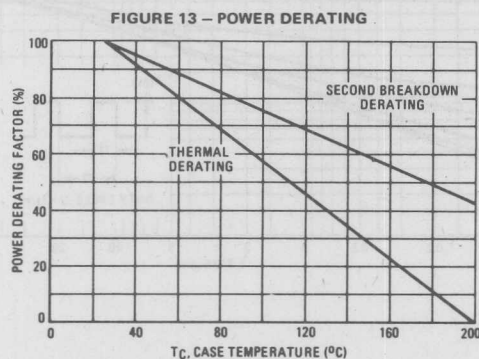
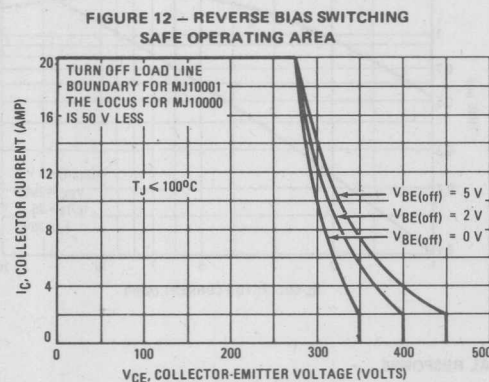
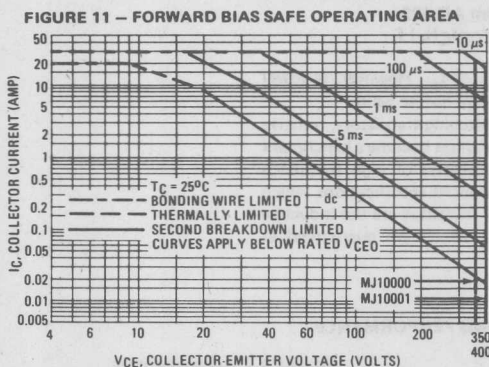


FIGURE 10 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(\text{sus})}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

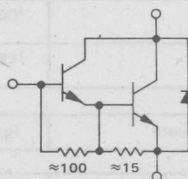
**MOTOROLA****MJ10002
MJ10003****Designers' Data Sheet****SWITCHMODE^Δ SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS**

The MJ10002 and MJ10003 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads —
140 ns Inductive Fall Time (Typ)
Saturation Voltages
Leakage Currents

**MAXIMUM RATINGS**

Rating	Symbol	MJ10002	MJ10003	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous	I_C	10		Adc
Collector Current — Peak (1)	I_{CM}	20		
Base Current — Continuous	I_B	2.5		Adc
Base Current — Peak (1)	I_{BM}	5		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150		Watts
Derate above 25°C		100		
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

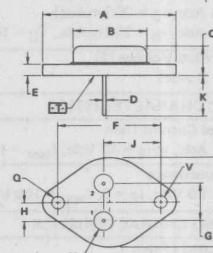
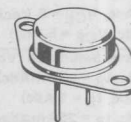
10 AMPERE
NPN SILICON

POWER DARLINGTON
TRANSISTORS

350 and 400 VOLTS
150 WATTS

**Designer's Data for
"Worst Case" Conditions**

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.

FOR LEADS:

13 (0.005) T V Q

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MIN	MAX	MIN	MAX
A	39.37	1.550		
B	21.08	0.830		
C	6.35	0.250		
D	0.87	0.034		
E	3.43	0.135		
F	30.15 BSC	1.187 BSC		
G	10.92 BSC	0.430 BSC		
H	5.46 BSC	0.215 BSC		
J	16.89 BSC	0.665 BSC		
K	11.18	0.440		
Q	3.81	0.150		
R	25.67	1.050		
U	4.83	0.190		
V	3.81	0.150		

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 250\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	$V_{\text{CEO(sus)}}$ MJ10002 MJ10003	350 400	— —	— —	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) ($I_C = 1\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$) ($I_C = 5\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$)	$V_{\text{CEX(sus)}}$ MJ10002 MJ10003 MJ10002 MJ10003	400 450 275 325	— — — —	— — — —	Vdc
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$) ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	0.25 5	mAdc
Collector Cutoff Current ($V_{\text{CE}} = \text{Rated } V_{\text{CEV}}$, $R_{\text{BE}} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current ($V_{\text{EB}} = 8\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{\text{S/b}}$	See Figure 11			Adc
ON CHARACTERISTICS (2)					
DC Current Gain ($I_C = 2.5\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$) ($I_C = 5\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$)	h_{FE}	40 30	— —	500 300	—
Collector-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 250\text{ mAdc}$) ($I_C = 10\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 5\text{ Adc}$, $I_B = 250\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{CE(sat)}}$	— — —	— — —	1.9 2.9 2	Vdc
Base-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 250\text{ mAdc}$) ($I_C = 5\text{ Adc}$, $I_B = 250\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{BE(sat)}}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage (1) ($I_F = 5.0\text{ Adc}$)	V_f	—	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 1\text{ Adc}$, $V_{\text{CE}} = 10\text{ Vdc}$, $f_{\text{test}} = 1\text{ MHz}$)	$ h_{\text{fe}} $	10	—	—	—
Output Capacitance ($V_{\text{CB}} = 50\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	60	—	275	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	$(V_{\text{CC}} = 250\text{ Vdc}$, $I_C = 5\text{ A}$, $I_{\text{B1}} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$).	t_d	—	0.05	0.2 μs
Rise Time		t_r	—	0.25	0.6 μs
Storage Time		t_s	—	1.2	3.0 μs
Fall Time		t_f	—	0.6	1.5 μs
Inductive Load, Clamped (Table 1)					
Storage Time	$(I_C = 5\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	2.1	5 μs
Crossover Time		t_c	—	1.3	3.3 μs
Storage Time	$(I_C = 5\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_{sv}	—	0.92	— μs
Crossover Time		t_c	—	0.5	— μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle < 2%.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

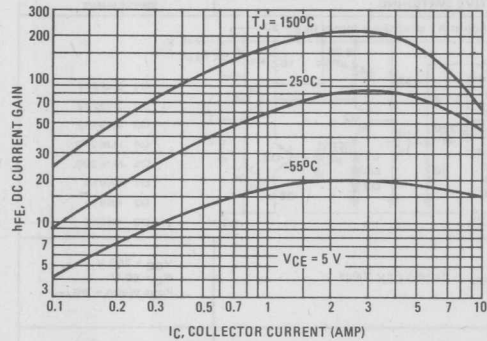


FIGURE 2 — COLLECTOR SATURATION REGION

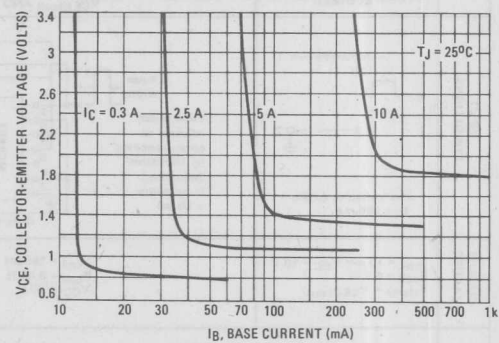


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

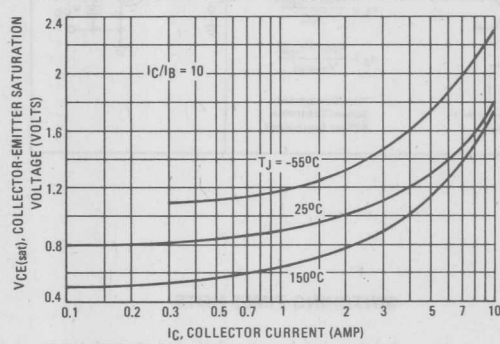


FIGURE 4 — BASE-EMITTER VOLTAGE

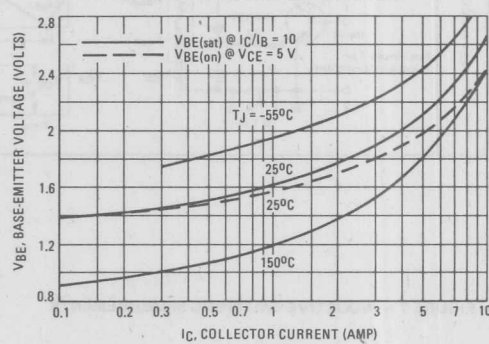


FIGURE 5 — COLLECTOR CUT-OFF REGION

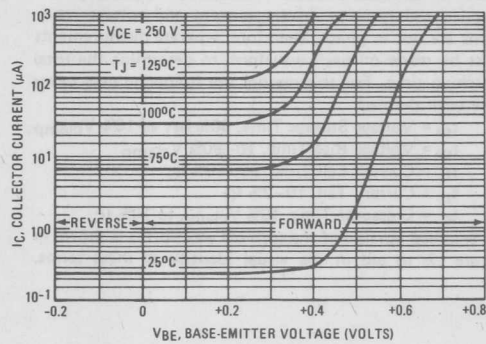


FIGURE 6 — OUTPUT CAPACITANCE

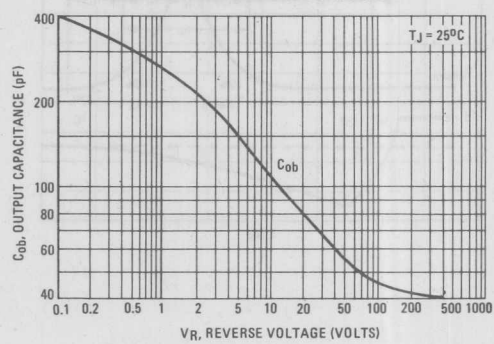
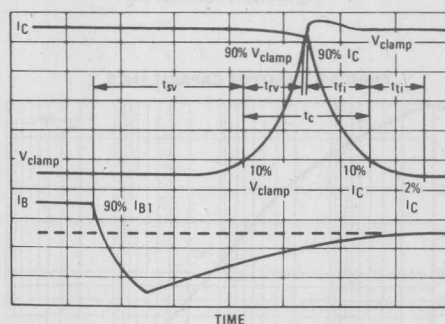


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO(sus)}	V _{CEX(sus)} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain $I_C = 250$ mA</p>	<p>Adjust R1 to obtain a forced $h_{FE} = 20$</p> <p>Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs)</p> <p>Duty Cycle < 3%</p>	<p>Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914</p>
CIRCUIT VALUES	<p>$L_{coil} = 10$ mH $V_{CC} = 10$ V $R_{coil} = 0.7$ Ω $V_{clamp} = V_{CEO(sus)}$</p>	<p>$L_{coil} = 180$ μH $R_{coil} = 0.05$ Ω $V_{CC} = 20$ V $V_{clamp} = \text{Rated } V_{CEX} \text{ Value}$</p>	<p>$V_{CC} = 250$ V $R_L = 50$ Ω Pulse Width = 50 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 = \frac{L_{coil} (I_{Cpk})}{V_{CC}}$</p> <p>$t_2 = \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope-Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> <p>See Above For Detailed Conditions</p>

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_B to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

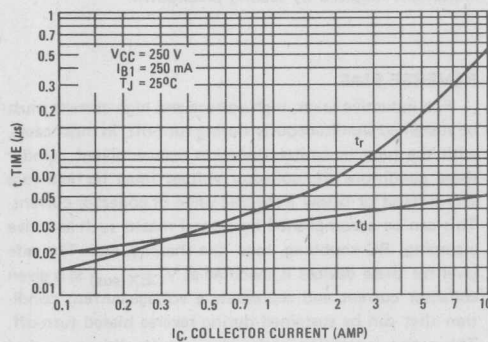


FIGURE 9 – TURN-OFF TIME

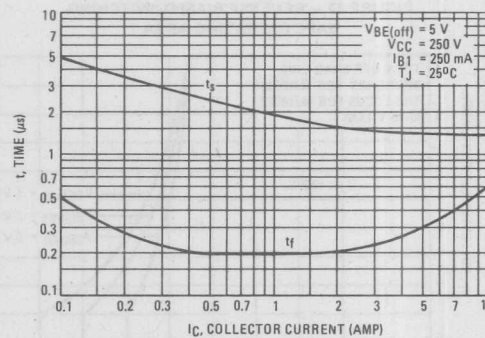
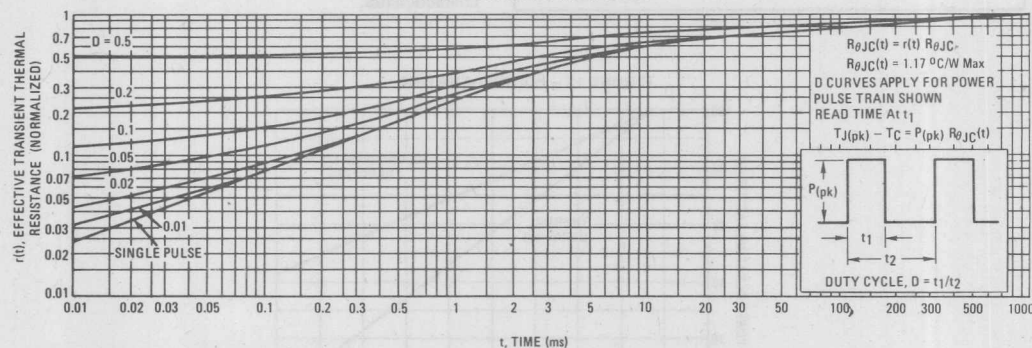


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – ACTIVE-REGION SAFE OPERATING AREA

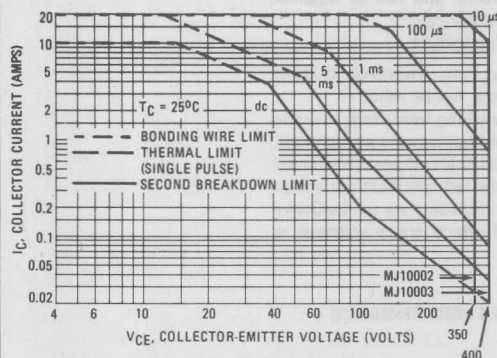
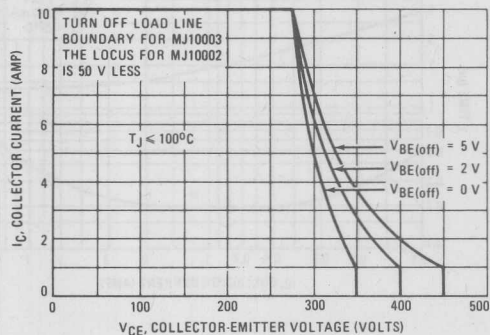


FIGURE 12 – REVERSE BIASED SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

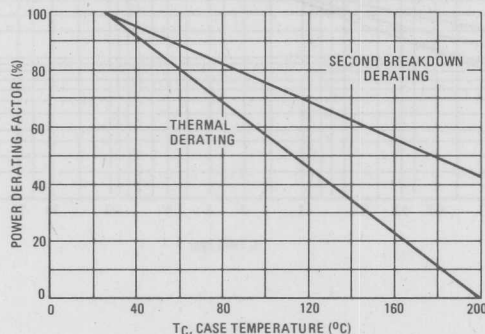
The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(\text{sus})}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



**MOTOROLA****MJ10004****MJ10005****Designers Data Sheet****SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE**

The MJ10004 and MJ10005 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

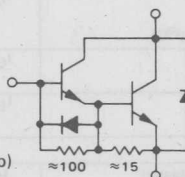
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times

40 ns Inductive Fall Time — 25°C (Typ)
650 ns Inductive Storage Time — 25°C (Typ)

Operating Temperature Range — 65 to +200°C

100°C Performance Specified for:

- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



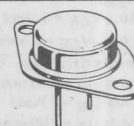
20 AMPERE
NPN SILICON

POWER DARLINGTON
TRANSISTORS

350 and 400 VOLTS
175 WATTS

**Designer's Data for
"Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

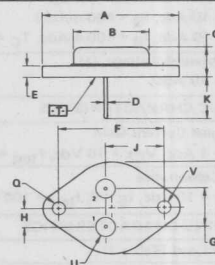
**MAXIMUM RATINGS**

Rating	Symbol	MJ10004	MJ10005	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous	I_C	20		Adc
— Peak (1)	I_{CM}	30		
Base Current — Continuous	I_B	2.5		Adc
— Peak (1)	I_{BM}	5		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	P_D	175 100		Watts
Derate above 25°C		1		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%



NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. \square IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$\phi .13 (0.005) \text{ } \ominus \text{ } T \text{ } V \text{ } \ominus$

FOR LEADS:

$\phi .13 (0.005) \text{ } \ominus \text{ } T \text{ } V \text{ } \ominus \text{ } Q \text{ } \ominus$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	38.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC	1.187 BSC		
G	10.92 BSC	0.430 BSC		
H	5.46 BSC	0.215 BSC		
J	16.89 BSC	0.665 BSC		
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 250\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$) MJ10004 MJ10005	$V_{\text{CEO(sus)}}$	350 400	— —	— —	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) ($I_C = 2\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$) MJ10004 MJ10005 ($I_C = 10\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$) MJ10004 MJ10005	$V_{\text{CEX(sus)}}$	400 450 275 325	— — — —	— — — —	Vdc
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$) ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	0.25 5	mAdc
Collector Cutoff Current ($V_{\text{CE}} = \text{Rated } V_{\text{CEV}}$, $R_{\text{BE}} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current ($V_{\text{EB}} = 2\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{\text{S/b}}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain ($I_C = 5\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$)	h_{FE}	50 40	— —	600 400	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$) ($I_C = 20\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{CE(sat)}}$	— — —	— — —	1.9 3 2	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$) ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{BE(sat)}}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage (1) ($I_F = 10\text{ Adc}$)	V_f	—	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 1\text{ Adc}$, $V_{\text{CE}} = 10\text{ Vdc}$, $f_{\text{test}} = 1\text{ MHz}$)	$ h_{\text{fe}} $	10	—	—	—
Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	100	—	325	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	$(V_{\text{CC}} = 250\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{\text{B1}} = 400\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2\%$).	t_d	—	0.12	0.2 μs
Rise Time		t_r	—	0.2	0.6 μs
Storage Time		t_s	—	0.6	1.5 μs
Fall Time		t_f	—	0.15	0.5 μs
Inductive Load, Clamped (Table 1)					
Storage Time	$(I_C = 10\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 400\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	1.0	2.5 μs
Crossover Time		t_c	—	0.4	1.5 μs
Storage Time	$(I_C = 10\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 400\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_{sv}	—	0.65	— μs
Crossover Time		t_c	—	0.2	— μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

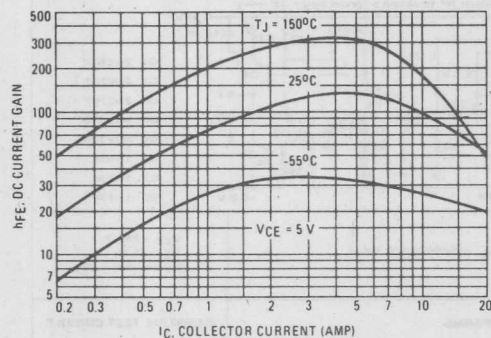


FIGURE 2 — COLLECTOR SATURATION REGION

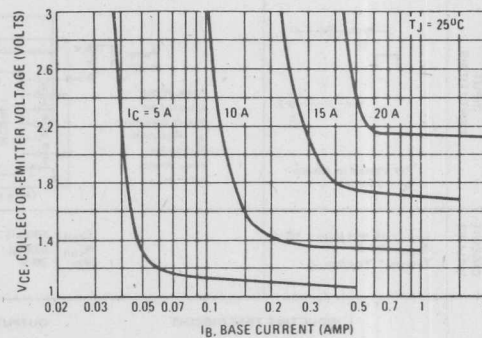


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

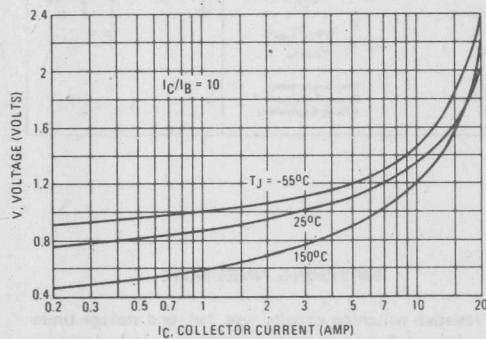


FIGURE 4 — BASE-EMITTER VOLTAGE

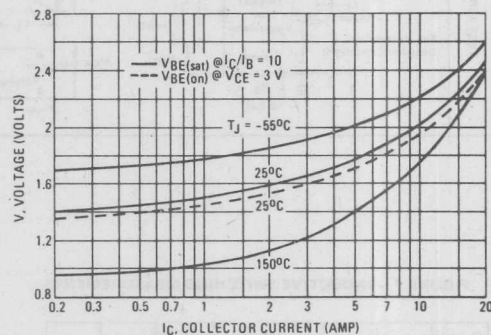


FIGURE 5 — COLLECTOR CUTOFF REGION

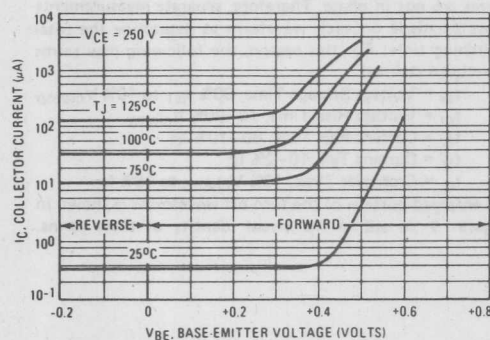
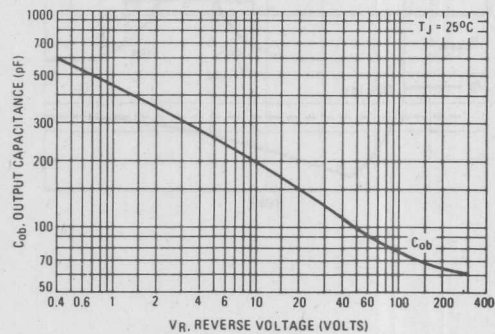


FIGURE 6 — OUTPUT CAPACITANCE



TYPICAL CHARACTERISTICS

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

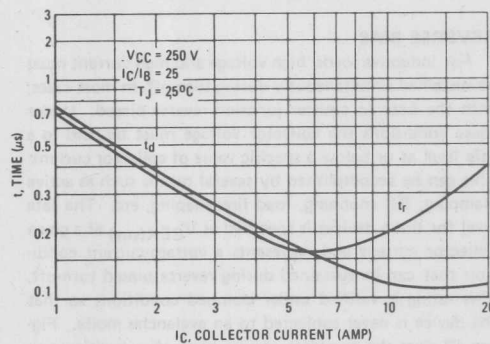


FIGURE 9 – TURN-OFF TIME

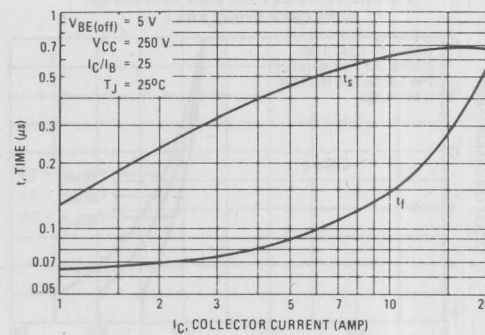
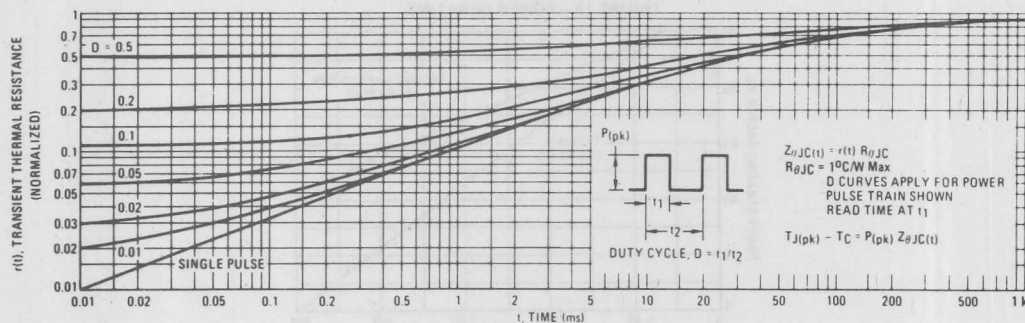


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATING AREA

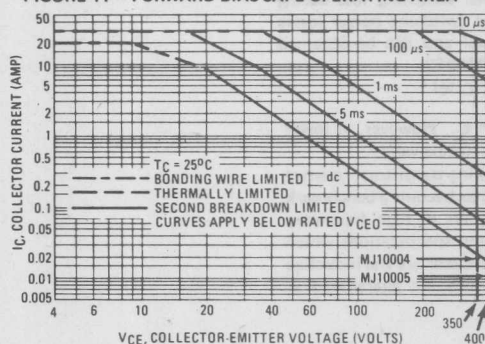
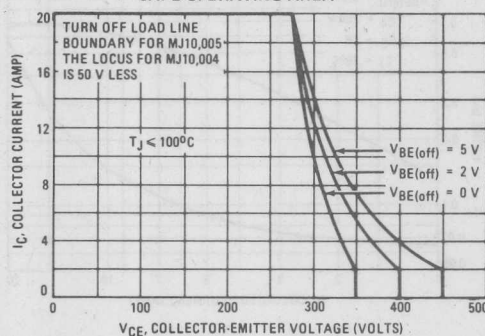


FIGURE 12 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

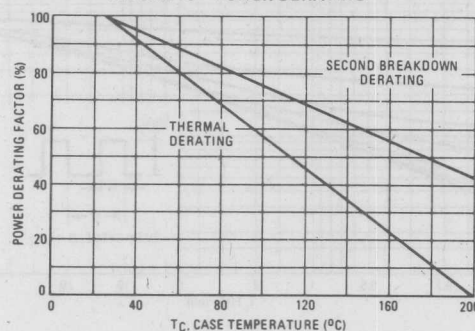
The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX}(\text{sus})$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 — POWER DERATING



**MOTOROLA****MJ10006****MJ10007****Designers Data Sheet****SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE**

The MJ10006 and MJ10007 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times

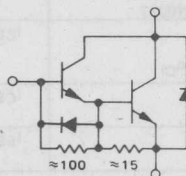
30 ns Inductive Fall Time – 25°C (Typ)

500 ns Inductive Storage Time – 25°C (Typ)

Operating Temperature Range –65 to +200°C

100°C Performance Specified for:

- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

**MAXIMUM RATINGS**

Rating	Symbol	MJ10006	MJ10007	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous	I_C	10		Adc
– Peak (1)	I_{CM}	20		
Base Current – Continuous	I_B	2.5		Adc
– Peak (1)	I_{BM}	5		
Total Power Dissipation @ $T_C = 25^{\circ}C$	P_D	150		Watts
@ $T_C = 100^{\circ}C$		100		
Derate above $25^{\circ}C$		0.86		W/ $^{\circ}C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^{\circ}C$

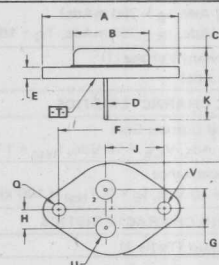
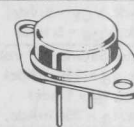
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

10 AMPERE**NPN SILICON****POWER DARLINGTON
TRANSISTORS****350 AND 400 VOLTS
150 WATTS****Designer's Data for
"Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
 2. [T] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Ø:

FOR LEADS:

Ø 0.13 (0.005) [T] [V] [W] [X] [Y] [Z]

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MIN	MAX	MIN	MAX
A	39.37	—	1.550	—
B	21.08	—	0.830	—
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	3.43	—	0.135	—
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	26.67	—	1.050	—
N	4.83	5.33	0.190	0.210
O	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 250\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	$V_{\text{CEO(sus)}}$	350 400	— —	— —	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) ($I_C = 1\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$)	$V_{\text{CEX(sus)}}$	400 450 275 325	— — — —	— — — —	Vdc
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$) ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	0.25 5	mAdc
Collector Cutoff Current ($V_{\text{CE}} = \text{Rated } V_{\text{CEV}}$, $R_{\text{BE}} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current ($V_{\text{EB}} = 2\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{\text{S/b}}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain ($I_C = 2.5\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$) ($I_C = 5\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$)	h_{FE}	40 30	— —	500 300	—
Collector-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 250\text{ mAdc}$) ($I_C = 10\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 5\text{ Adc}$, $I_B = 250\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{CE(sat)}}$	— — —	— — —	1.9 2.9 2	Vdc
Base-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 250\text{ mAdc}$) ($I_C = 5\text{ Adc}$, $I_B = 250\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{BE(sat)}}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage (1) ($I_F = 5\text{ Adc}$)	V_f	—	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 1\text{ Adc}$, $V_{\text{CE}} = 10\text{ Vdc}$, $f_{\text{test}} = 1\text{ MHz}$)	$ h_{\text{fe}} $	10	—	—	—
Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	60	—	275	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	$(V_{\text{CC}} = 250\text{ Vdc}$, $I_C = 5\text{ A}$, $I_{B1} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.05	0.2 μs
Rise Time		t_r	—	0.25	0.6 μs
Storage Time		t_s	—	0.5	1.5 μs
Fall Time		t_f	—	0.06	0.5 μs
Inductive Load, Clamped (Table 1)					
Storage Time	$(I_C = 5\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{B1} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	0.8	2.0 μs
Crossover Time		t_c	—	0.6	1.5 μs
Storage Time	$(I_C = 5\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{B1} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_{sv}	—	0.5	— μs
Crossover Time		t_c	—	0.3	— μs

- (1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.
- (2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

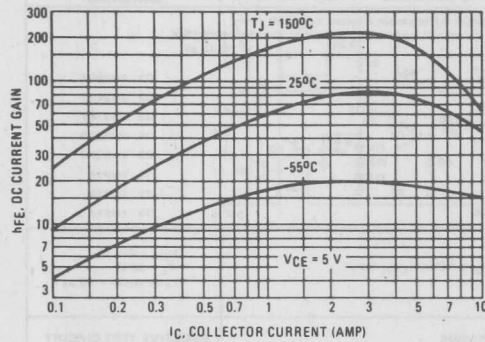


FIGURE 2 — COLLECTOR SATURATION REGION

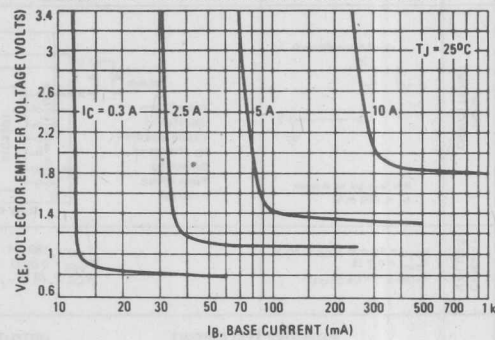


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

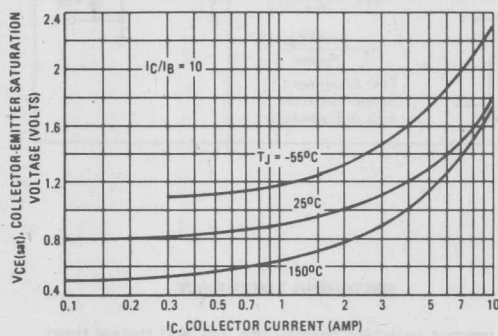


FIGURE 4 — BASE-EMITTER VOLTAGE

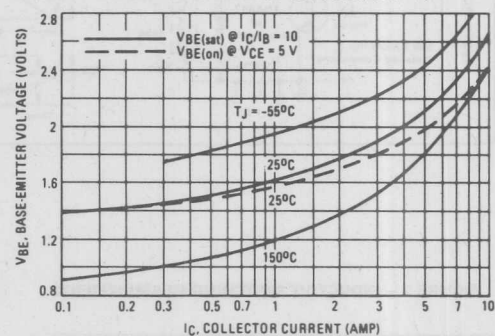


FIGURE 5 — COLLECTOR CUTOFF REGION

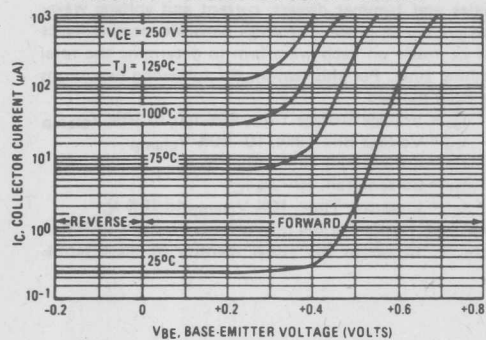


FIGURE 6 — OUTPUT CAPACITANCE

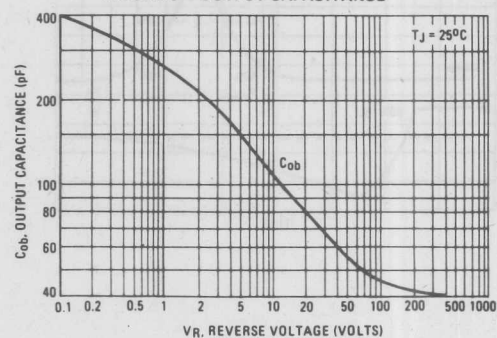
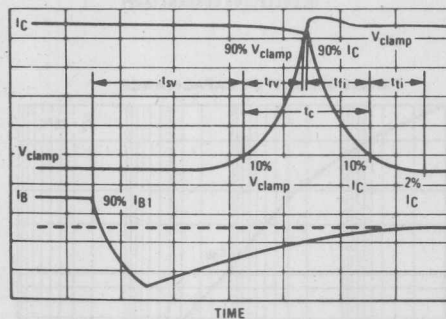


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CE0}(sus)$	$V_{CEX}(sus)$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain $I_C = 250$ mA</p>	<p>Adjust R1 to obtain a forced $h_{FE} = 20$</p> <p>Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs)</p> <p>Duty Cycle < 3%</p>	<p>Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914</p>
CIRCUIT VALUES	$L_{coil} = 10$ mH $V_{CC} = 10$ V $R_{coil} = 0.7$ Ω $V_{clamp} = V_{CE0}(sus)$	$L_{coil} = 180$ μ H $R_{coil} = 0.05$ Ω $V_{CC} = 20$ V $V_{clamp} = \text{Rated } V_{CEX} \text{ Value}$	$V_{CC} = 250$ V $R_L = 50$ Ω Pulse Width = 50 μ s
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 = \frac{L_{coil} (I_{Cpk})}{V_{CC}}$</p> <p>$t_2 = \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

TYPICAL CHARACTERISTICS

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

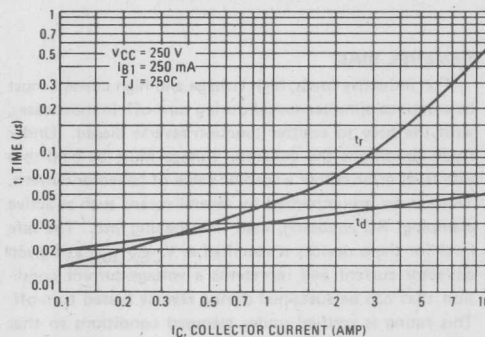


FIGURE 9 – TURN-OFF TIME

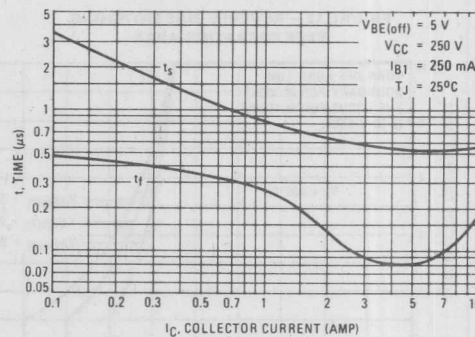
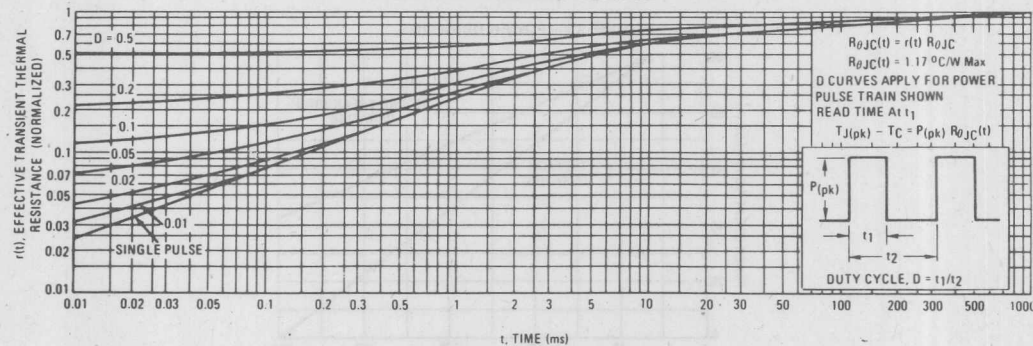


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATING AREA

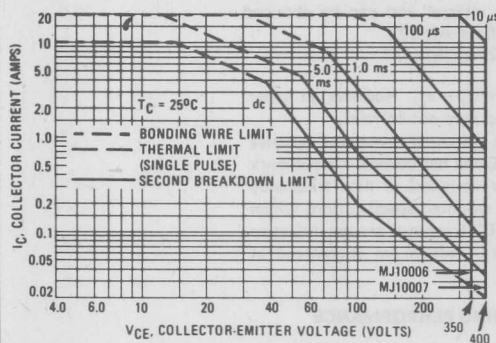
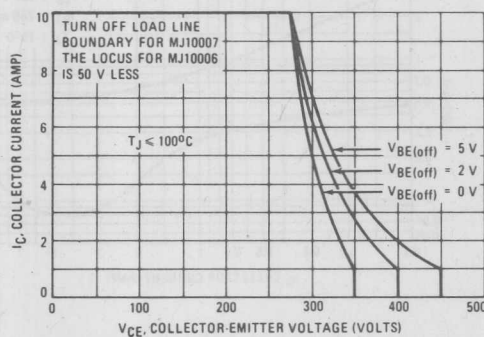


FIGURE 12 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

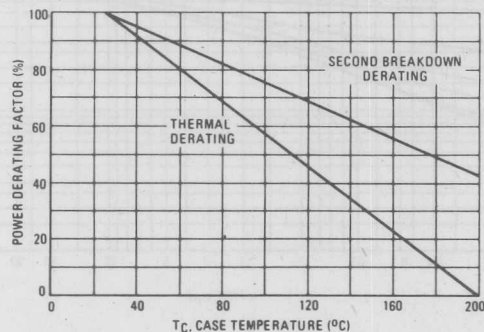
The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(\text{sus})}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 — POWER DERATING



**MOTOROLA****MJ10008
MJ10009****Designers' Data Sheet****SWITCHMODE[▲] SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE**

The MJ10008 and MJ10009 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

1.6 μ s (max) Inductive Crossover Time – 10 A, 100°C

3.5 μ s (max) Inductive Storage Time – 10 A, 100°C

Operating Temperature Range –65 to +200°C

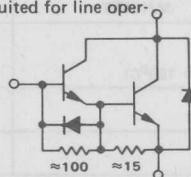
100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads

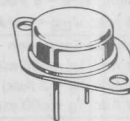
Switching Times with Inductive Loads

Saturation Voltages

Leakage Currents

**20 AMPERE****NPN SILICON****POWER DARLINGTON
TRANSISTORS****450 and 500 VOLTS****175 WATTS****Designer's Data for
"Worst Case" Conditions**

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

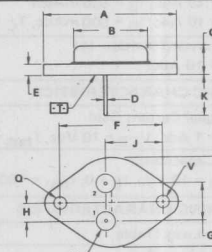
**MAXIMUM RATINGS**

Rating	Symbol	MJ10008	MJ10009	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	450	500	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	500	Vdc
Collector-Emitter Voltage	V_{CEV}	650	700	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous	I_C	20		Adc
– Peak (1)	I_{CM}	30		Adc
Base Current – Continuous	I_B	2.5		Adc
– Peak (1)	I_{BM}	5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175		Watts
@ $T_C = 100^\circ\text{C}$		100		
Derate above 25°C		1		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$\phi .13 (0.005) \text{ } \odot \text{ } T \text{ } \nabla \text{ } \odot$

FOR LEADS:

$\phi .13 (0.005) \text{ } \odot \text{ } T \text{ } \nabla \text{ } \odot \text{ } \odot$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	33.37	—	1.550
B	—	21.88	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.48 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	$V_{\text{CEO(sus)}}$	450 500	— —	— —	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) ($I_C = 2\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$, $V_{\text{BE(off)}} = 5\text{ V}$) ($I_C = 10\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$, $V_{\text{BE(off)}} = 5\text{ V}$)	$V_{\text{CEX(sus)}}$	450 500 325 375	— — — —	— — — —	Vdc
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$) ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	0.25 5	mA
Collector Cutoff Current ($V_{\text{CE}} = \text{Rated } V_{\text{CEV}}$, $R_{\text{BE}} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5	mA
Emitter Cutoff Current ($V_{\text{EB}} = 2\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	175	mA

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{\text{S/b}}$	See Figure 11			
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ON CHARACTERISTICS (2)

DC Current Gain ($I_C = 5\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$)	h_{FE}	40 30	— —	400 300	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 500\text{ mA}$) ($I_C = 20\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 500\text{ mA}$, $T_C = 100^\circ\text{C}$)	$V_{\text{CE(sat)}}$	— — —	— — —	2 3.5 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 500\text{ mA}$) ($I_C = 10\text{ Adc}$, $I_B = 500\text{ mA}$, $T_C = 100^\circ\text{C}$)	$V_{\text{BE(sat)}}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage (1) ($I_F = 10\text{ Adc}$)	V_f	—	3	5	Vdc

DYNAMIC CHARACTERISTICS

Small-Signal Current Gain ($I_C = 1\text{ Adc}$, $V_{\text{CE}} = 10\text{ Vdc}$, $f_{\text{test}} = 1\text{ MHz}$)	$ h_{\text{fe}} $	8	—	—	—
Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	100	—	325	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 250 Vdc, I _C = 10 A, I _{B1} = 500 mA, V _{BE(off)} = 5 Vdc, t _p = 25 μs Duty Cycle ≤ 2%)	t _d	—	0.12	0.25	μs
Rise Time		t _r	—	0.5	1.5	μs
Storage Time		t _s	—	0.8	2.0	μs
Fall Time		t _f	—	0.2	0.6	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I _C = 10 A(pk), V _{clamp} = 250 V, I _{B1} = 500 mA, V _{BE(off)} = 5 Vdc, T _C = 100°C)	t _{sv}	—	1.5	3.5	μs
Crossover Time		t _c	—	0.36	1.6	μs
Storage Time	(I _C = 10 A(pk), V _{clamp} = 250 V, I _{B1} = 500 mA, V _{BE(off)} = 5 Vdc)	t _{sv}	—	0.8	—	μs
Crossover Time		t _c	—	0.18	—	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: $\text{PW} = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 1 – DC CURRENT GAIN

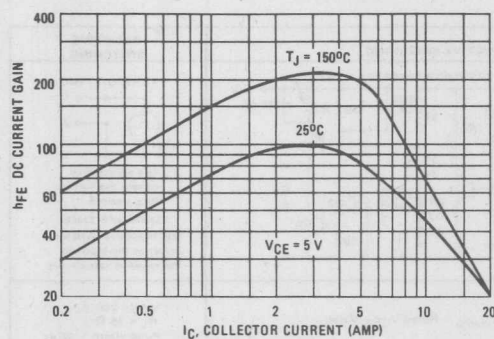


FIGURE 2 – COLLECTOR SATURATION REGION

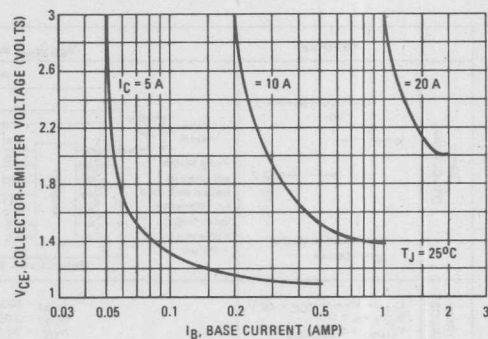


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

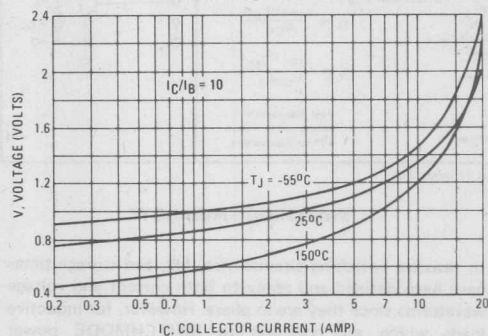


FIGURE 4 – BASE-EMITTER VOLTAGE

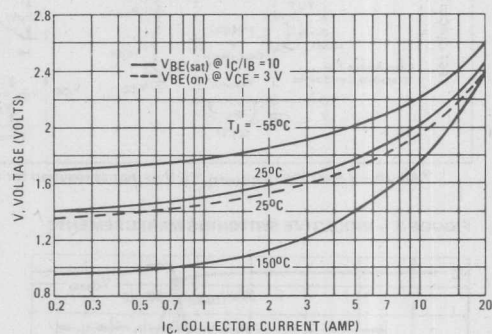


FIGURE 5 – COLLECTOR CUTOFF REGION

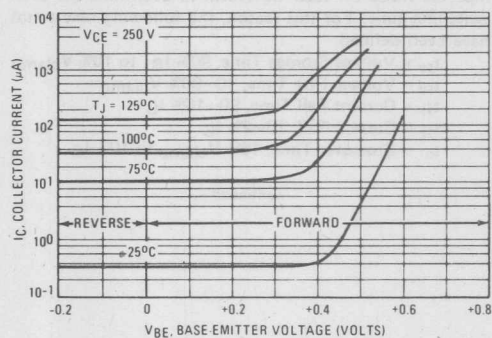


FIGURE 6 – OUTPUT CAPACITANCE

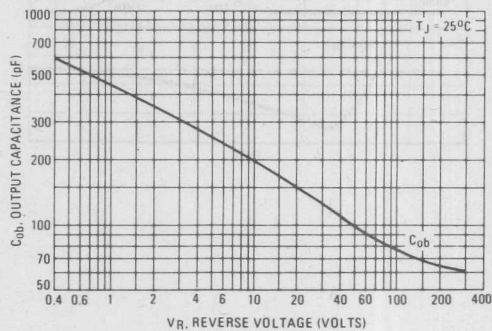
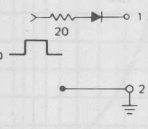
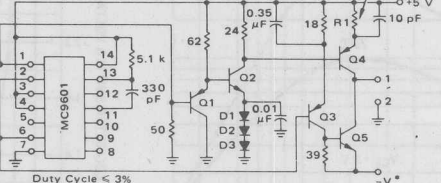
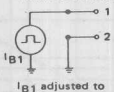
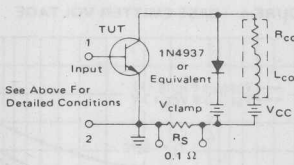
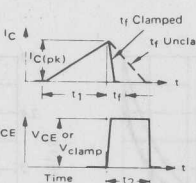
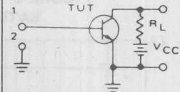
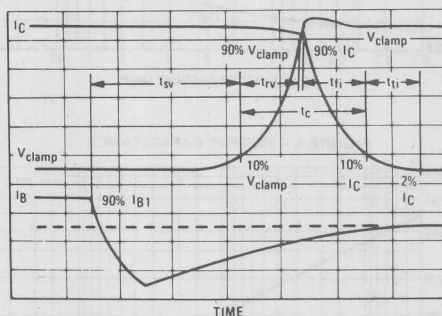


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

V _{CEO(sus)}	V _{CEX(sus)} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS  PW Varied to Attain $I_C = 100 \text{ mA}$	Adjust R1 to obtain a forced $h_{FE} = 20$  Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 25 µs) Duty Cycle ≤ 3%	RESISTIVE SWITCHING  TURN-ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES $L_{coil} = 10 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CEO(sus)}$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = \text{Rated } V_{CEX} \text{ Value}$	$V_{CC} = 250 \text{ V}$ $R_L = 25 \Omega$ Pulse Width = 25 µs
TEST CIRCUITS INDUCTIVE TEST CIRCUIT  See Above For Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 = \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 = \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$ Test Equipment - Scope - Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

*Adjust -V such that $V_{BE(off)} = 5 \text{ V}$ except as required for RB SOA (Figure 12).

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

— continued —

TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

Typical inductive switching waveforms are shown in Figure 7. In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at $T_C = 25^\circ\text{C}$ and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at $T_C = 100^\circ\text{C}$.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

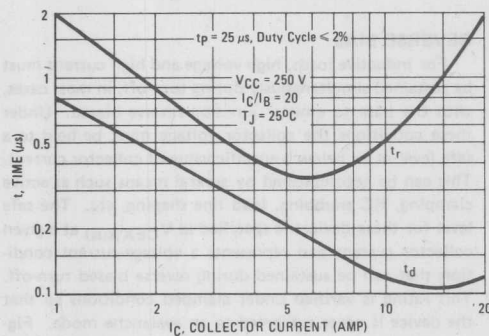


FIGURE 9 – TURN-OFF TIME

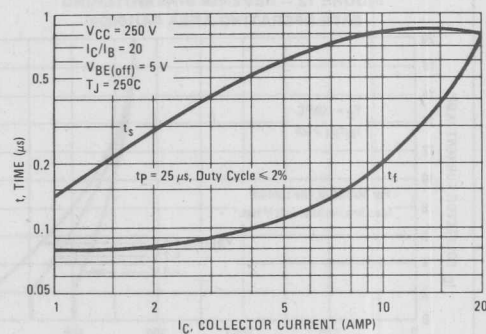
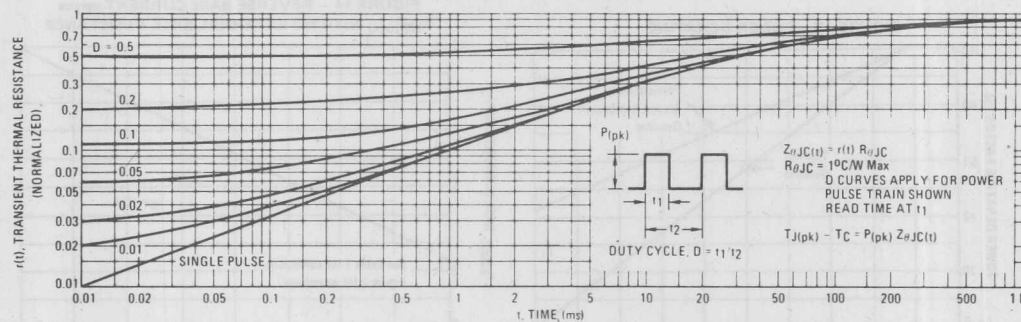


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATING AREA

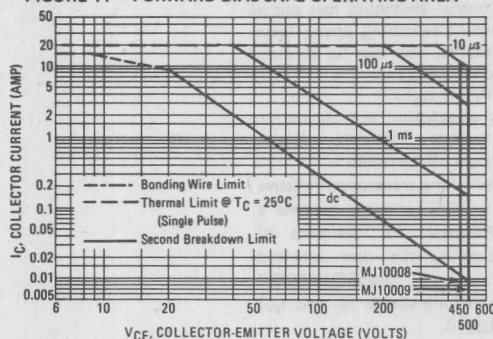


FIGURE 12 — REVERSE BIAS SWITCHING SAFE OPERATING AREA (MJ10009)

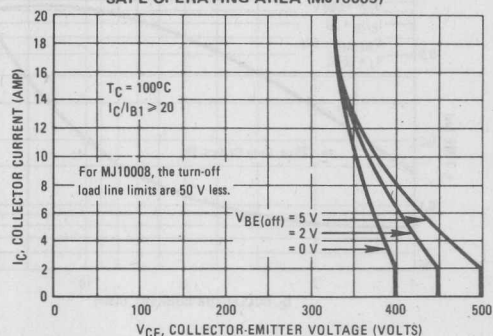
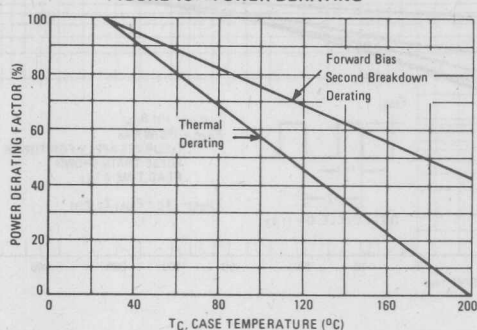


FIGURE 13 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

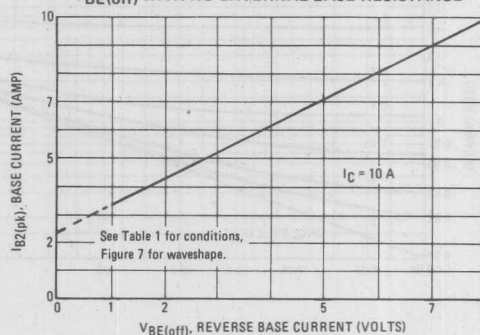
The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX}(\text{sus})$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics. See Table 1 for circuit conditions.

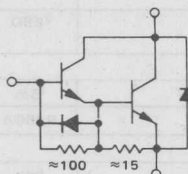
FIGURE 14 — REVERSE BASE CURRENT versus $V_{BE}(\text{off})$ WITH NO EXTERNAL BASE RESISTANCE



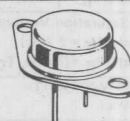
**MOTOROLA****MJ10013
MJ10014****Designers Data Sheet****SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS**

The MJ10013 and MJ10014 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 250 ns Inductive Fall Time—25°C (Typ)
 - 500 ns Inductive Crossover Time—25°C (Typ)
 - 1.4 μ s Inductive Storage Time—25°C (Typ)
- Operating Temperature Range: -65 to +200°C
- 100°C Performance Specified for:
 - Reversed Biased SOA With Inductive Loads
 - Switching Times With Inductive Loads
 - Saturation Voltages
 - Leakage Currents


**10 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS**
**550 AND 600 VOLTS
175 WATTS**
**Designers Data for
"Worst-Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristic boundaries—are given to facilitate "worst-case" design.

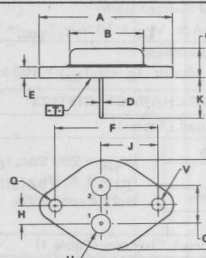
**MAXIMUM RATINGS**

Rating	Symbol	MJ10013	MJ10014	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	550	600	Vdc
Collector-Emitter Voltage	V_{CEV}	650	700	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous	I_C	10		Adc
— Peak (1)	I_{CM}	15		
Base Current — Continuous	I_B	7		Adc
— Peak (1)	I_{BM}	10		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175		Watts
@ $T_C = 100^\circ\text{C}$		100		
Derate above 25°C		1		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering	T_L	275	°C
Purposes: 1/8" from Case for 5 Seconds			

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
 2. \square IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
- FOR LEADS:
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	6.97	7.62	0.274	0.300
E	—	3.43	—	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.48 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	550 600	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^{\circ}\text{C}$)	I_{CEV}	— —	— —	0.3 5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^{\circ}\text{C}$)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current ($V_{EB} = 2\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (2)					
DC Current Gain ($I_C = 5\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	20 10	— —	500 250	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^{\circ}\text{C}$)	$V_{CE(sat)}$	— —	— —	2.5 2.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^{\circ}\text{C}$)	$V_{BE(sat)}$	— —	— —	3 3	Vdc
Diode Forward Voltage (1) ($I_F = 10\text{ Adc}$)	V_f	—	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 1\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1\text{ MHz}$)	$ h_{fe} $	10	—	—	—
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ kHz}$)	C_{ob}	100	—	350	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{B1} = 1\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2\%$)	t_d	—	0.02	0.2 μs
Rise Time		t_r	—	0.9	2 μs
Storage Time		t_s	—	0.95	4 μs
Fall Time		t_f	—	0.22	1 μs
Inductive Load, Clamped (Table 1)					
Storage Time	$(I_C = 10\text{ A(pk)}$, $V_{clamp} = 250\text{ Vdc}$, $I_{B1} = 1\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^{\circ}\text{C}$)	t_s	—	2.3	6 μs
Crossover Time		t_c	—	1	3 μs
Storage Time	$(I_C = 10\text{ A(pk)}$, $V_{clamp} = 250\text{ Vdc}$, $I_{B1} = 1\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 25^{\circ}\text{C}$)	t_s	—	1.4	— μs
Crossover Time		t_c	—	0.5	— μs
Fall Time		t_{fi}	—	0.25	— μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads.

Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs , Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

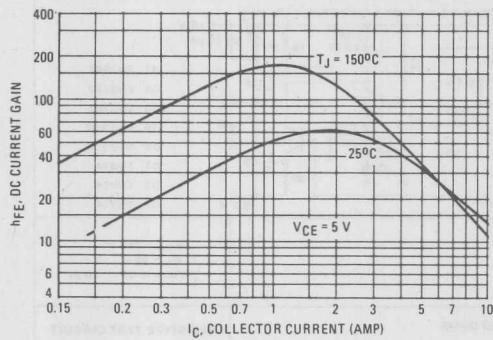


FIGURE 2 – COLLECTOR SATURATION REGION

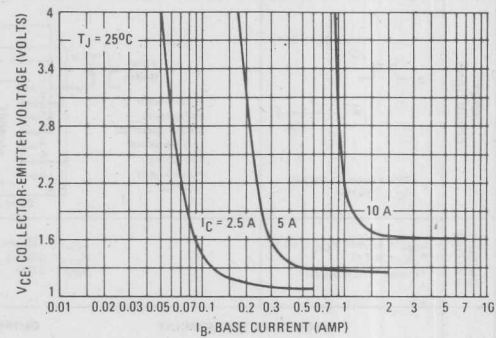


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

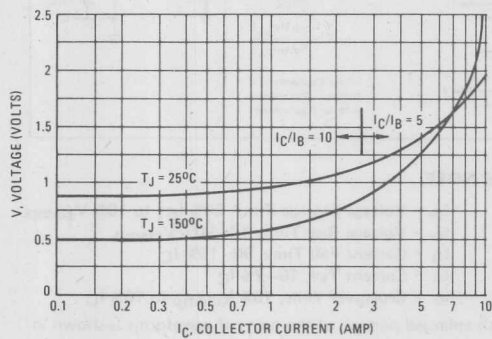


FIGURE 4 – BASE-EMITTER VOLTAGE

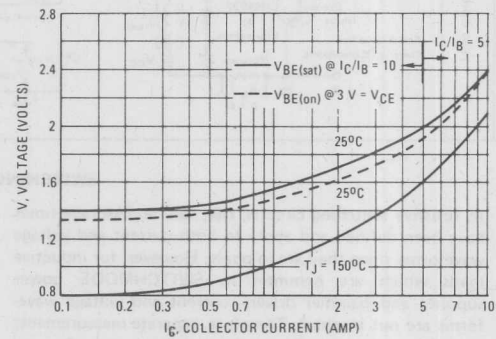


FIGURE 5 – COLLECTOR CUTOFF REGION

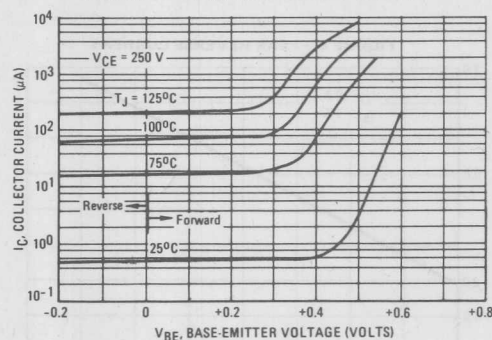


FIGURE 6 – OUTPUT CAPACITANCE

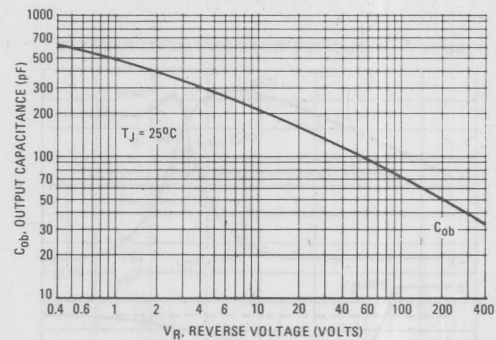


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CE0}(sus)$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain $I_C = 250\text{ mA}$</p>	<p>Adjust R_1 to obtain a forced $h_{FE} = 10$</p> <p>Duty Cycle $< 3\%$</p>	
CIRCUIT VALUES	$L_{coil} = 10\text{ mH}$ $R_{coil} = 0.7\ \Omega$ $V_{clamp} = V_{CE0}(sus)$	$L_{coil} = 180\ \mu\text{H}$ $R_{coil} = 0.05\ \Omega$ $V_{CC} = 20\text{ V}$	$V_{CC} = 250\text{ V}$ $R_L = 25\ \Omega$ Pulse Width $= 50\ \mu\text{s}$
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT <p>See Above for Detailed Conditions</p>	OUTPUT WAVEFORMS 	RESISTIVE TEST CIRCUIT

SWITCHING TIME NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
 t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
 t_{fi} = Current Fall Time, 90–10% I_C
 t_{ti} = Current Tail, 10–2% I_C
 t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

— continued —

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

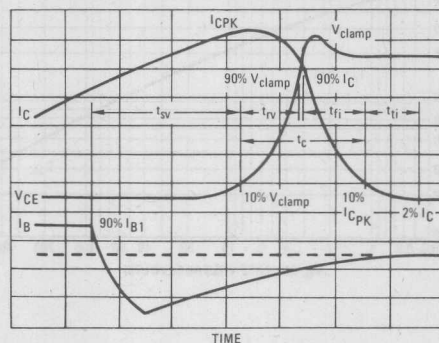
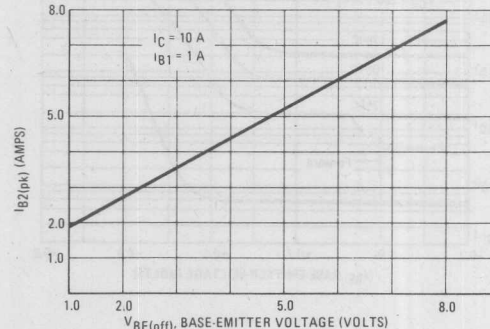


FIGURE 8 – PEAK REVERSE CURRENT



TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON TIME

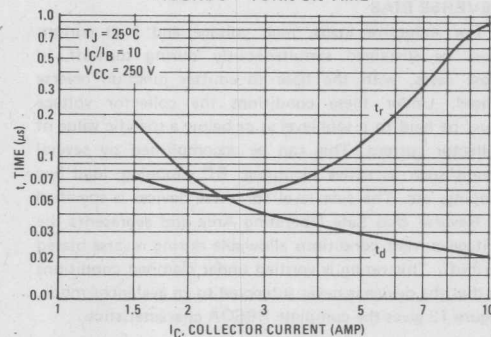


FIGURE 10 – TURN-OFF TIME

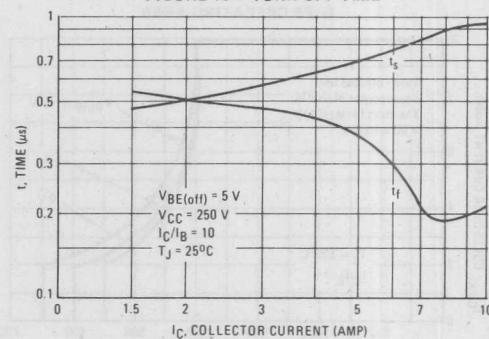
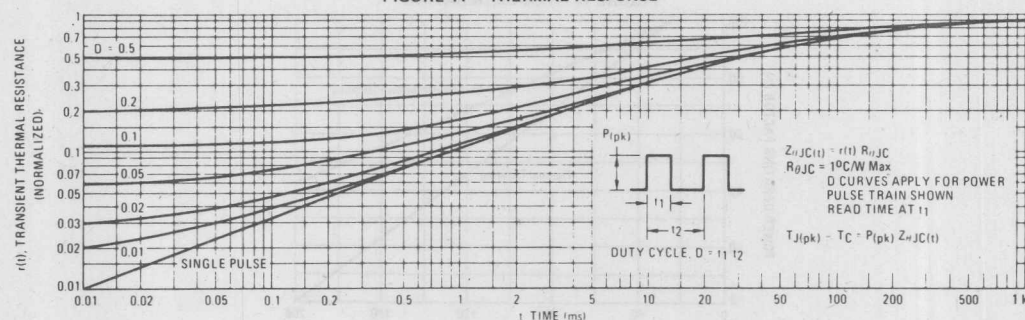


FIGURE 11 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

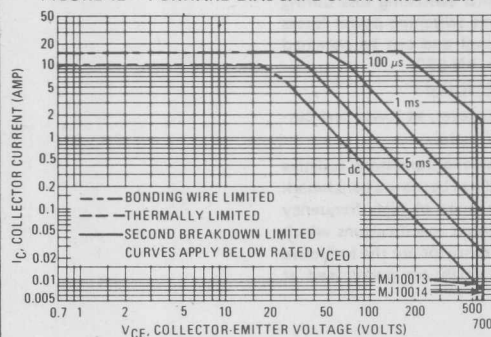
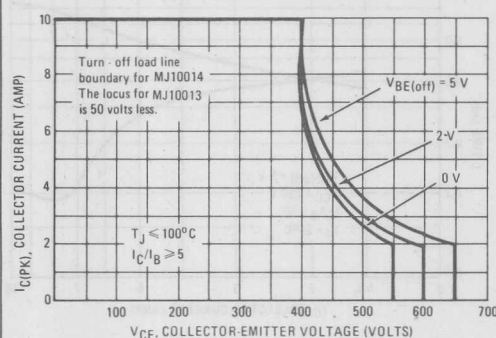


FIGURE 13 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

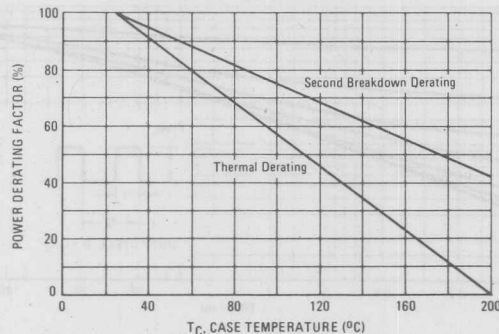
The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 — POWER DERATING



**MOTOROLA****MJ10015
MJ10016**

SWITCHMODE SERIES NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10015 and MJ10016 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Motor Controls
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 1.0 μ s (max) Inductive Crossover Time – 20 Amps
 - 2.5 μ s (max) Inductive Storage Time – 20 Amps
- Operating Temperature Range –65 to +200°C
- Performance Specified for
 - Reversed Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	MJ10015	MJ10016	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	400	500	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current – Continuous	I_C	50		Adc
– Peak (1)	I_{CM}	75		
Base Current – Continuous	I_B	10		Adc
– Peak (1)	I_{BM}	15		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250		Watts
@ $T_C = 100^\circ\text{C}$		143		
Derate above 25°C		1.43		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

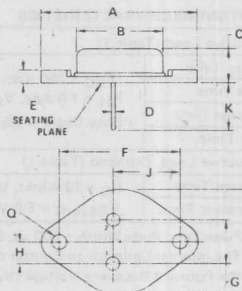
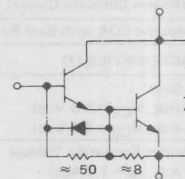
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%

50 AMPERE

NPN SILICON POWER DARLINGTON TRANSISTORS

**400 and 500 VOLTS
250 WATTS**



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E		3.43		0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	$V_{\text{CEO(sus)}}$	400 500	—	—	Vdc
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$)	I_{CEV}	—	—	0.25	mA _{dc}
Emitter Cutoff Current ($V_{\text{EB}} = 2.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	350	mA _{dc}

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{\text{S/b}}$	See Figure 7			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 8			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 20\text{ A}$ dc, $V_{\text{CE}} = 5.0\text{ Vdc}$) ($I_C = 40\text{ A}$ dc, $V_{\text{CE}} = 5.0\text{ Vdc}$)	h_{FE}	25 10	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 20\text{ A}$ dc, $I_B = 1.0\text{ A}$ dc) ($I_C = 50\text{ A}$ dc, $I_B = 10\text{ A}$ dc)	$V_{\text{CE(sat)}}$	—	—	2.2 5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 20\text{ A}$ dc, $I_B = 1.0\text{ A}$ dc)	$V_{\text{BE(sat)}}$	—	—	2.75	Vdc
Diode Forward Voltage (2) ($I_F = 20\text{ A}$ dc)	V_f	—	2.5	5.0	Vdc

DYNAMIC CHARACTERISTIC

Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	—	—	750	pF
--	-----------------	---	---	-----	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 250 Vdc, I _C = 20 A, I _{B1} = 1.0 Adc, V _{BE(off)} = 5 Vdc, t _p = 25 μs Duty Cycle ≤ 2%).	t _d	—	0.14	0.3	μs
Rise Time		t _r	—	0.3	1.0	μs
Storage Time		t _s	—	0.8	2.5	μs
Fall Time		t _f	—	0.3	1.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I _C = 20 A(pk), V _{clamp} = 250 V, I _{B1} = 1.0 A, V _{BE(off)} = 5.0 Vdc)	t _{sv}	—	1.0	2.5	μs
Crossover Time		t _c	—	0.36	1.0	μs

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.(2) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

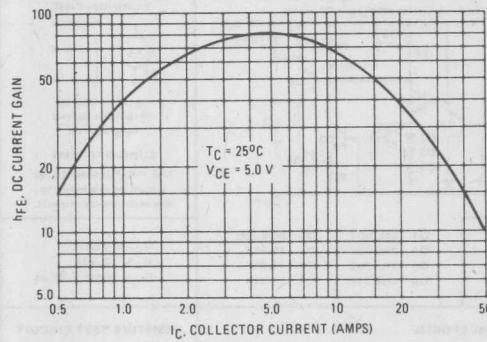


FIGURE 2 – COLLECTOR-EMITTER SATURATION VOLTAGE

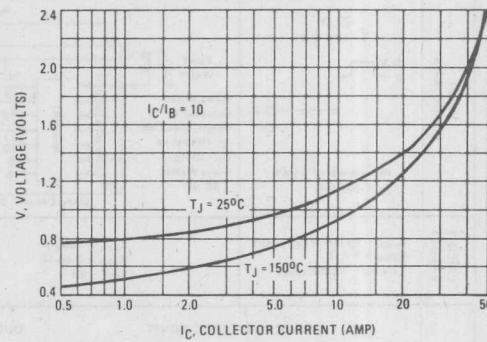


FIGURE 3 – BASE-EMITTER SATURATION VOLTAGE

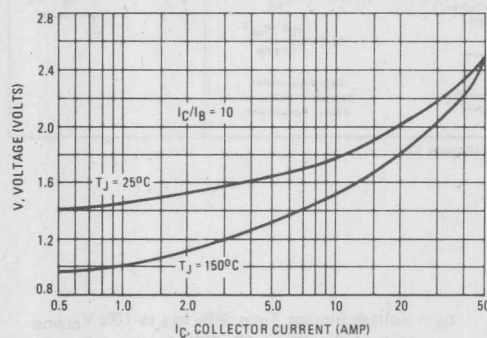


FIGURE 4 – COLLECTOR CUTOFF REGION

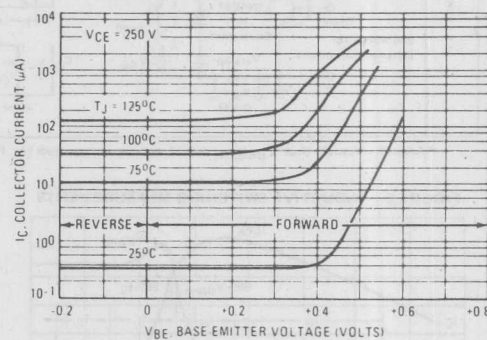


FIGURE 5 – OUTPUT CAPACITANCE

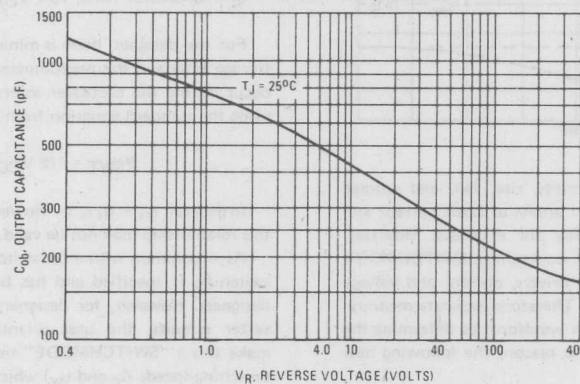
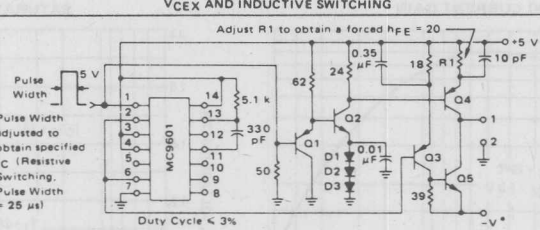
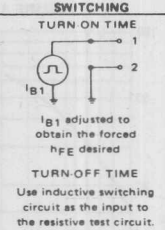
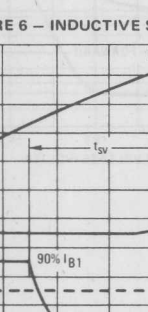
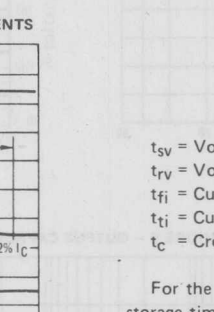
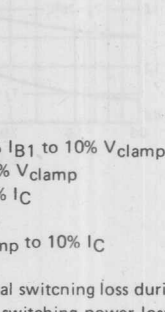
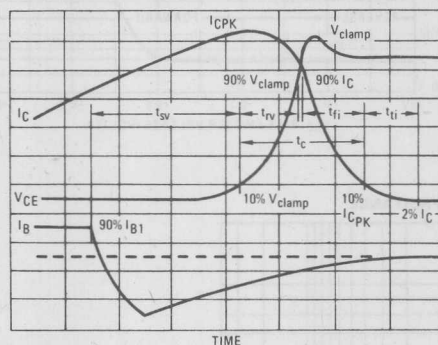


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

INPUT CONDITIONS	V _{CE0(sus)}	V _{CEX} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
CIRCUIT VALUES	$L_{coil} = 10 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CE0(sus)}$		
		L _{coil} = 180 μH R _{coil} = 0.05 Ω V _{CC} = 20 V	V _{CC} = 250 V R _L = 12.5 Ω Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT	OUTPUT WAVEFORMS	RESISTIVE TEST CIRCUIT
			

*Adjust -V such that $V_{BE(off)} = 5 \text{ V}$ except as required for RB SOA (Figure 12).

FIGURE 6 — INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
 t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
 t_{fi} = Current Fall Time, 90–10% I_C
 t_{ti} = Current Tail, 10–2% I_C
 t_c = Crossover Time, 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed.

The Safe Operating Area figures shown in Figures 7 and 8 are specified ratings for these devices under the test conditions shown.

FIGURE 7 – FORWARD BIAS SAFE OPERATING AREA

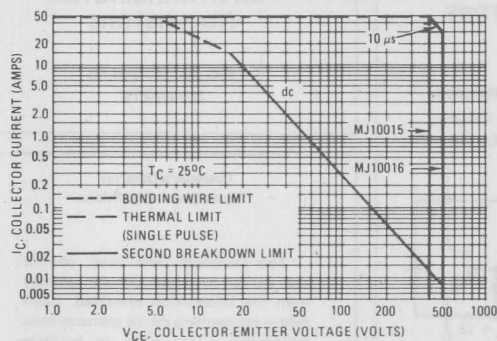


FIGURE 8 – REVERSE BIAS SWITCHING SAFE OPERATING AREA

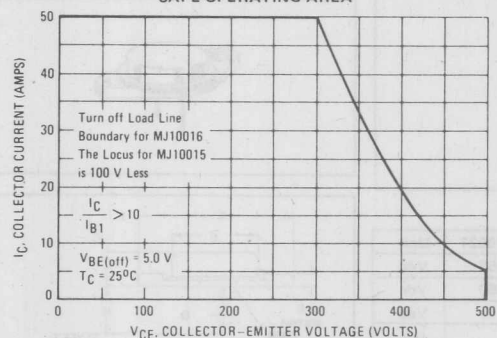
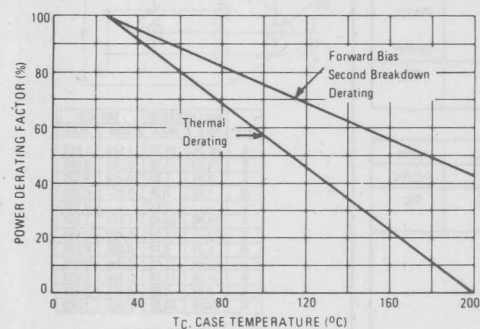


FIGURE 9 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

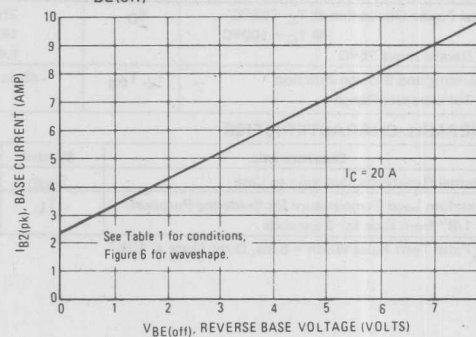
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the complete RBSOA characteristics.

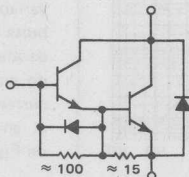
FIGURE 10 – TYPICAL REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



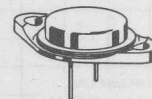
**MOTOROLA****MJ10020
MJ10021****Designers Data Sheet****SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE**

The MJ10020 and MJ10021 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 150 ns Inductive Fall Time at 25°C (Typ)
 - 750 ns Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
 - Reversed Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

**60 AMPERE****NPN SILICON
POWER DARLINGTON
TRANSISTORS****200 and 250 VOLTS
250 WATTS****Designer's Data for
"Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

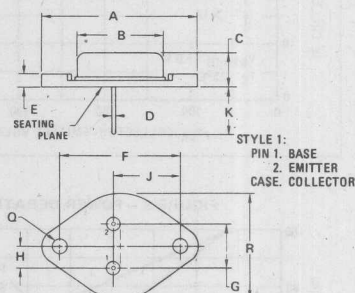
**MAXIMUM RATINGS**

Rating	Symbol	MJ10020	MJ10021	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	200	250	Vdc
Collector-Emitter Voltage	V_{CEV}	300	350	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous	I_C	60		Adc
Collector Current — Peak (1)	I_{CM}	100		Adc
Base Current — Continuous	I_B	20		Adc
Base Current — Peak (1)	I_{BM}	30		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	P_D	250 143		Watts
Derate above 25°C		1.43		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

**CASE 197-01
MODIFIED TO-3**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ10020 MJ10021 $V_{CEO(sus)}$	200 250	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$)	I_{CEV}	—	—	0.25	mAdc
($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)		—	—	5.0	
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 15\text{ Adc}$, $V_{CE} = 5.0\text{ V}$)	h_{FE}	75	—	1000	—
Collector-Emitter Saturation Voltage ($I_C = 30\text{ Adc}$, $I_B = 1.2\text{ Adc}$)	$V_{CE(sat)}$	—	—	2.2	Vdc
($I_C = 60\text{ Adc}$, $I_B = 4.0\text{ Adc}$)		—	—	4.0	
($I_C = 30\text{ Adc}$, $I_B = 1.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)		—	—	2.4	
Base-Emitter Saturation Voltage ($I_C = 30\text{ Adc}$, $I_B = 1.2\text{ Adc}$)	$V_{BE(sat)}$	—	—	3.0	Vdc
($I_C = 30\text{ Adc}$, $I_B = 1.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)		—	—	3.5	
Diode Forward Voltage ($I_F = 30\text{ Adc}$)	V_f	—	2.5	5.0	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	175	—	700	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 175 Vdc, I _C = 30 A, I _{B1} = 1.0 Adc, V _{BE(off)} = 5.0 V, t _p = 25 μs Duty Cycle ≤ 2.0%).	t _d	—	0.02	0.2	μs
Rise Time		t _r	—	0.30	1.0	μs
Storage Time		t _s	—	1.0	3.5	μs
Fall Time		t _f	—	0.07	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I _{CM} = 30 A(pk), V _{CEM} = 200 V, I _{B1} = 1.2 A, V _{BE(off)} = 5 V, T _C = 100°C)	t _{sv}	—	1.2	3.5	μs
Crossover Time		t _c	—	0.45	2.0	μs
Storage Time	(I _{CM} = 30 A(pk), V _{CEM} = 200 V, I _{B1} = 1.2 A, V _{BE(off)} = 5 V, T _C = 25°C)	t _{sv}	—	0.75	—	μs
Crossover Time		t _c	—	0.25	—	μs
Fall Time		t _{fj}	—	0.15	—	μs

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

FIGURE 1 — DC CURRENT GAIN

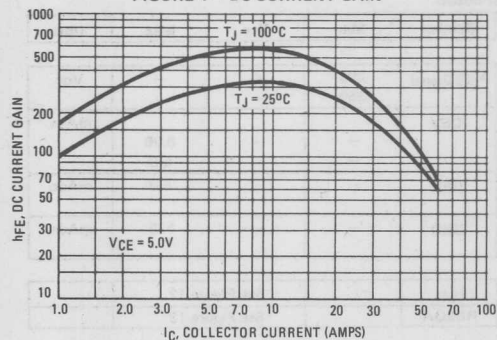


FIGURE 2 — COLLECTOR SATURATION REGION

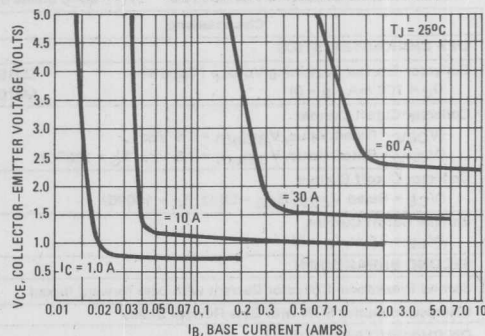


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

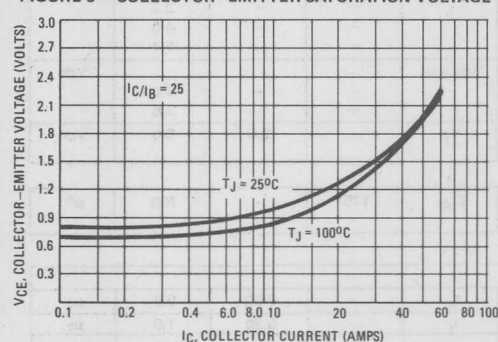


FIGURE 4 — BASE-EMITTER VOLTAGE

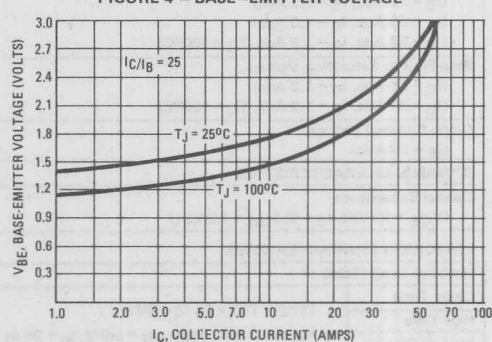


FIGURE 5 — COLLECTOR CUTOFF REGION

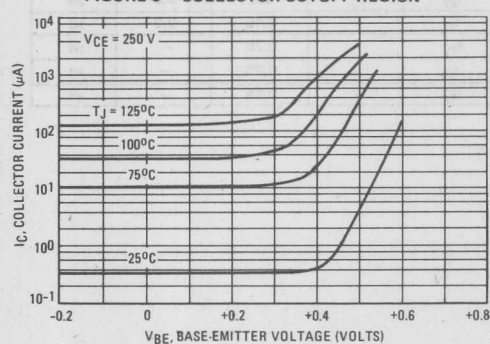


FIGURE 6 — OUTPUT CAPACITANCE

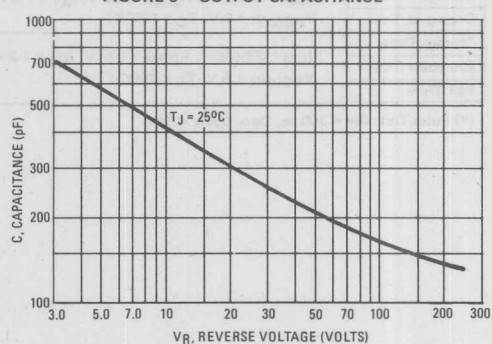


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	<p>$V_{CE(sus)}$</p> <p>PW Varied to Attain $I_C = 100$ mA</p>	<p>RBSOA AND INDUCTIVE SWITCHING</p> <p>Adjust R1 to obtain a forced $h_{FE} = 30$</p> <p>Duty Cycle < 3%</p>		<p>RESISTIVE SWITCHING</p> <p>TURN ON TIME</p> <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN-OFF TIME</p> <p>Use inductive switching circuit as the input to the resistive test circuit.</p>
<p>INPUT CONDITIONS</p>				
<p>CIRCUIT VALUES</p>	<p>$L_{coil} = 10$ mH $V_{CC} = 10$ V $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CE(sus)}$</p>	<p>$L_{coil} = 180 \mu H$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20$ V</p>	<p>Q1 2N2907 Q5 MJE15028 Q2 2N2222 D1 1N914 Q3 2N3762 D2 1N914 Q4 MJE15029 D3 1N914</p>	<p>$V_{CC} = 175$ V $R_L = 5.6 \Omega$ Pulse Width = 25 μs</p>
<p>TEST CIRCUITS</p>	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$</p> <p>$t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$</p> <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>	

*Adjust — V such that $V_{BE(off)} = 5$ V except as required for RBSOA (Figure 14).

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

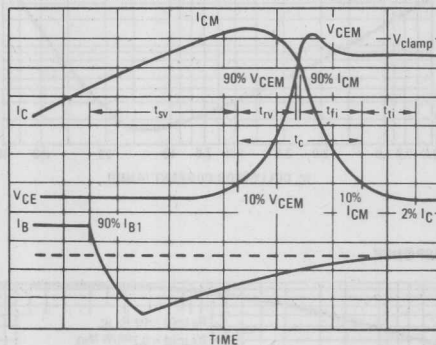


FIGURE 8 — PEAK REVERSE BASE CURRENT

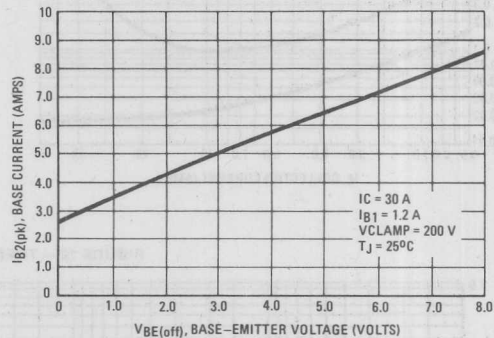
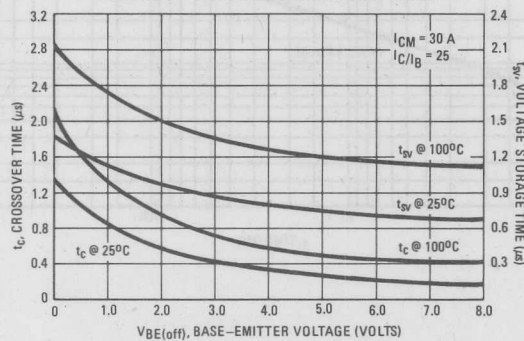


FIGURE 9 — INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{rv} = Voltage Rise Time, 10 — 90% V_{CEM}

t_{fi} = Current Fall Time, 90 — 10% I_{CM}

t_{ti} = Current Tail, 10 — 2% I_{CM}

t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

FIGURE 10 — TURN-ON SWITCHING TIMES

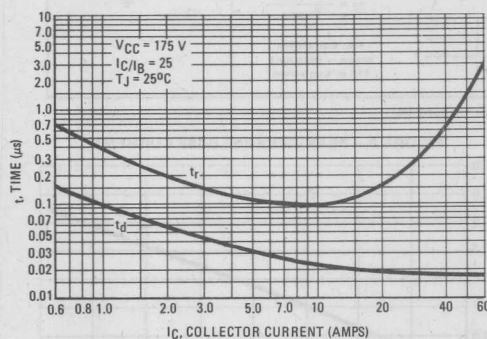


FIGURE 11 — TURN-OFF SWITCHING TIMES

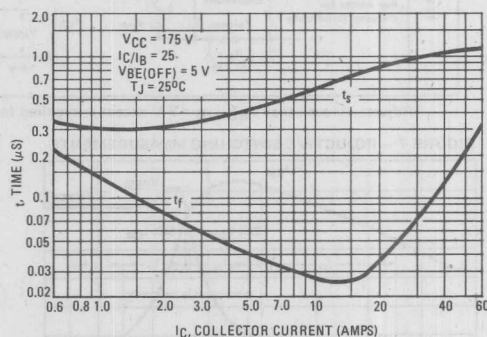
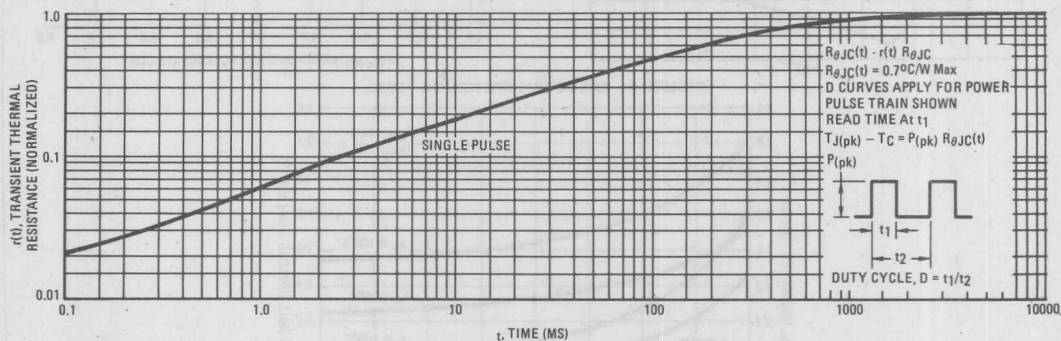


FIGURE 12 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 13 — FORWARD BIAS SAFE OPERATING AREA

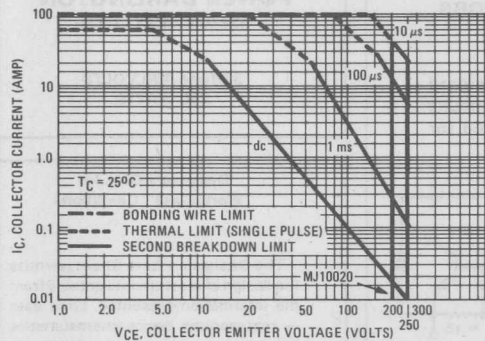
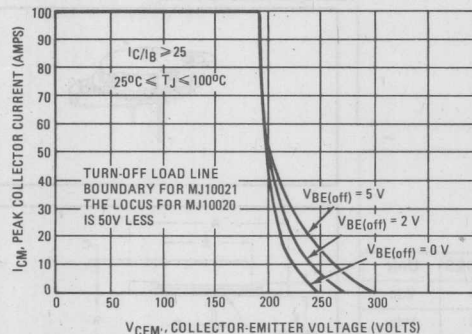


FIGURE 14 — RBSOA, REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

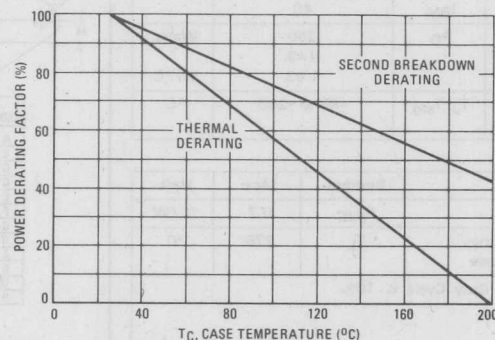
The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

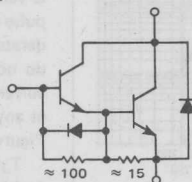
FIGURE 15 — POWER DERATING



**MJ10023**

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

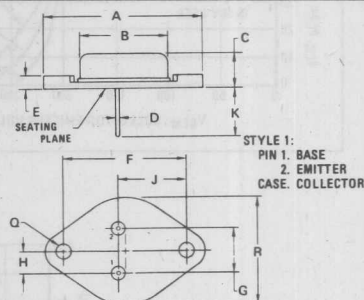


Rating	Symbol	MJ10022	MJ10023	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	450	600	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous	I_C	40		Adc
— Peak (1)	I_{CM}	80		
Base Current — Continuous	I_B	20		Adc
— Peak (1)	I_{BM}	40		
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	250		Watts
@ $T_C = 100^\circ C$		143		
Derate above $25^\circ C$		1.43		W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ C$

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

**NPN SILICON
POWER DARLINGTON
TRANSISTORS**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.198
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
L	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ10022 MJ10023 $V_{CEO(sus)}$	350 400	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 13	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 14	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10\text{ Adc}$, $V_{CE} = 5.0\text{ V}$)	h_{FE}	50	—	600	—
Collector-Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 40\text{ Adc}$, $I_B = 5.0\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.2 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 1.2\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 1.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage ($I_F = 20\text{ Adc}$)	V_f	—	2.5	5.0	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	150	—	600	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$V_{CC} = 250\text{ Vdc}$, $I_C = 20\text{ A}$, $I_{B1} = 1.0\text{ Adc}$, $V_{BE(off)} = 5.0\text{ V}$, $t_p = 50\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.03	0.2	μs
Rise Time		t_r	—	0.4	1.2	μs
Storage Time		t_s	—	0.9	2.5	μs
Fall Time		t_f	—	0.3	0.9	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$I_{CM} = 20\text{ A}$, $V_{CEM} = 250\text{ V}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	1.9	4.4	μs
Crossover Time		t_c	—	0.6	2.0	μs
Fall Time		t_{fi}	—	0.3	—	μs
Storage Time	$I_{CM} = 20\text{ A}$, $V_{CEM} = 250\text{ V}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $T_C = 25^\circ\text{C}$)	t_{sv}	—	1.0	—	μs
Crossover Time		t_c	—	0.3	—	μs
Fall Time		t_{fi}	—	0.15	—	μs

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

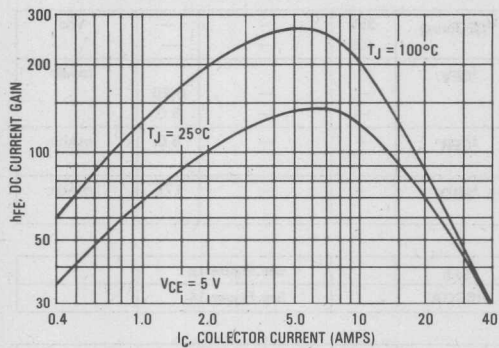


FIGURE 2 — COLLECTOR SATURATION REGION

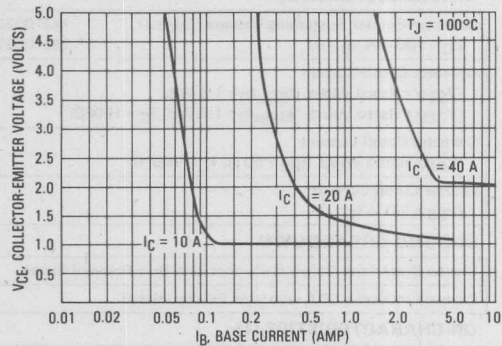


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

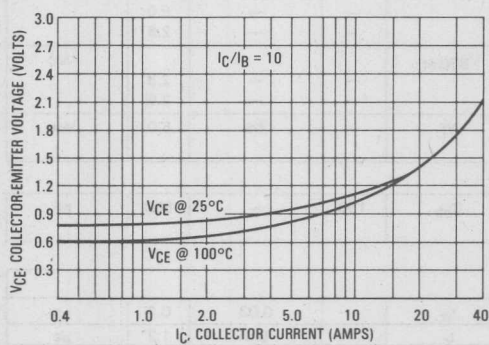


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

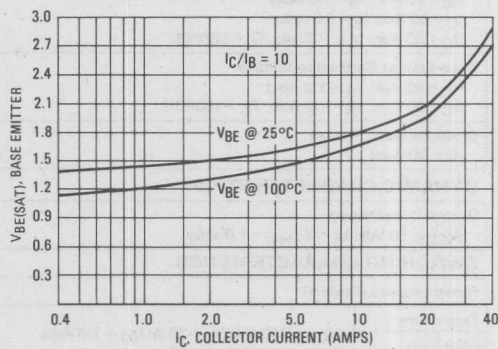


FIGURE 5 — COLLECTOR CUTOFF REGION

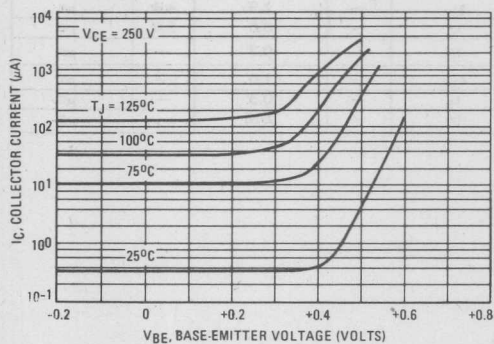
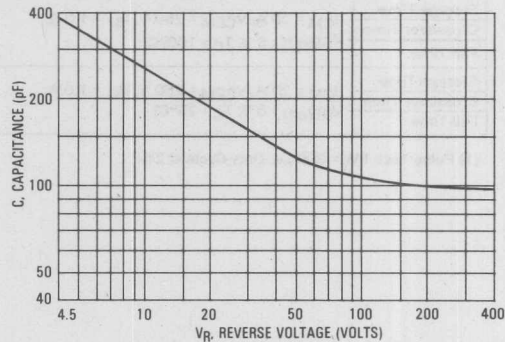
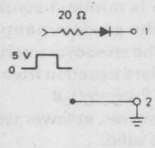
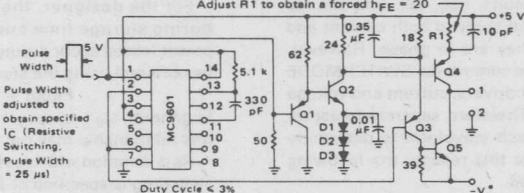
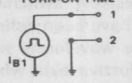
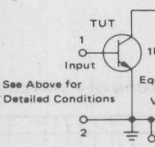
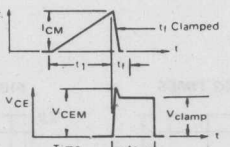
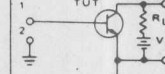
FIGURE 6 — C_{ob} OUTPUT CAPACITANCE

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO}(sus)$	RBSOA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 100\text{ mA}$</p>	 <p>Adjust R1 to obtain a forced $h_{FE} = 20$</p> <p>Duty Cycle $\leq 3\%$</p>		 <p>TURN-ON TIME</p> <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN-OFF TIME</p> <p>Use inductive switching circuit as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 10\text{ mH}$ $V_{CC} = 10\text{ V}$ $R_{coil} = 0.7\ \Omega$ $V_{clamp} = V_{CEO}(sus)$	$L_{coil} = 180\ \mu\text{H}$ $R_{coil} = 0.05\ \Omega$ $V_{CC} = 20\text{ V}$	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE15029	Q5 MJE15028 D1 1N914 D2 1N914 D3 1N914
TEST CIRCUITS	 <p>INDUCTIVE TEST CIRCUIT</p>	 <p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$</p> <p>$t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$</p> <p>Test Equipment Scope – Tektronix 475 or Equivalent</p>	 <p>RESISTIVE TEST CIRCUIT</p>	

*Adjust – V such that $V_{BE(off)} = 5\text{ V}$ except as required for RBSOA (Figure 14).

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

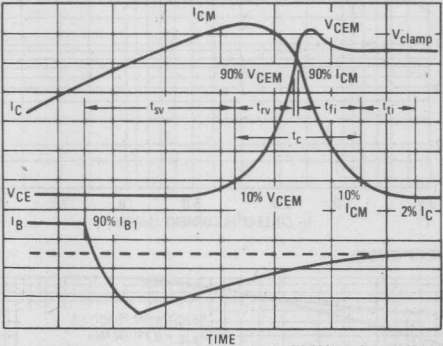


FIGURE 8 – TYPICAL PEAK REVERSE BASE CURRENT

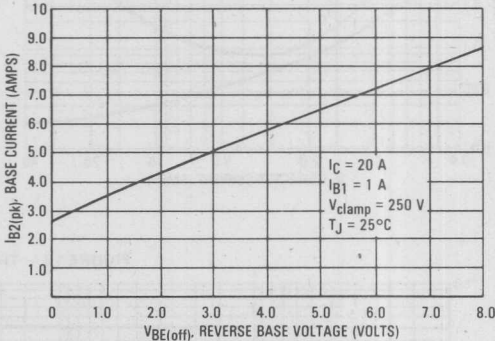
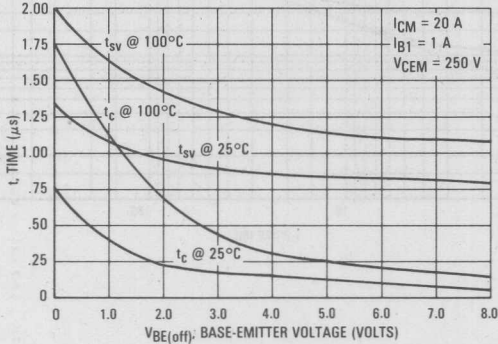


FIGURE 9 – TYPICAL INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{rV} = Voltage Rise Time, 10–90% V_{CEM}

t_{fi} = Current Fall Time, 90–10% I_{CM}

t_{ti} = Current Tail, 10–2% I_{CM}

t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rV} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{SV}) which are guaranteed at 100°C.

FIGURE 10 – TYPICAL TURN-ON SWITCHING TIMES

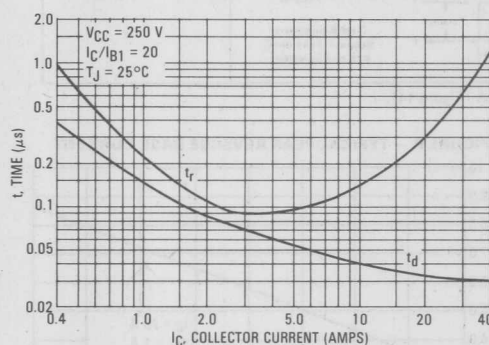


FIGURE 11 – TYPICAL TURN-OFF SWITCHING TIMES

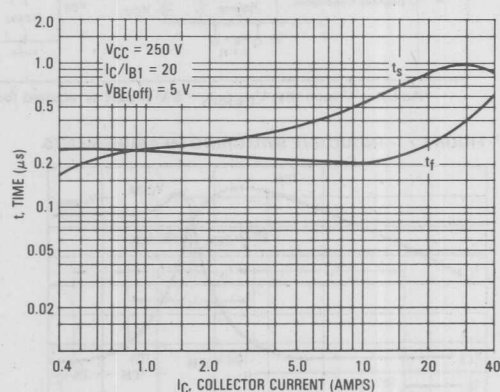
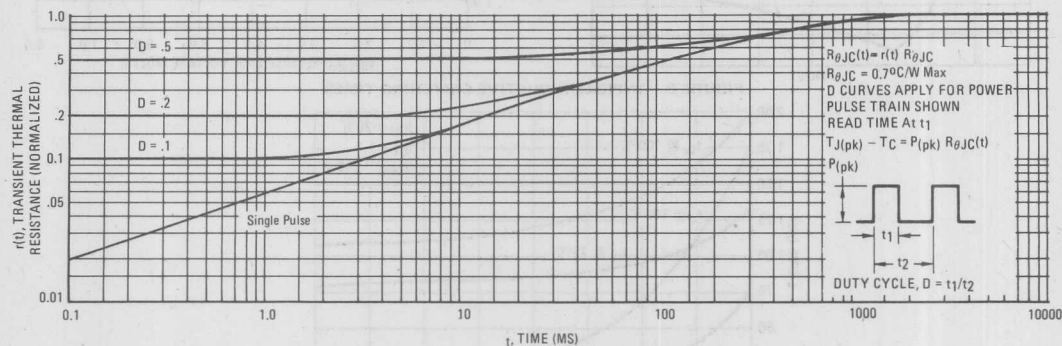


FIGURE 12 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 - MAXIMUM FORWARD BIAS
SAFE OPERATING AREA

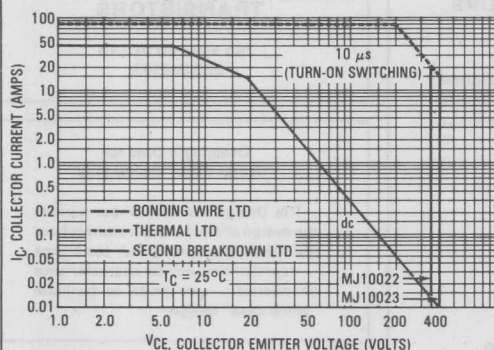
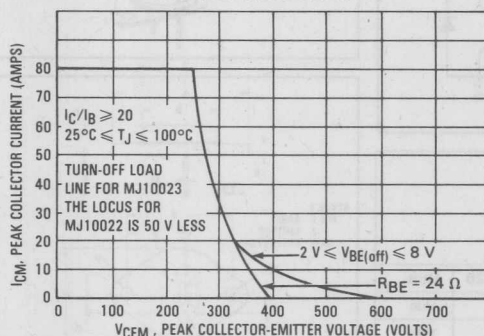


FIGURE 14 - MAXIMUM RBSOA, REVERSE BIAS
SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

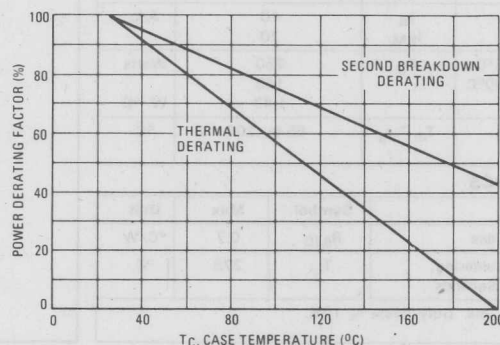
The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

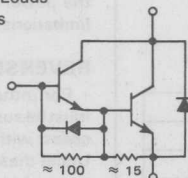
FIGURE 15 - POWER DERATING



**MOTOROLA****MJ10024
MJ10025****Designer's Data Sheet****SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE**

The MJ10024 and MJ10025 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
 - Reversed Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

**MAXIMUM RATINGS**

Rating	Symbol	MJ10024	MJ10025	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	750	850	Vdc
Collector-Emitter Voltage	V_{CEV}	1000	1200	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous	I_C	20		Adc
— Peak (1)	I_{CM}	40		
Base Current — Continuous	I_B	10		Adc
— Peak (1)	I_{BM}	20		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250		Watts
— @ $T_C = 100^\circ\text{C}$		143		
Derate above 25°C		1.43		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

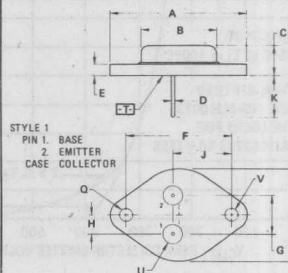
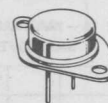
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

20 AMPERE**NPN SILICON
POWER DARLINGTON
TRANSISTORS****750 and 850 VOLTS
250 WATTS****Designer's Data for
"Worst Case" Conditions**

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
 2. \square IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$\phi \pm 0.13 (0.005) \text{ (M)} \text{ (T)} \text{ (V)} \text{ (W)}$

FOR LEADS:

$\phi \pm 0.13 (0.005) \text{ (M)} \text{ (T)} \text{ (V)} \text{ (W)} \text{ (Q)} \text{ (U)}$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	38.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	1.187 BSC		
G	10.92 BSC	0.430 BSC		
H	5.48 BSC	0.215 BSC		
J	16.80 BSC	0.665 BSC		
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ10024 MJ10025 $V_{CEO(sus)}$	750 850	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 14		
Clamped Inductive SOA with base reverse biased	RBSOA		See Figure 15		

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ V}$)	h_{FE}	50	—	600	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 5.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.2 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage ($I_F = 10\text{ Adc}$)	V_f	—	1.25	4.0	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	110	—	500	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$V_{CC} = 250\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{B1} = 1.0\text{ Adc}$, $V_{BE(off)} = 5.0\text{ V}$, $t_p = 50\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.03	0.3	μs
Rise Time		t_r	—	0.6	1.8	
Storage Time		t_s	—	2.0	5.0	
Fall Time		t_f	—	0.6	1.8	
Inductive Load, Clamped (Table 1)						
Storage Time	$I_{CM} = 10\text{ A}$, $V_{CEM} = 250\text{ V}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	2.9	7.0	μs
Crossover Time		t_c	—	1.0	3.3	
Storage Time	$I_{CM} = 10\text{ A}$, $V_{CEM} = 250\text{ V}$, $I_{B1} = 1.0\text{ A}$, $R_{BE} = 24\text{ }\Omega$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	21	50	μs
Crossover Time		t_c	—	9.0	25	
Storage Time	$I_{CM} = 10\text{ A}$, $V_{CEM} = 250\text{ V}$, $V_{BE(off)} = 5.0\text{ V}$, I_{B1} Baker Clamped [1 Ampere Source], $T_C = 100^\circ\text{C}$)	t_{sv}	—	2.2	—	μs
Crossover Time		t_c	—	0.5	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

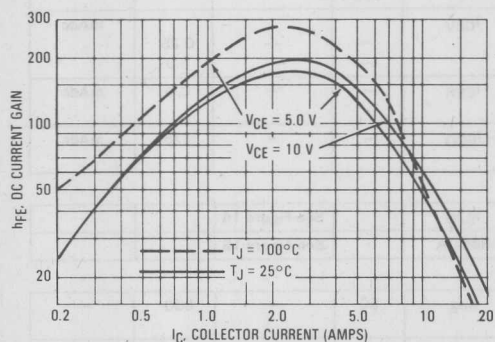


FIGURE 2 — COLLECTOR SATURATION REGION

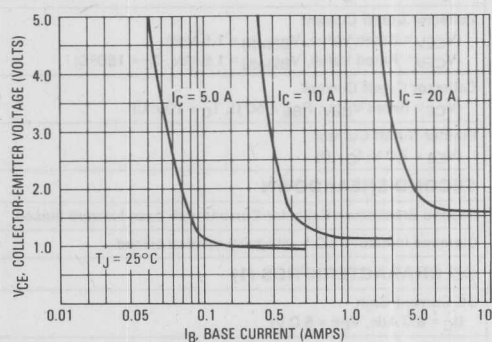


FIGURE 3 — COLLECTOR SATURATION VOLTAGE

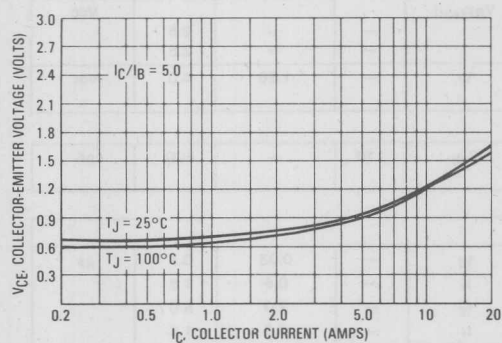


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

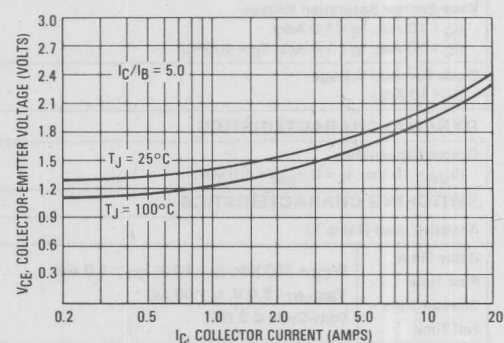


FIGURE 5 — COLLECTOR CUTOFF REGION

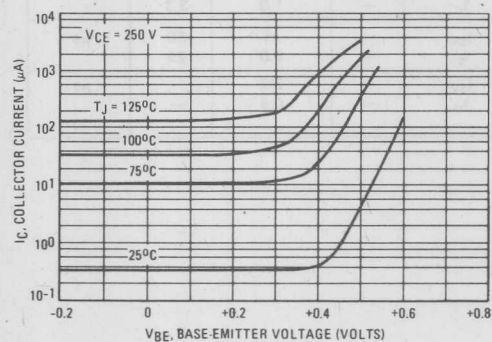
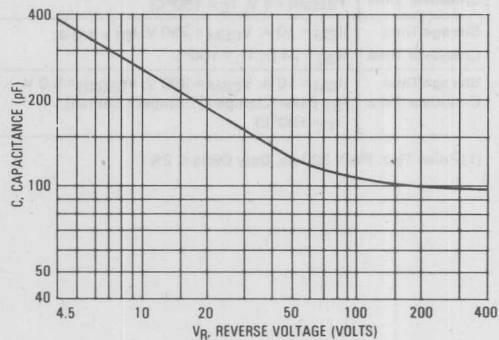
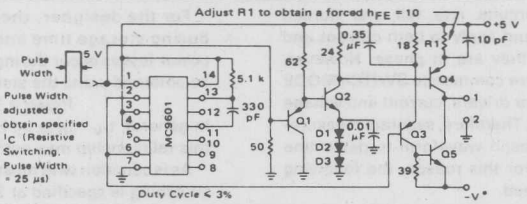
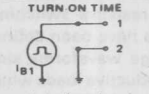
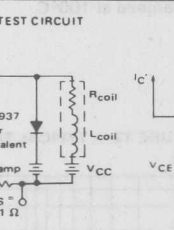
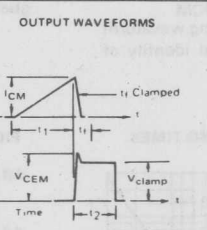
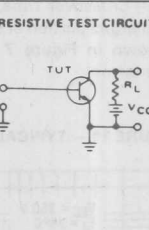
FIGURE 6 — C_{ob} , OUTPUT CAPACITANCE

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CE0(sus)}$	RESISTIVE SWITCHING
INPUT CONDITIONS	RBSOA AND INDUCTIVE SWITCHING Adjust R1 to obtain a forced $h_{FE} = 10$  Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 25 μs) Duty Cycle $\leq 3\%$	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching circuit as the input to the resistive test circuit.
CIRCUIT VALUES	$L_{coil} = 10 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CE0(sus)}$ $L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ Q1 2N2907 Q5 MJE15028 Q2 2N2222 D1 1N914 Q3 2N3762 D2 1N914 Q4 MJE15029 D3 1N914	$V_{CC} = 250 \text{ V}$ $R_L = 25 \Omega$ Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 = \frac{L_{coil} (I_{CM})}{V_{CC}}$ $t_2 = \frac{L_{coil} (I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

*Adjust — V such that $V_{BE(off)} = 5 \text{ V}$ except as required for RBSOA (Figure 14).

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

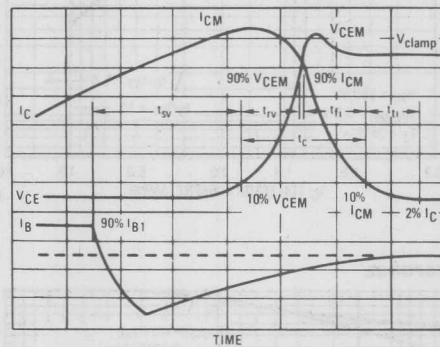


FIGURE 9 — TYPICAL INDUCTIVE SWITCHING TIMES

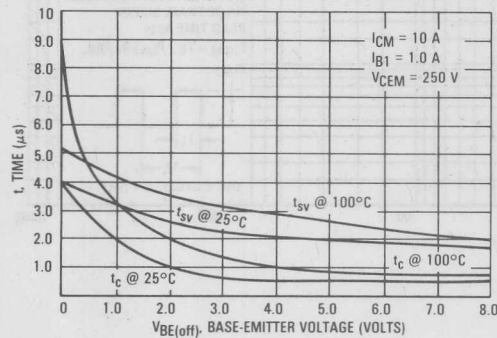


FIGURE 8 — TYPICAL PEAK REVERSE BASE CURRENT

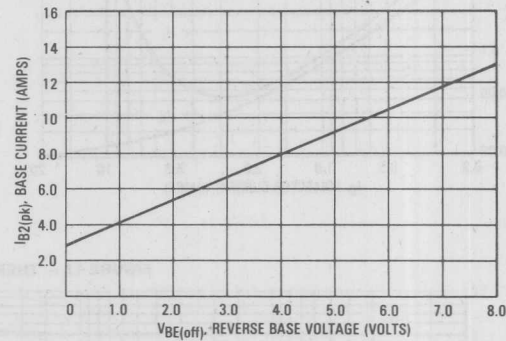
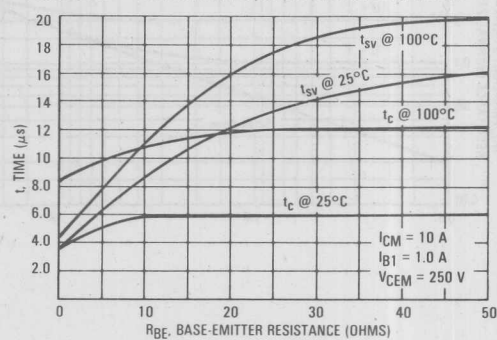


FIGURE 10 — TYPICAL INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{RV} = Voltage Rise Time, 10—90% V_{CEM}

t_{fi} = Current Fall Time, 90—10% I_{CM}

t_{ti} = Current Tail, 10—2% I_{CM}

t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{RV} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{SV}) which are guaranteed at 100°C.

FIGURE 11 — TYPICAL TURN-ON SWITCHING TIMES

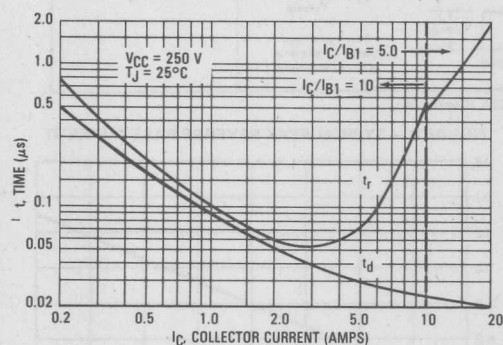


FIGURE 12 — TYPICAL TURN-OFF SWITCHING TIMES

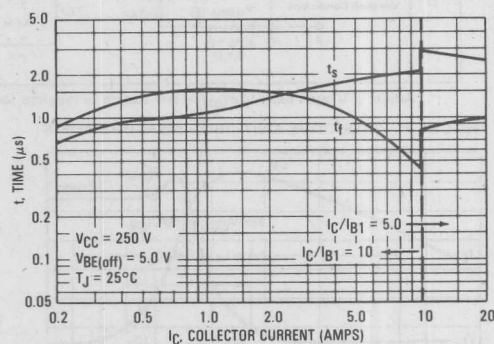
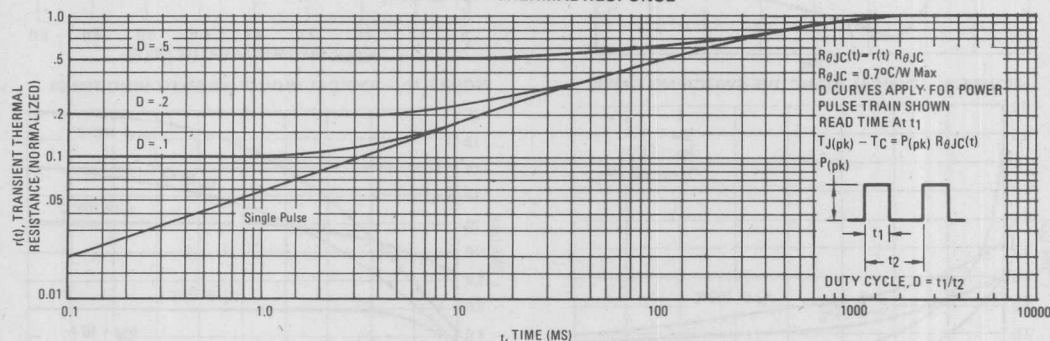


FIGURE 13 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 14 and 15 are specified for these devices under the test conditions shown.

FIGURE 14 — MAXIMUM FORWARD BIAS
SAFE OPERATING AREA

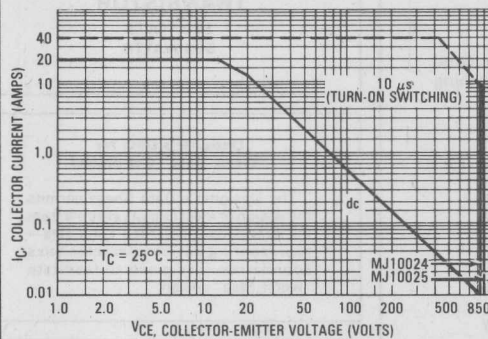
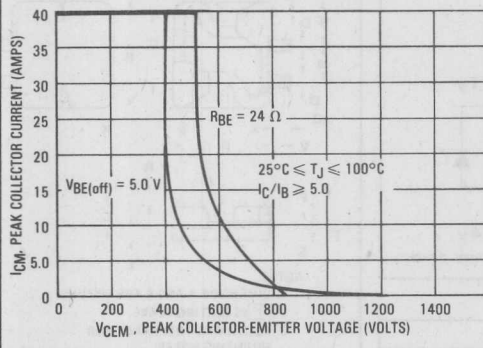


FIGURE 15 — MAXIMUM RBSOA, REVERSE BIAS
SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

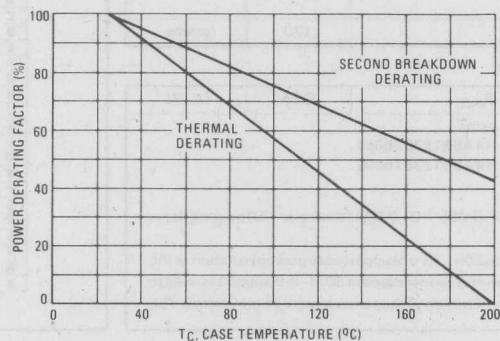
The data of Figure 14 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 14 may be found at any case temperature by using the appropriate curve on Figure 16.

$T_J(\text{pk})$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

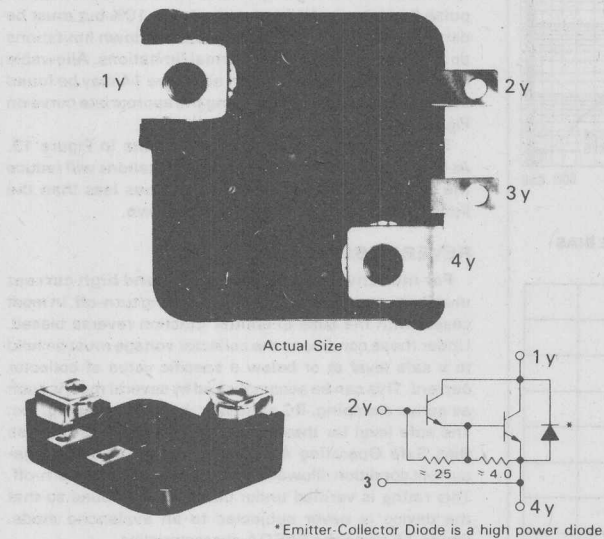
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

FIGURE 16 — POWER DERATING



**MOTOROLA****MJ10050****Designer's Data Sheet****50 KVA SWITCHMODE TRANSISTOR**
50-Ampere Operating Current

The MJ10050 Darlington transistor is designed for industrial service under practical operating environments found in switching high power inductive loads off 460-Volt lines.



*Emitter-Collector Diode is a high power diode.

MAXIMUM RATINGS**Mechanical Ratings**

Rating	Value	Unit
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	$^{\circ}\text{C}/\text{W}$
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Mica Insulators available as separate items.

0.003" thick, Motorola Part Number 14ASB12387B001.

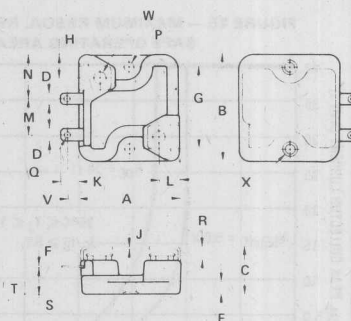
0.006" thick, Motorola Part Number 14ASB12387B002.

Notes:

1. A Belleville washer of 0.472" O.D., 0.205" I.D., 0.024" thick and 150 pounds flat is recommended.
2. The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75".

50 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
850 VOLTS
500 WATTS
Designer's Data for
"Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.

**NOTES:**

1. DIMENSION A AND B ARE DATUMS.
2. [T] IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:

$$\phi 0.36 (0.014) \text{ } \phi T A B$$

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C		26.67		1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31 BSC		1.705 BSC	
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01

MAXIMUM RATINGS (Continued)

Electrical Ratings				
Rating	Symbol	Value	Unit	
Collector-Emitter Voltage	V_{CEO}	850	Vdc	
Collector-Emitter Voltage ($R_{BE} = 10 \text{ Ohms}$)	V_{CER}	900	Vdc	
Collector-Base Voltage	V_{CB}	900	Vdc	
Emitter-Base Voltage	V_{EB}	8.0	Vdc	
Collector Current — Operating, $T_C = 125^\circ\text{C}$ — Continuous, $T_C = 25^\circ\text{C}$ — Peak Repetitive, $T_C = 25^\circ\text{C}$ — Peak Nonrepetitive, $T_C = 25^\circ\text{C}$	I_C	50	A	
		75		
		150		
		250		
Base Current — Continuous — Peak Nonrepetitive	I_B	50	A	
		100		
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C For 1-minute overload	P_D	500	Watts	
		4.0	W/ $^\circ\text{C}$	
		667	Watts	
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
		-55 to 200		

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 250 \text{ mAdc}, I_B = 0$)	$V_{CEO(sus)}$	850	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 900 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 900 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)	I_{CEV}	—	—	2.0	mAdc
		—	—	10	
Collector Cutoff Current ($V_{CE} = 900 \text{ Vdc}, R_{BE} = 10 \Omega, T_C = 100^\circ\text{C}$)	I_{CER}	—	—	10	mAdc
Emitter Cutoff Current ($V_{EB} = 4.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	—	650	mAdc

SAFE OPERATING AREA

Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figure 13
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figure 14
Overload SOA	OLSOA	See Figures 16 and 17

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 50 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 50 \text{ A}, V_{CE} = 10 \text{ V}$)	h_{FE}	35	—	—	
		40	—	—	
Collector-Emitter Saturation Voltage ($I_C = 50 \text{ A}, I_B = 4.0 \text{ A}$) ($I_C = 75 \text{ Adc}, I_B = 15 \text{ A}$) ($I_C = 50 \text{ Adc}, I_B = 4.0 \text{ A}, T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	2.0	Vdc
		—	—	5.0	
		—	—	2.5	
Base-Emitter Saturation Voltage ($I_C = 50 \text{ Adc}, I_B = 4.0 \text{ Adc}$) ($I_C = 50 \text{ Adc}, I_B = 4.0 \text{ Adc}, T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	3.0	Vdc
		—	—	3.0	

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f_{test} = 1.0 \text{ kHz}$)	C_{ob}	—	—	4000	pF
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(1) Pulse Test. Pulse width of $300 \mu\text{s}$, duty cycle $\leq 2.0\%$.

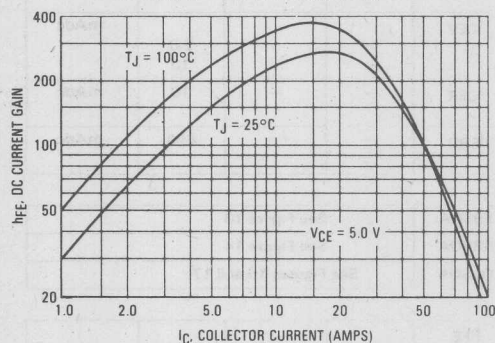
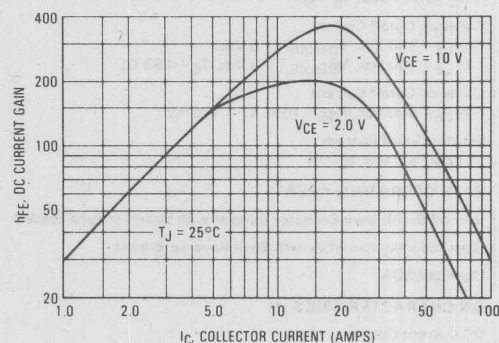
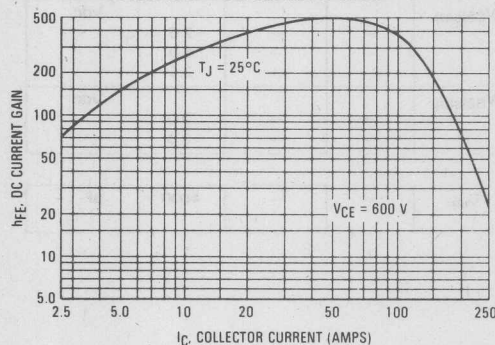
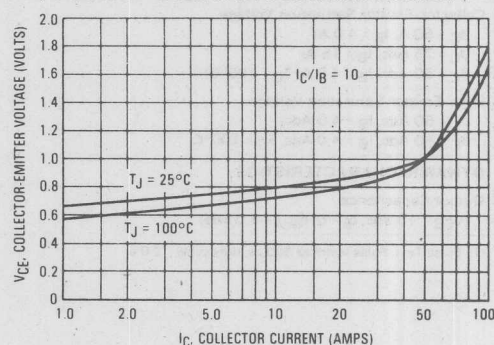
ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit	
SWITCHING CHARACTERISTICS							
Resistive Load							
Delay Time	(V _{CC} = 300 Vdc, I _C = 50 A, I _{B1} = 4.0 A, R _{BE} = 10 Ω, t _p = 50 μs, Duty Cycle ≤ 2.0%)	t _d	—	0.03	0.25	μs	
Rise Time		t _r	—	1.2	5.0	μs	
Storage Time		t _s	—	35	100	μs	
Fall Time		t _f	—	8.5	35	μs	
Inductive Load, Clamped							
Storage Time	(I _{CM} = 50 A, V _{CEM} = 300 V, R _{BE} = 10 Ω, I _{B1} = 4.0 A)	T _J = 100°C	t _{sv}	—	50	150	μs
Crossover Time			t _c	—	20	60	μs
Storage Time		T _J = 25°C	t _{sv}	—	35	100	μs
Crossover Time			t _c	—	10	35	μs

C-E DIODE CHARACTERISTICS

Power Dissipation ($I_B = 0$)	P_D	—	—	250	W
Forward Voltage (1) ($I_F = 50\text{ A}$)	V_F	—	1.0	1.5	V
		—	1.2	2.0	V
Reverse Recovery Time ($d_i/d_t = 25\text{ A}/\mu\text{s}, I_F = 50\text{ A}$)	t_{rr}	—	4.0	12	μs
Forward Turn-On Time (Compliance Voltage = 50 V, $I_F = 50\text{ A}$)	t_{on}	—	0.3	1.2	μs
Single Cycle Surge Current (60 Hz)	I_{FSM}	—	—	500	A

(1) Pulse Test. Pulse width of 300 μs , duty cycle $\leq 2.0\%$.

TYPICAL ELECTRICAL CHARACTERISTICS
FIGURE 1 — DC CURRENT GAIN

FIGURE 2 — DC CURRENT GAIN

FIGURE 3 — DC CURRENT GAIN

FIGURE 4 — COLLECTOR SATURATION VOLTAGE


TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

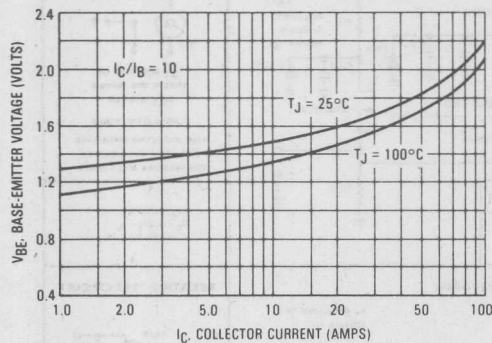
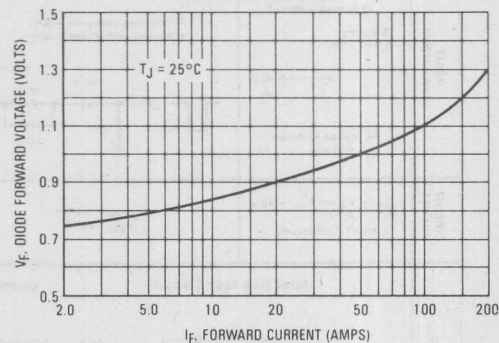


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

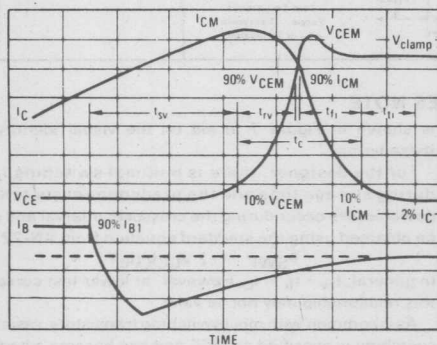


FIGURE 8 — TYPICAL INDUCTIVE SWITCHING TIMES

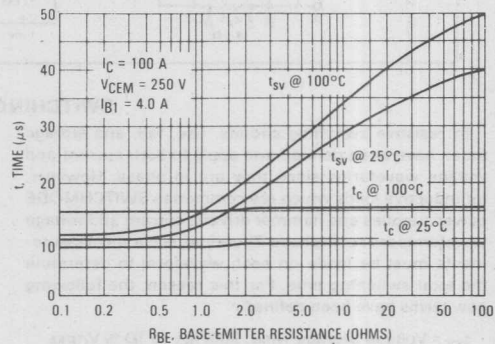


FIGURE 9 — TYPICAL TURN-ON SWITCHING TIMES

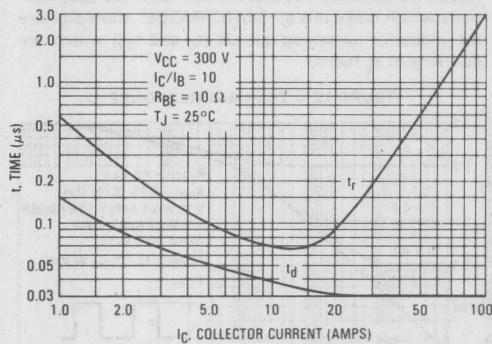


FIGURE 10 — TYPICAL TURN-OFF SWITCHING TIMES

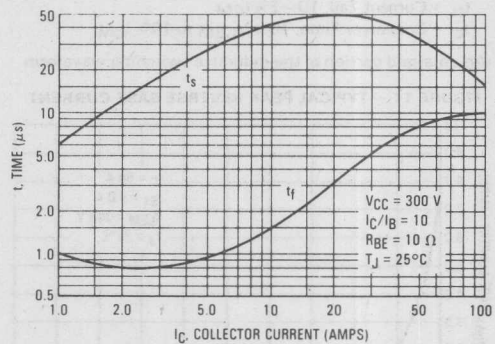
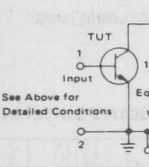
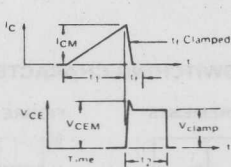
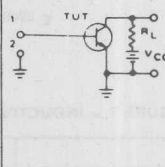


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

INPUT CONDITIONS	V _{CE0(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
CIRCUIT VALUES	$L_{coil} = 10 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CE0(sus)}$	<p>DRIVER SCHEMATIC</p> <p>For inductive loads pulse width is adjusted to obtain specified I_C</p> <p>$t_{coil} = 5.0 \mu\text{H}$ $V_{CC} = 20 \text{ V}$</p>	<p>RESISTIVE SWITCHING</p> <p>TURN ON TIME</p> <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME</p> <p>Use inductive switching circuit as the input to the resistive test circuit</p> <p>$V_{CC} = 300 \text{ V}$ $R_L = 6.0 \Omega$ Pulse Width: $25 \mu\text{s}$</p>
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT	OUTPUT WAVEFORMS	RESISTIVE TEST CIRCUIT
	 <p>See Above for Detailed Conditions</p>	 <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$</p> <p>$t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$</p> <p>Test Equipment: Scope Tektronix 475 or Equivalent</p>	

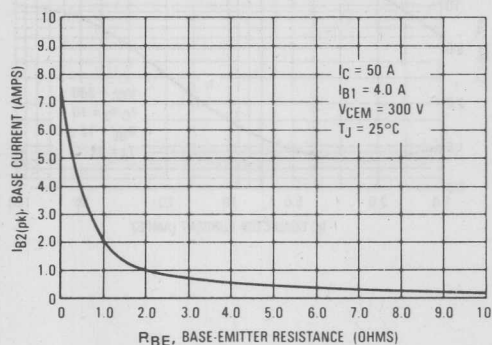
SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{RV} = Voltage Rise Time, 10–90% V_{CEM}
- t_{fi} = Current Fall Time, 90–10% I_{CM}
- t_{ti} = Current Tail, 10–2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform

FIGURE 11 — TYPICAL PEAK REVERSE BASE CURRENT



is shown in Figure 7 to aid on the visual identity of these terms.

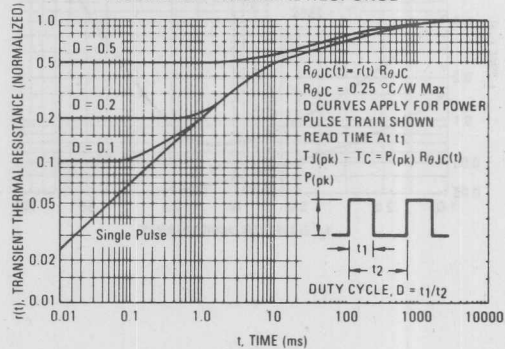
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c + t_{fi})$$

In general, $t_{RV} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{SV}) which are guaranteed at 100°C .

FIGURE 12 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

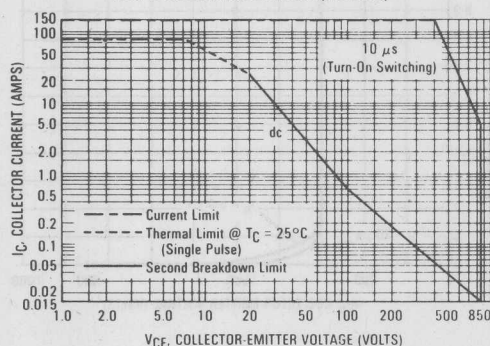


FIGURE 14 — MAXIMUM REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

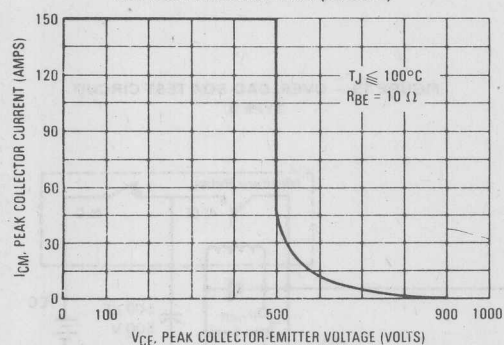
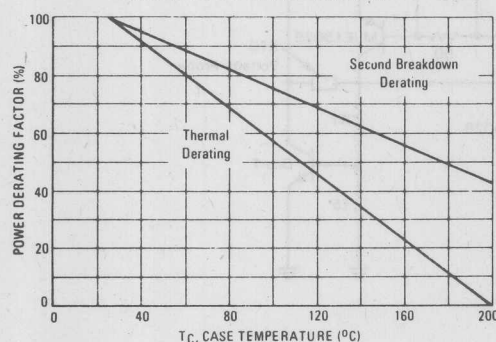


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the MJ10050. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known,

(continued on back page)

OVERLOAD CHARACTERISTICS

FIGURE 16 — OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)

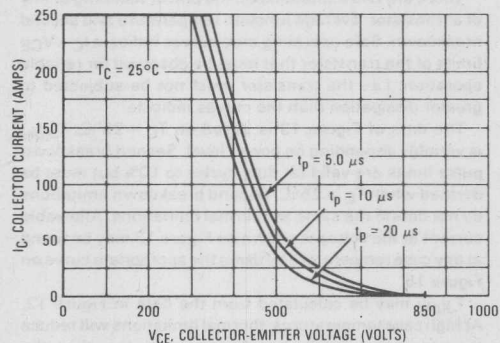


FIGURE 17 — OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)

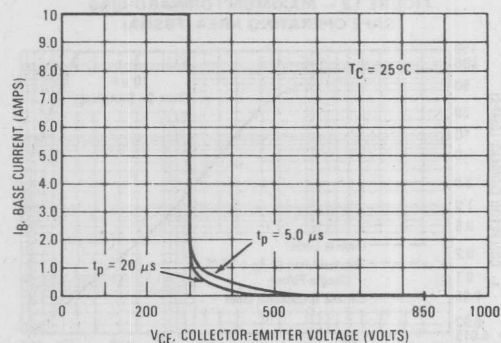


FIGURE 18 — OVERLOAD SOA TEST CIRCUIT
TYPE I

- Notes:**

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C , t_p

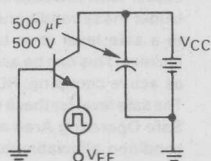


FIGURE 19 — OVERLOAD SOA TEST CIRCUIT
TYPE II

- Notes:**

- Rep Rate ≤ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test

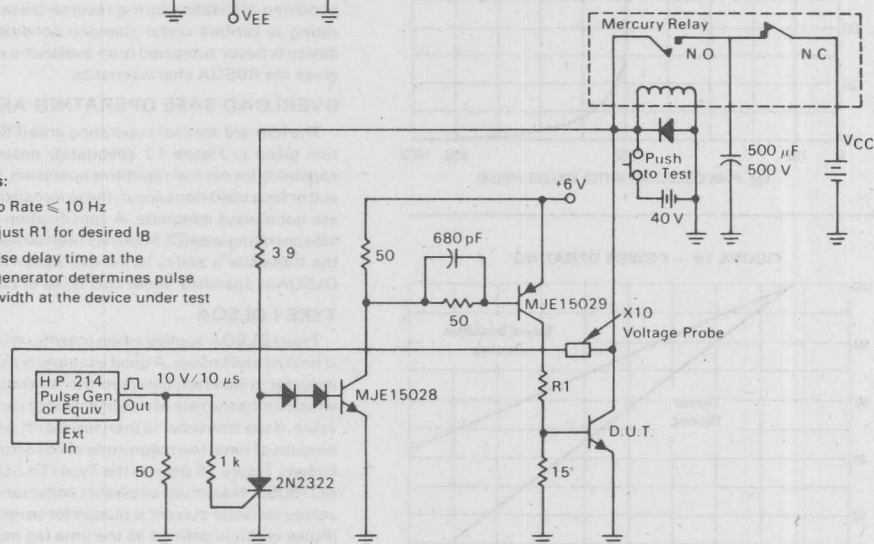
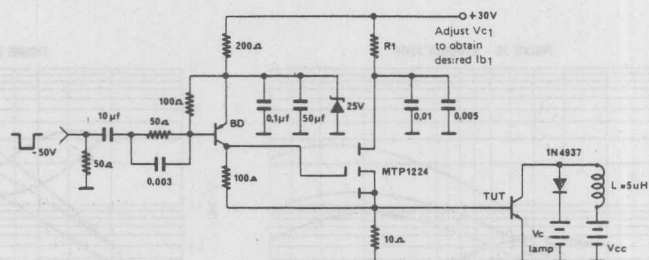
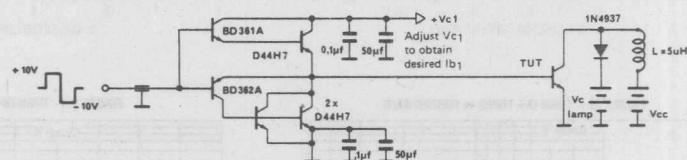


TABLE 2 — TYPICAL SWITCHING CHARACTERISTICS vs BASE DRIVE CIRCUITS

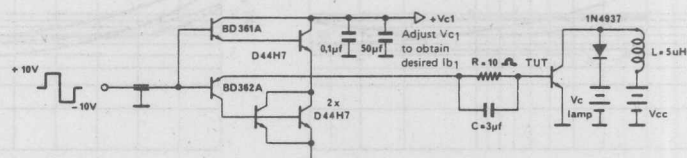
CIRCUIT A



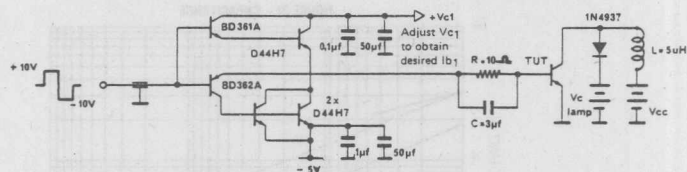
CIRCUIT B



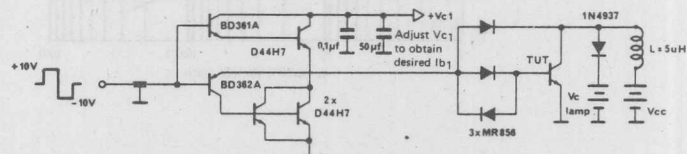
CIRCUIT C



CIRCUIT D



CIRCUIT E



TYPICAL SWITCHING CHARACTERISTICS vs BASE DRIVE CIRCUITS

FIGURE 20 - STORAGE TIME

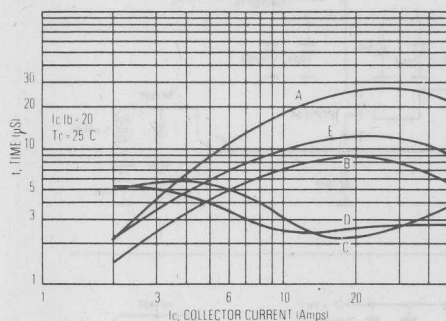


FIGURE 21 - FALL TIMES

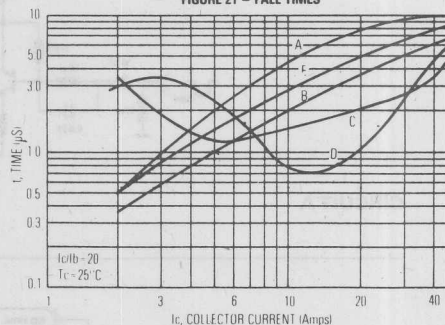


FIGURE 22 - TURN-OFF TIMES vs FORCED GAIN

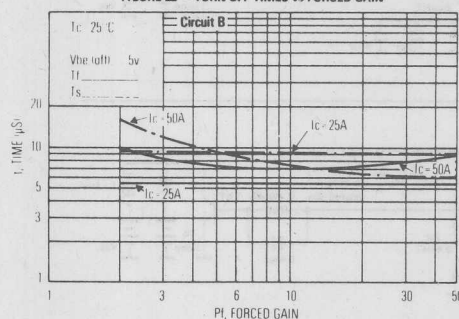


FIGURE 23 - TURN-OFF TIMES vs I_b2/I_b1

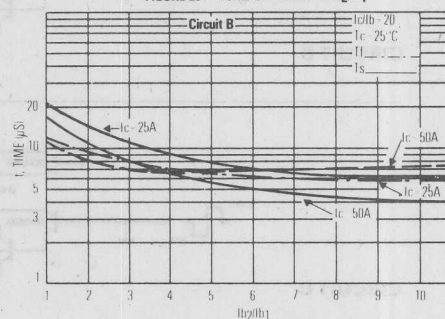
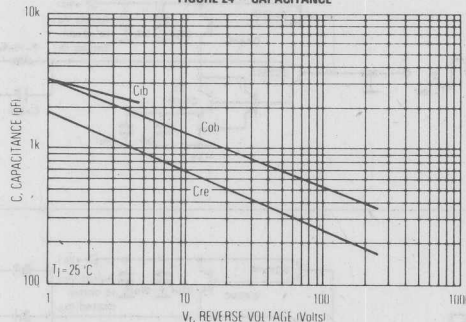


FIGURE 24 - CAPACITANCE



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as

shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the MJ10050 is 100 occurrences. Another factor is the form of turn-off bias. For the MJ10050, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.



PARAMETER	SYMBOL	UNIT	MIN.	MAX.
DC Current Gain	h_{FE}		100	300
Base-Emitter Voltage	V_{BE}	V	0.6	0.7
Collector-Emitter Voltage	V_{CE}	V	0	30
Collector Current	I_C	A	0	1.0
Base Current	I_B	A	0	0.1
Power Dissipation	P_D	W	0.5	1.0
Storage Time	t_s	ns	0	100
Turn-Off Time	t_{off}	ns	0	100
Switching Time	t_{sw}	ns	0	100
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10

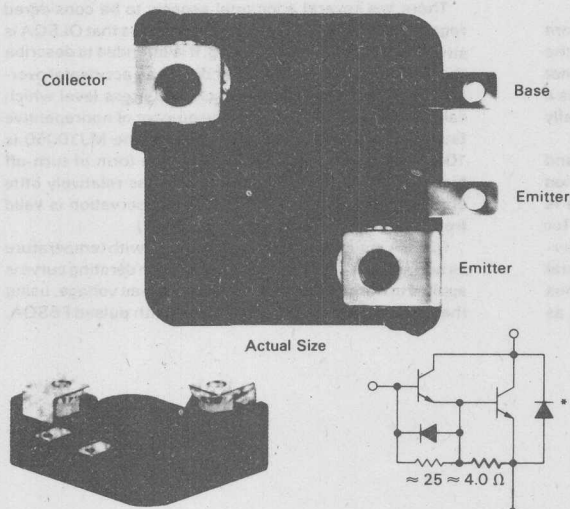
PARAMETER	SYMBOL	UNIT	MIN.	MAX.
DC Current Gain	h_{FE}		100	300
Base-Emitter Voltage	V_{BE}	V	0.6	0.7
Collector-Emitter Voltage	V_{CE}	V	0	30
Collector Current	I_C	A	0	1.0
Base Current	I_B	A	0	0.1
Power Dissipation	P_D	W	0.5	1.0
Storage Time	t_s	ns	0	100
Turn-Off Time	t_{off}	ns	0	100
Switching Time	t_{sw}	ns	0	100
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10

PARAMETER	SYMBOL	UNIT	MIN.	MAX.
DC Current Gain	h_{FE}		100	300
Base-Emitter Voltage	V_{BE}	V	0.6	0.7
Collector-Emitter Voltage	V_{CE}	V	0	30
Collector Current	I_C	A	0	1.0
Base Current	I_B	A	0	0.1
Power Dissipation	P_D	W	0.5	1.0
Storage Time	t_s	ns	0	100
Turn-Off Time	t_{off}	ns	0	100
Switching Time	t_{sw}	ns	0	100
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10
Capacitance	C_{je}	pF	0	10
Capacitance	C_{jc}	pF	0	10
Capacitance	C_{js}	pF	0	10

Designer's Data Sheet

50 KVA HIGH SPEED SWITCHMODE TRANSISTOR 50-Ampere Operating Current

The MJ10051 Darlington transistor is designed for industrial service under practical operating environments requiring fast switching speed for highly efficient systems operating at high frequency such as inverters, PWM controllers and other high frequency system operating from 460 V lines.



*Emitter-Collector Diode is a fast recovery, high power diode.

MAXIMUM RATINGS

MECHANICAL RATINGS

Rating	Value	Unit
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	$^{\circ}\text{C}/\text{W}$
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Mica Insulators available as separate items.

0.003" thick. Motorola Part Number B12387B001.

0.006" thick. Motorola Part Number B12387B002.

Notes:

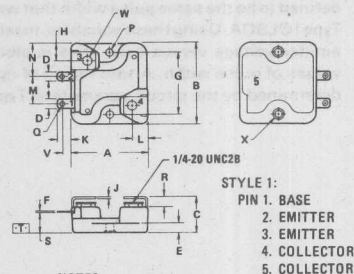
- A Belleville washer of 0.472" O.D., 0.205" I.D., 0.024" thick and 150 pounds flat is recommended such as P/N AM125206 available from National Disc Spring Div., 385 Hillside Ave., Hillside N.J. 07205.
- The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75".

50 AMPERE NPN SILICON POWER DARLINGTON TRANSISTOR

750 and 850 VOLTS
500 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



NOTES:

- DIMENSION A AND B ARE DATUMS.
- $\overline{\text{T}}$ IS SEATING PLANE.
- POSITIONAL TOLERANCE FOR MOUNTING HOLES:
 $\phi 0.36 (0.014) \text{ T A } \text{B}$
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	—	26.67	—	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31	BSC	1.705	BSC
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01

MAXIMUM RATINGS (Continued)

ELECTRICAL RATINGS				
Rating		Symbol	Value	Unit
Collector-Emitter Voltage	MJ10051 MJ10052	V_{CEO}	850 750	Vdc
Collector-Emitter Voltage ($R_{BE} = 10 \text{ Ohms}$)		V_{CER}	900	Vdc
Collector-Base Voltage		V_{CB}	900	Vdc
Emitter-Base Voltage		V_{EB}	8.0	Vdc
Collector Current — Operating, $T_C = 125^\circ\text{C}$ — Continuous, $T_C = 25^\circ\text{C}$ — Peak Repetitive, $T_C = 25^\circ\text{C}$ — Peak Nonrepetitive, $T_C = 25^\circ\text{C}$		I_C	50 75 150 250	A
Base Current — Continuous — Peak Nonrepetitive		I_B	50 100	A
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C For 1-minute overload		P_D	500 4.0 667	Watts W/ $^\circ\text{C}$ Watts
Operating Junction and Storage Temperature Range For 1-minute overload		T_J, T_{stg}	-55 to +150 -55 to +200	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 250 \text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	850 750	— —	— —	Vdc
Collector Cutoff Current ($V_{CE} = 900 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 900 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	2.0 10	mAdc
Emitter Cutoff Current ($V_{EB} = 4.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	950	mAdc
SAFE OPERATING AREA					
Second Breakdown Collector Current with Base Forward-Biased	FBSOA			—	
Clamped Inductive SOA with Base Reverse-Biased	RBSOA			—	
Overload SOA	OLSOA			—	
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 50 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 50 \text{ A}$, $V_{CE} = 10 \text{ V}$)	h_{FE}	25 40	— —	— —	
Collector-Emitter Saturation Voltage ($I_C = 50 \text{ Adc}$, $I_B = 5.0 \text{ A}$) ($I_C = 75 \text{ Adc}$, $I_B = 15 \text{ A}$) ($I_C = 50 \text{ Adc}$, $I_B = 5.0 \text{ A}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.0 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 50 \text{ Adc}$, $I_B = 5.0 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 5.0 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	3.0 3.0	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0 \text{ kHz}$)	C_{ob}	—	—	4000	pF

(1) Pulse Test. Pulse width of 300 μs , duty cycle $\leq 2.0\%$.

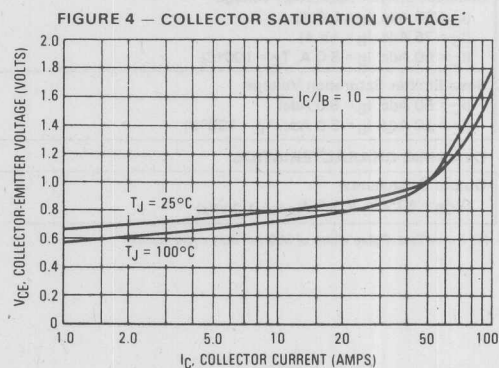
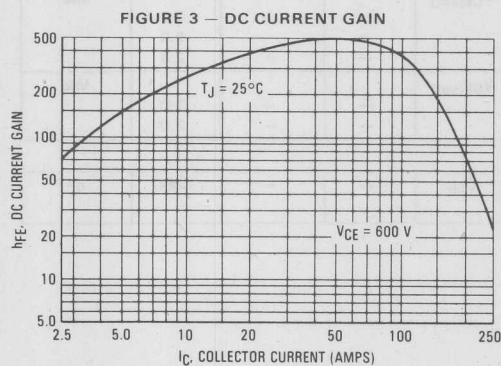
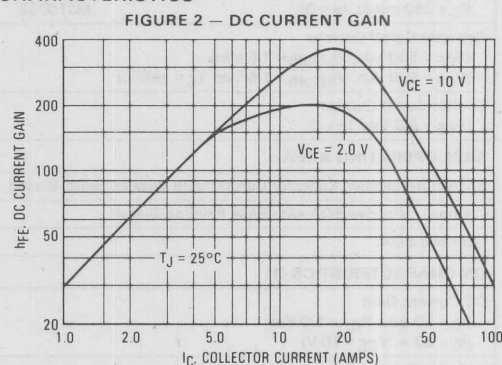
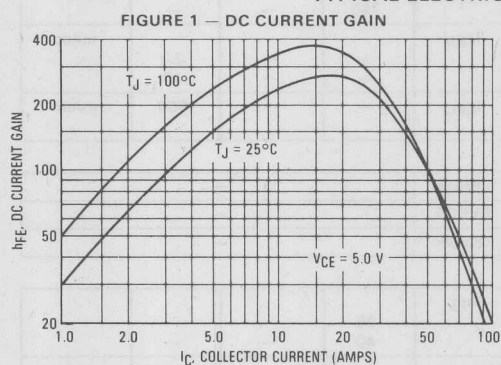
ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
SWITCHING CHARACTERISTICS						
Resistive Load						
Delay Time	$(V_{CC} = 300\text{ Vdc}, I_C = 50\text{ A}, I_{B1} = 5.0\text{ A},$ $V_{BE(off)} = 5.0\text{ V}, t_p = 50\text{ }\mu\text{s},$ Duty Cycle $\leq 2.0\%$)	t_d	—	0.03	μs	
Rise Time		t_r	—	1.2	μs	
Storage Time		t_s	—	3.3	μs	
Fall Time		t_f	—	1.5	μs	
Inductive Load, Clamped						
Storage Time	$(I_{CM} = 50\text{ A},$ $V_{CEM} = 300\text{ V}, V_{BE(off)} = 5.0\text{ V},$ $I_{B1} = 5.0\text{ A})$	$T_J = 100^\circ\text{C}$	t_{sv}	—	5.0	μs
Crossover Time		t_c	—	3.0	μs	
Storage Time	$T_J = 25^\circ\text{C}$	t_{sv}	—	3.5	μs	
Crossover Time		t_c	—	1.5	μs	
C-E DIODE CHARACTERISTICS						
Power Dissipation ($I_B = 0$)	P_D	—	—	250	W	
Forward Voltage (1) ($I_F = 50\text{ A}$)	V_F	—	2.7	5.0	V	
Reverse Recovery Time* ($di/dt = 50\text{ A}/\mu\text{s}, I_F = 50\text{ A}, V_{BE(off)} = 5.0\text{ V}$)	t_{rr}	—	0.2	1.0	μs	
Forward Turn-On Time (Compliance Voltage = $50\text{ V}, I_F = 50\text{ A}$)	t_{on}	—	0.1	1.0	μs	
Single Cycle Surge Current (60 Hz)	I_{FSM}	—	—	500	A	
Reverse Recovery Current ($I_F = 50\text{ A}, di/dt = 50\text{ A}/\mu\text{s}$)	$I_{RM(REC)}$	—	7.0	25	A	

(1) Pulse Test. Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2.0\%$.

*Requires negative base-emitter voltage for fast recovery performance.

TYPICAL ELECTRICAL CHARACTERISTICS



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

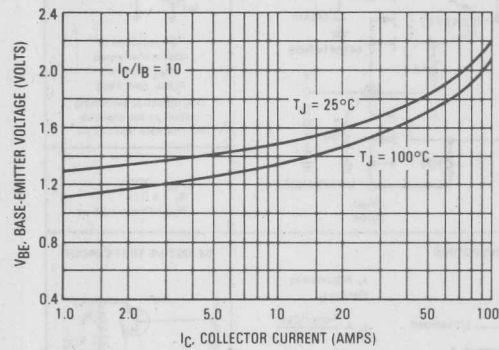
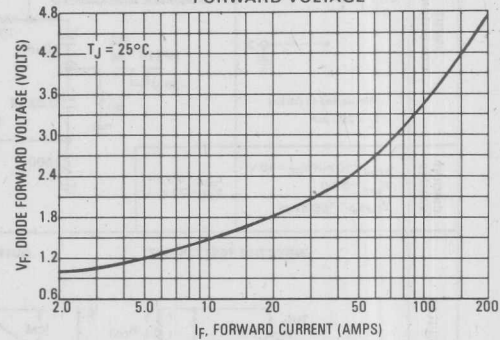


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

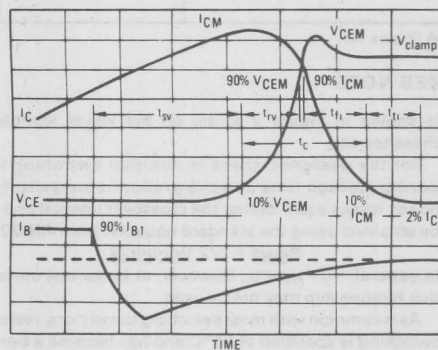


FIGURE 8 — INDUCTIVE SWITCHING TIMES

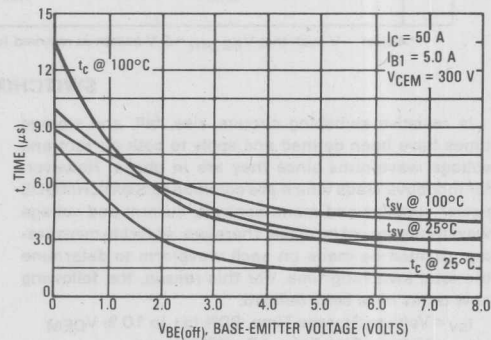


FIGURE 9 — TYPICAL TURN-ON SWITCHING TIMES

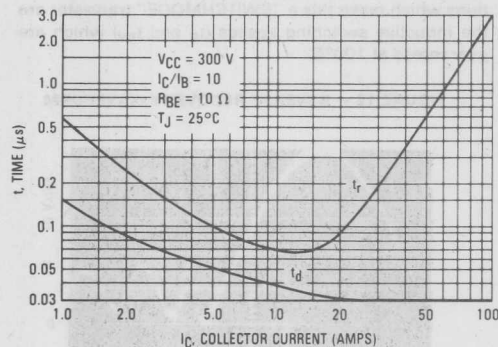


FIGURE 10 — TURN-OFF SWITCHING TIMES

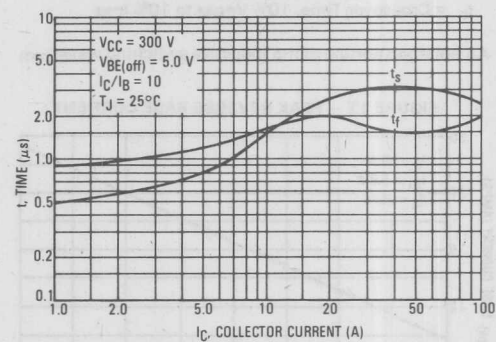
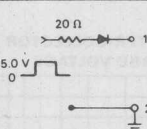
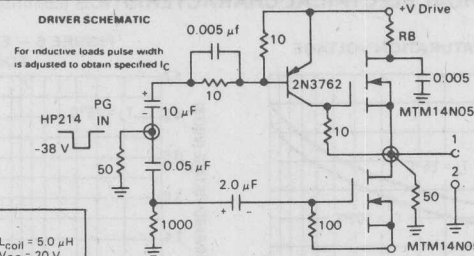
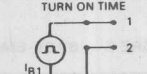
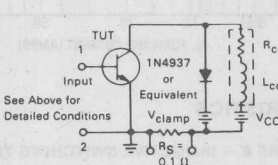
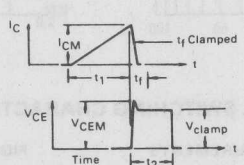
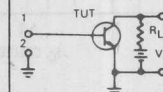


TABLE 1 — RBSOA AND INDUCTIVE SWITCHING DRIVER SCHEMATIC

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 250$ mA</p>	<p>DRIVER SCHEMATIC</p> <p>For inductive loads pulse width is adjusted to obtain specified I_C</p> 	<p>RESISTIVE SWITCHING</p> <p>TURN ON TIME</p>  <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN-OFF TIME</p> <p>Use inductive switching circuit as the input to the resistive test circuit</p>
CIRCUIT VALUES	$L_{coil} = 10$ mH $V_{CC} = 10$ V $R_{coil} = 0.7$ Ω $V_{clamp} = V_{CEO(sus)}$	$L_{coil} = 5.0$ μ H $V_{CC} = 20$ V	$V_{CC} = 300$ V $R_L = 6.0$ Ω Pulse Width = 25 μ s
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 \approx \frac{L_{coil} (I_{CM})}{V_{CC}}$</p> <p>$t_1 \approx \frac{L_{coil} (I_{CM})}{V_{clamp}}$</p> <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

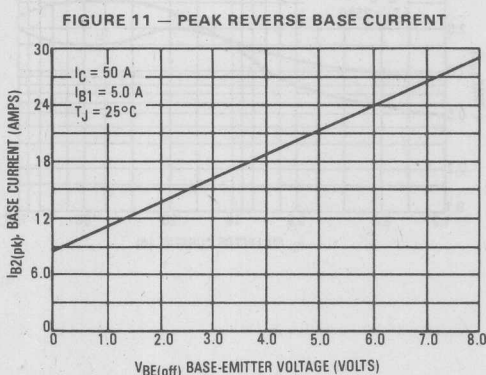
*Adjust — V such that $V_{BE(off)} = 5$ V except as required for RBSOA (Figure 14).

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
- t_{fi} = Current Fall Time, 90—10% I_{CM}
- t_{ti} = Current Tail, 10—2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform



is shown in Figure 7 to aid on the visual identity of these terms.

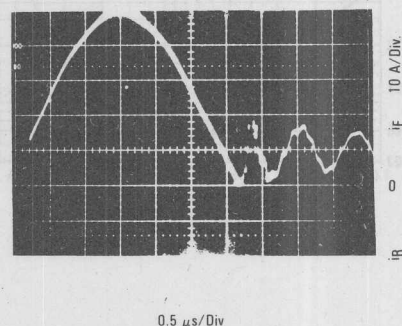
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C t_{cf}$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{SV}) which are guaranteed at 100°C.

FIGURE 12 — REVERSE RECOVERY WAVEFORM



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

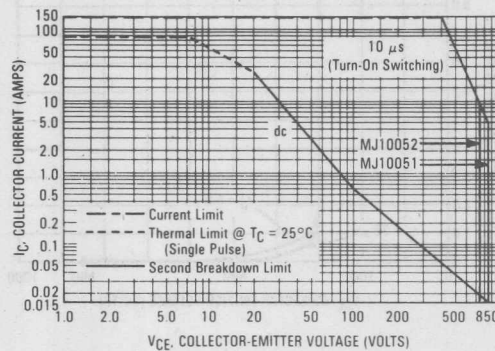


FIGURE 14 — MAXIMUM REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

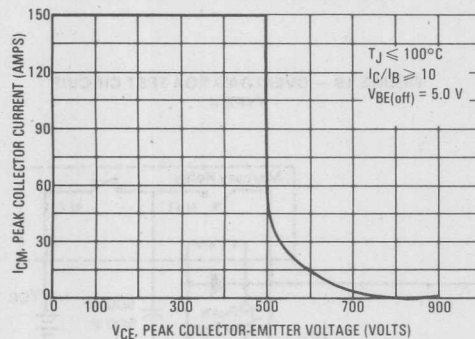
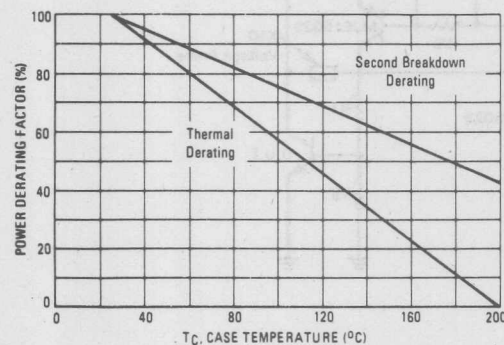


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 20. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the devices. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault

(continued on back page)

OVERLOAD CHARACTERISTICS

**FIGURE 16 — OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)**

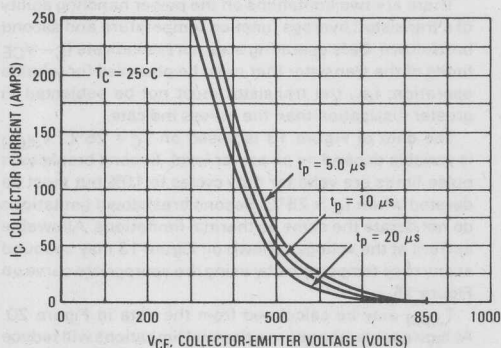


FIGURE 17 — OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)

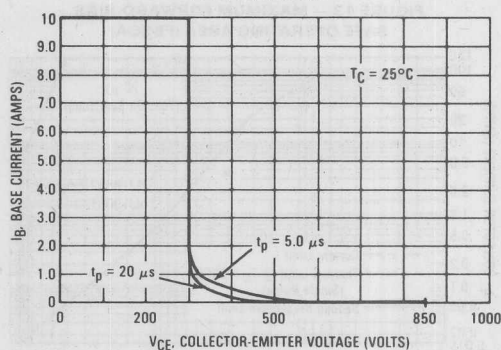


FIGURE 18 — OVERLOAD SOA TEST CIRCUIT
TYPE I

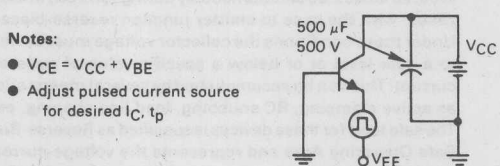
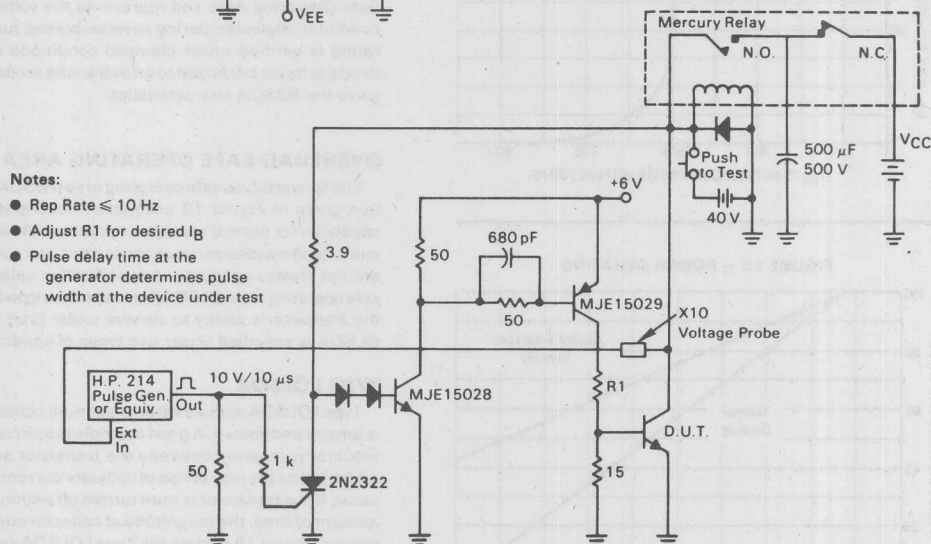


FIGURE 19 — OVERLOAD SOA TEST CIRCUIT
TYPE II



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

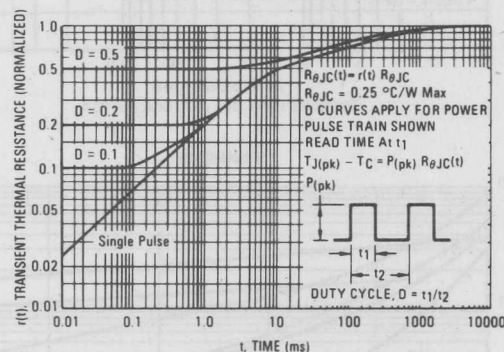
This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus

determined by the circuit parameters. Type II OLSOA, as shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the devices are 100 occurrences. Another factor is the form of turn-off bias. For the devices, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

FIGURE 20 — THERMAL RESPONSE



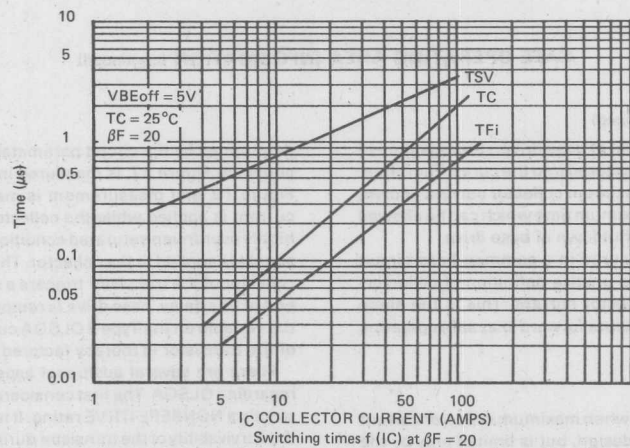


FIGURE 22

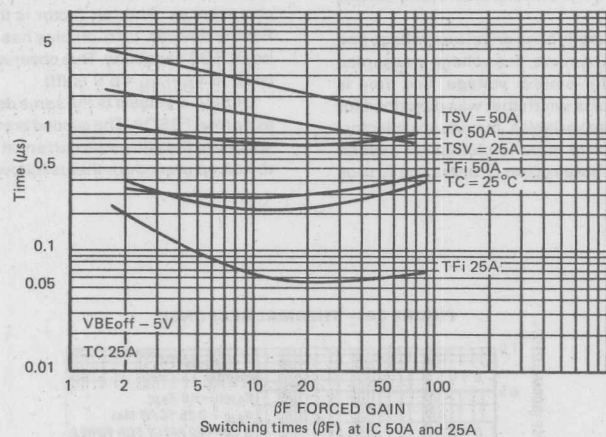
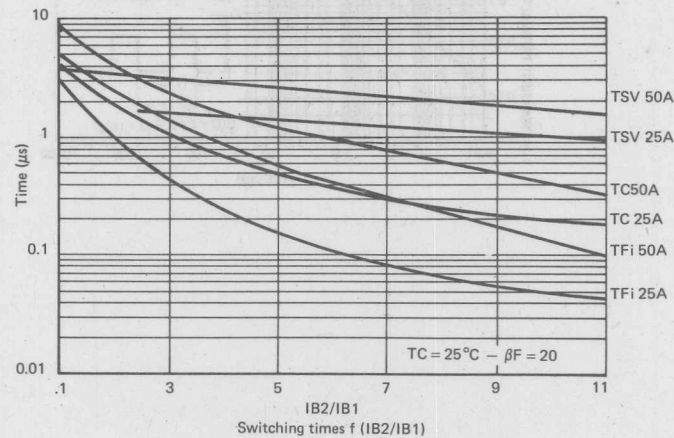
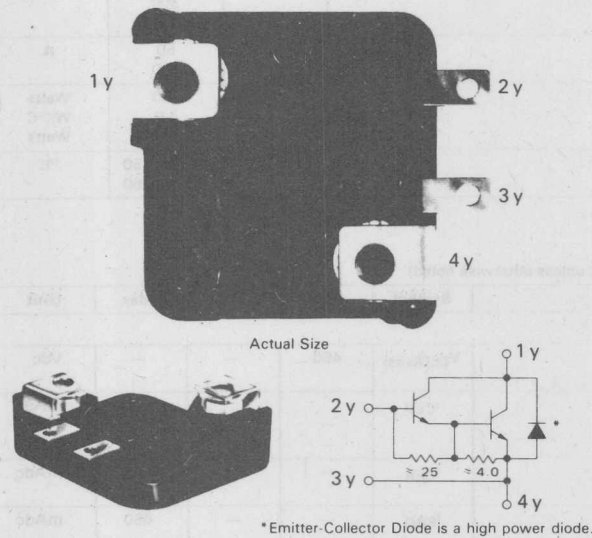


FIGURE 23



**MOTOROLA****MJ10100****Designer's Data Sheet****50 KVA SWITCHMODE TRANSISTOR
100-Ampere Operating Current**

The MJ10100 Darlington transistor is designed for industrial service under practical operating environments found in switching high power inductive loads off 230-Volt lines.

**MAXIMUM RATINGS****Mechanical Ratings**

Rating	Value	Unit
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	$^{\circ}\text{C}/\text{W}$
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Mica Insulators available as separate items.

0.003" thick. Motorola Part Number 14ASB12387B001.

0.006" thick. Motorola Part Number 14ASB12387B002.

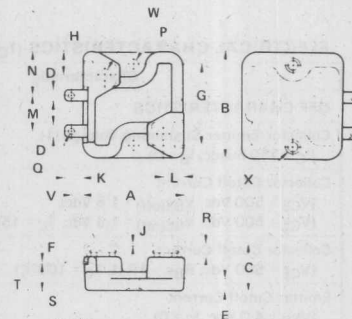
Notes:

1. A Belleville washer of 0.472" O.D., 0.205" I.D., 0.024" thick and 150 pounds flat is recommended.
2. The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75"

**100 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
450 VOLTS
500 WATTS**

**Designer's Data for
"Worst-Case" Conditions**

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.

**NOTES:**

1. DIMENSION A AND B ARE DATUMS.
2. T IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:

$$\pm 0.036 (0.014) \text{ T A B}$$

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C		26.67		1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31	BSC	1.705	BSC
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01

MAXIMUM RATINGS (Continued)

Electrical Ratings				
Rating	Symbol	Value	Unit	
Collector-Emitter Voltage	V_{CEO}	450	Vdc	
Collector-Emitter Voltage ($R_{BE} = 10 \text{ Ohms}$)	V_{CER}	500	Vdc	
Collector-Base Voltage	V_{CB}	500	Vdc	
Emitter-Base Voltage	V_{EB}	8.0	Vdc	
Collector Current — Operating, $T_C = 87.5^\circ\text{C}$ — Continuous, $T_C = 25^\circ\text{C}$ — Peak Repetitive, $T_C = 25^\circ\text{C}$ — Peak Nonrepetitive, $T_C = 25^\circ\text{C}$	I_C	100 150 300 500	A	
Base Current — Continuous — Peak Nonrepetitive	I_B	50 100	A	
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C For 1-minute overload	P_D	500 4.0 667	Watts W/ $^\circ\text{C}$ Watts	
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	-55 to +150 -55 to +200	$^\circ\text{C}$	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 250 \text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 500 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 500 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	2.0 10	mAdc
Collector Cutoff Current ($V_{CE} = 500 \text{ Vdc}$, $R_{BE} = 10 \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	10	mAdc
Emitter Cutoff Current ($V_{EB} = 4.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	650	mAdc

SAFE OPERATING AREA

Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figure 13
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figure 14
Overload SOA	OLSOA	See Figures 16 and 17

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 100 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 100 \text{ A}$, $V_{CE} = 10 \text{ V}$)	h_{FE}	50 60	— —	— —	
Collector-Emitter Saturation Voltage ($I_C = 100 \text{ Adc}$, $I_B = 3.3 \text{ A}$) ($I_C = 150 \text{ Adc}$, $I_B = 12 \text{ A}$) ($I_C = 100 \text{ Adc}$, $I_B = 3.3 \text{ A}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.0 3.3 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 100 \text{ Adc}$, $I_B = 3.3 \text{ Adc}$) ($I_C = 100 \text{ Adc}$, $I_B = 3.3 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— — —	— — —	3.0 3.0	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0 \text{ kHz}$)	C_{ob}	—	—	4000	pF
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(1) Pulse Test. Pulse width of 300 μs , duty cycle $\leq 2.0\%$.

ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
SWITCHING CHARACTERISTICS						
Resistive Load						
Delay Time	$(V_{CC} = 250\text{ Vdc}, I_C = 100\text{ A}, I_{B1} = 3.3\text{ A}, R_{BE} = 10\ \Omega, t_p = 50\ \mu\text{s}, \text{Duty Cycle} \leq 2.0\%)$	t_d	—	0.03	μs	
Rise Time		t_r	—	0.9	3.0	μs
Storage Time		t_s	—	10	25	μs
Fall Time		t_f	—	3.0	10	μs
Inductive Load, Clamped						
Storage Time	$(I_{CM} = 100\text{ A}, V_{CEM} = 250\text{ V}, R_{BE} = 10\ \Omega, I_{B1} = 3.3\text{ A})$	$T_J = 100^\circ\text{C}$	t_{sv}	—	15	μs
Crossover Time			t_c	—	4.0	15
Storage Time		$T_J = 25^\circ\text{C}$	t_{sv}	—	10	μs
Crossover Time			t_c	—	2.7	10
C-E DIODE CHARACTERISTICS						
Power Dissipation ($I_B = 0$)	P_D	—	—	250	W	
Forward Voltage (1) ($I_F = 100\text{ A}$) ($I_F = 200\text{ A}$)	V_F	—	1.1	1.5	V	
		—	1.4	2.0	V	
Reverse Recovery Time ($d_i/d_t = 25\text{ A}/\mu\text{s}, I_F = 100\text{ A}$)	t_{rr}	—	3.3	10	μs	
Forward Turn-On Time (Compliance Voltage = 250 V, $I_F = 100\text{ A}$)	t_{on}	—	0.3	1.0	μs	
Single Cycle Surge Current (60 Hz)	I_{FSM}	—	—	500	A	

(1) Pulse Test. Pulse width of 300 μs , duty cycle $\leq 2.0\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

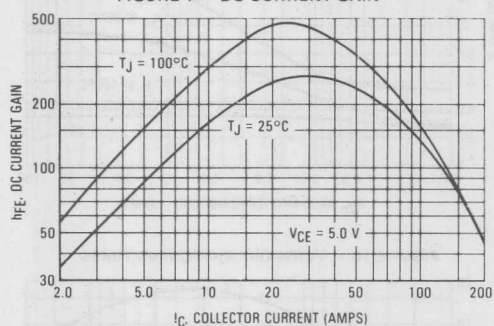


FIGURE 2 — DC CURRENT GAIN

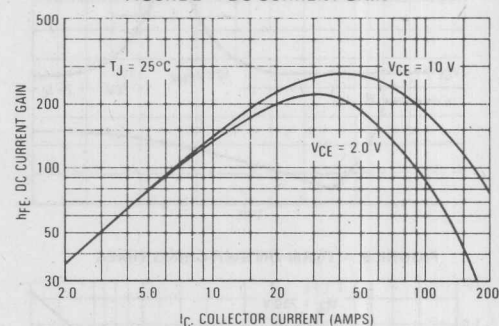


FIGURE 3 — DC CURRENT GAIN

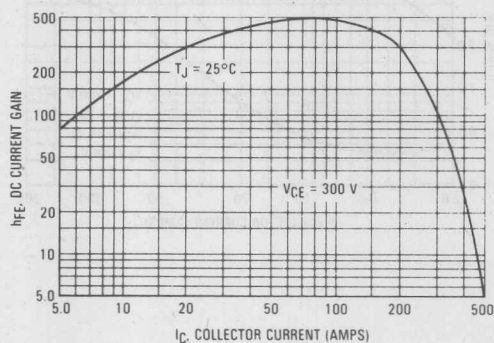
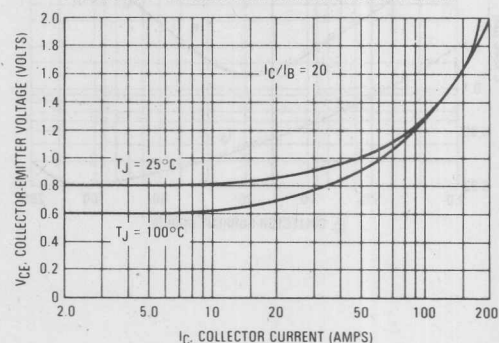


FIGURE 4 — COLLECTOR SATURATION REGION



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

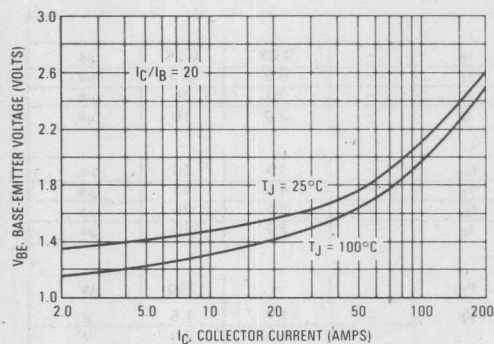
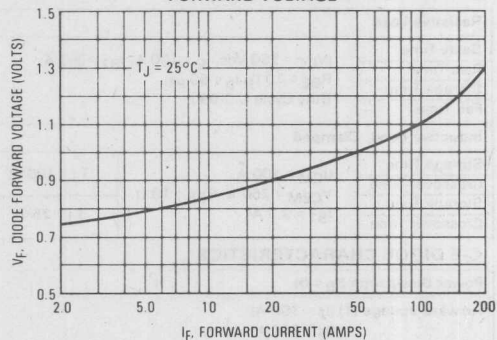


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

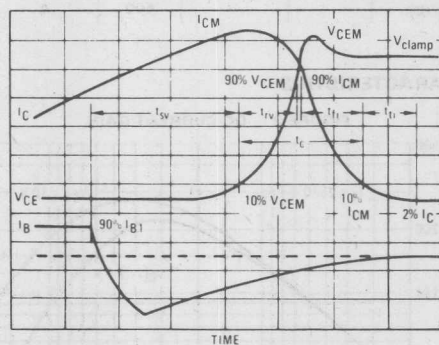


FIGURE 8 — INDUCTIVE SWITCHING TIMES

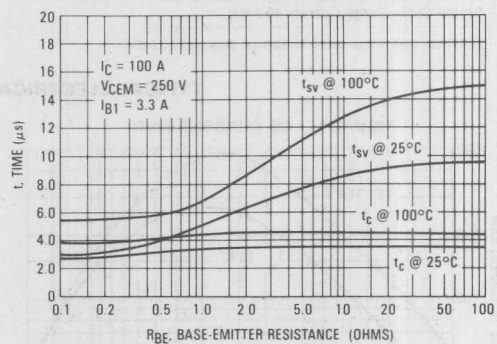


FIGURE 9 — TURN-ON SWITCHING TIMES

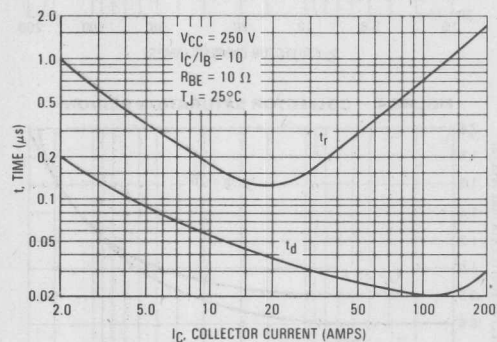


FIGURE 10 — TURN-OFF SWITCHING TIMES

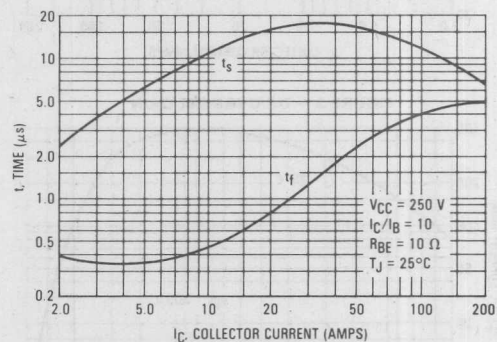


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

VCE(susl)		RBSOA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING	
INPUT CONDITIONS	<p>PW Varied to Attain $I_C = 250 \text{ mA}$</p>	DRIVER SCHEMATIC For inductive loads pulse width is adjusted to obtain specified I_C 		TURN ON TIME <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> TURN OFF TIME Use inductive switching circuit as the input to the resistive test circuit.	
CIRCUIT VALUES	$L_{coil} = 10 \text{ mH}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CE(susl)}$	$L_{coil} = 50 \mu\text{H}$ $V_{CC} = 20 \text{ V}$		$V_{CC} = 250 \text{ V}$ $R_L = 2.5 \Omega$ Pulse Width = $25 \mu\text{s}$	
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT <p>See Above for Detailed Conditions</p>		OUTPUT WAVEFORMS <p>t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope - Tektronix 475 or Equivalent</p>		RESISTIVE TEST CIRCUIT

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{RV} = Voltage Rise Time, 10–90% V_{CEM}
- t_{fi} = Current Fall Time, 90–10% I_{CM}
- t_{ti} = Current Tail, 10–2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform

is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{RV} + t_{fi} = t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{SV}) which are guaranteed at 100°C.

FIGURE 11 — PEAK REVERSE BASE CURRENT

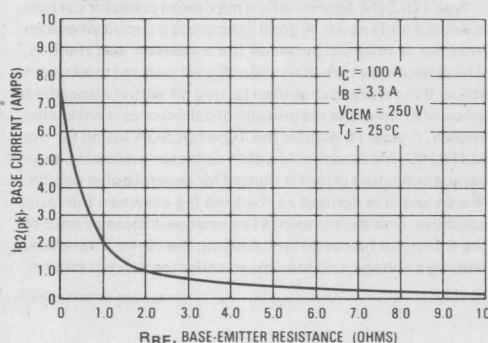
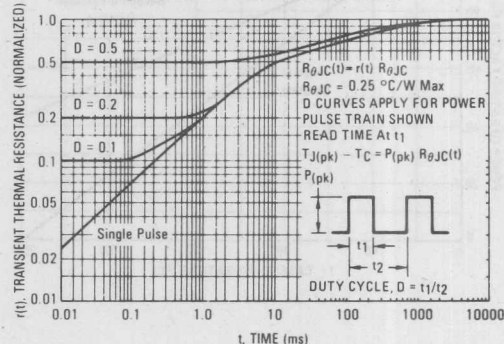


FIGURE 12 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM RATED FORWARD BIAS, SAFE OPERATING AREA (FBSOA)

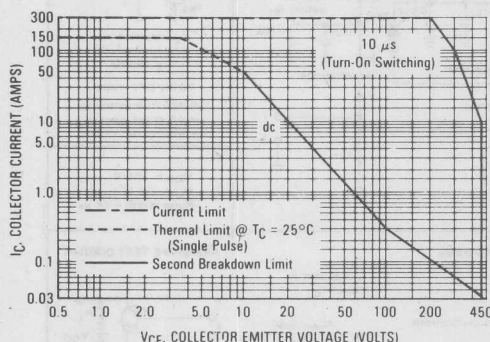


FIGURE 14 — MAXIMUM RATED REVERSE-BIAS, SAFE OPERATING AREA (RBSOA)

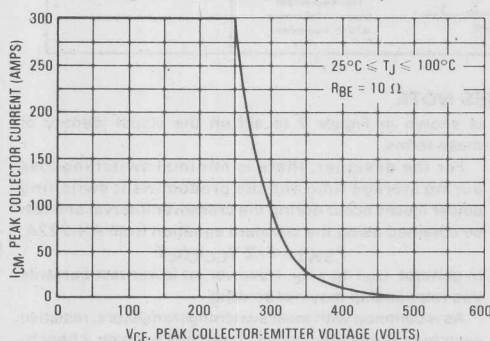
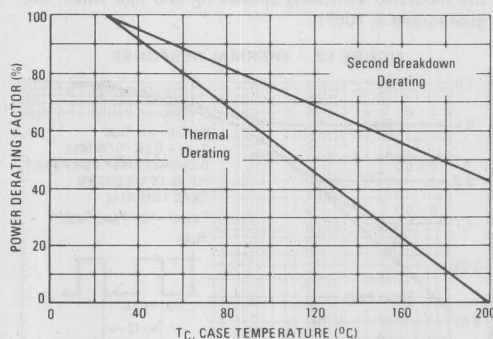


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

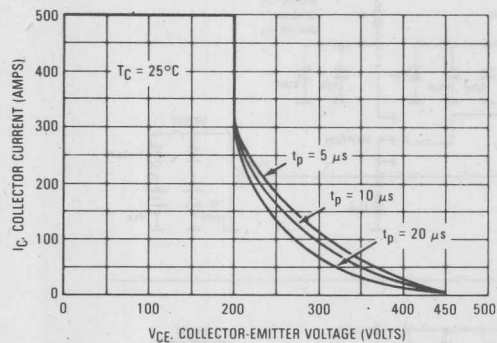
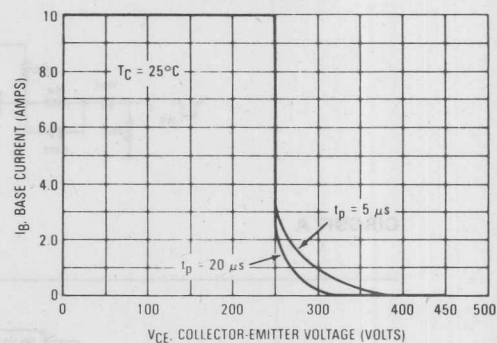
The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the MJ10100. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known,

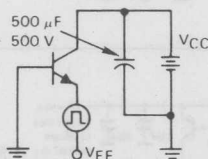
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OVERLOAD CHARACTERISTICS

FIGURE 16 — OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)FIGURE 17 — OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)FIGURE 18 — OVERLOAD SOA TEST CIRCUIT
TYPE I

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C , t_p

FIGURE 19 — OVERLOAD SOA TEST CIRCUIT
TYPE II

Notes:

- Rep Rate ≤ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test

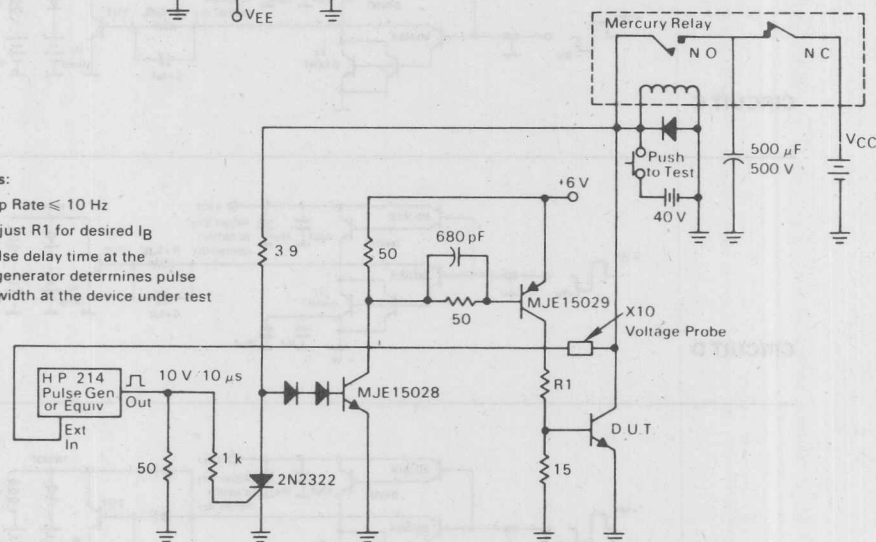
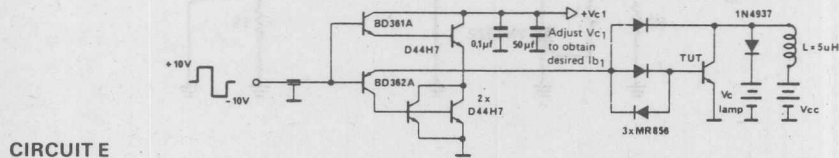
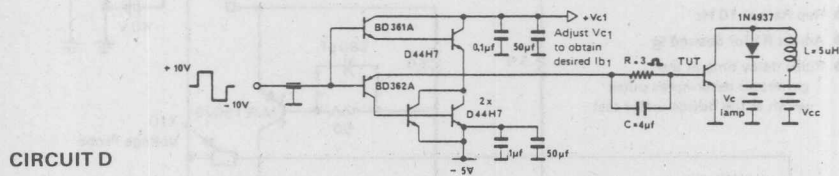
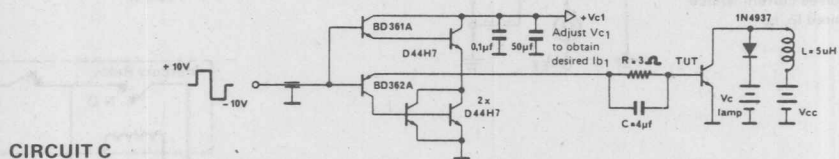
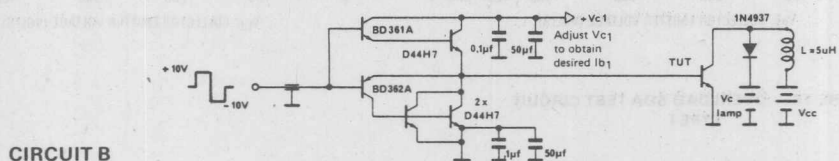
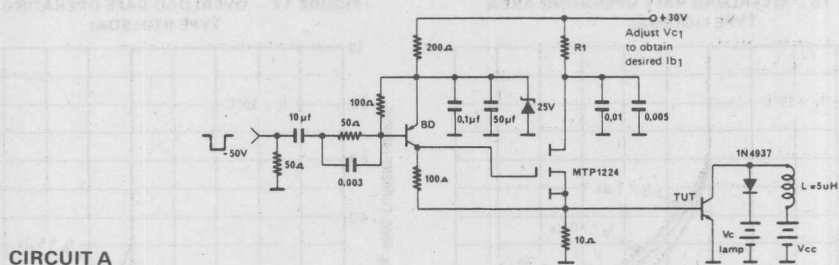


TABLE 2 — TYPICAL SWITCHING CHARACTERISTICS vs BASE DRIVE CIRCUITS



TYPICAL SWITCHING CHARACTERISTICS vs BASE DRIVE CIRCUITS

FIGURE 20 - STORAGE TIMES

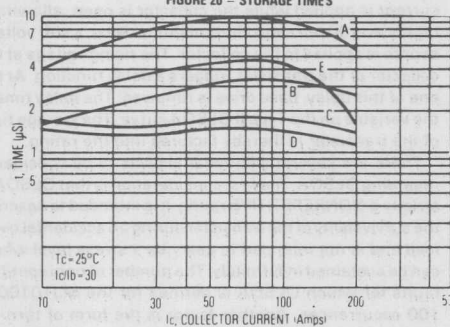


FIGURE 21 - FALL TIMES

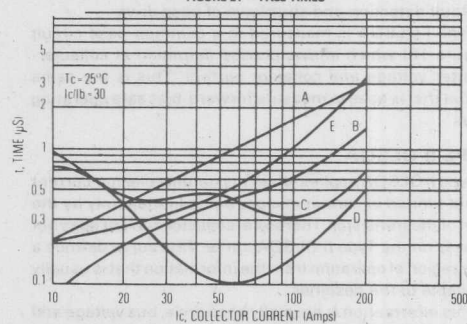


FIGURE 22 - TURN OFF TIMES vs FORCED GAIN

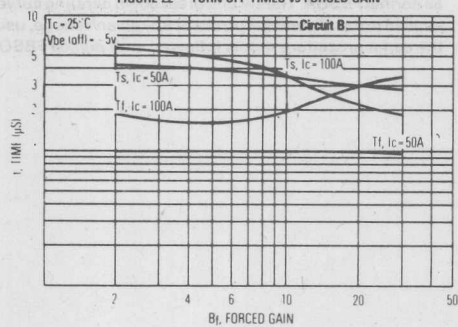
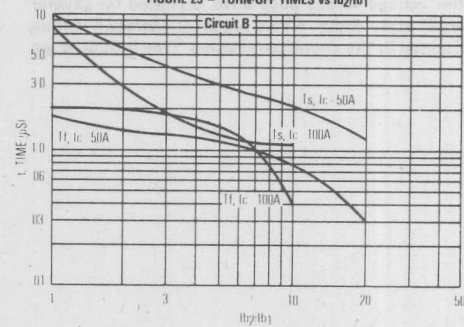
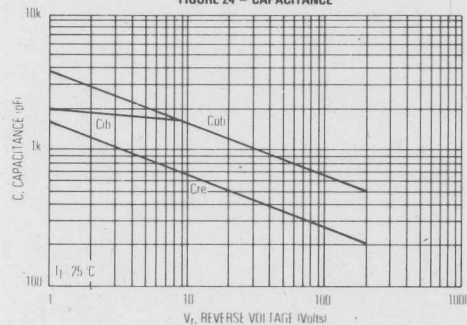
FIGURE 23 - TURN OFF TIMES vs I_{b2}/I_{b1} 

FIGURE 24 - CAPACITANCE



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as

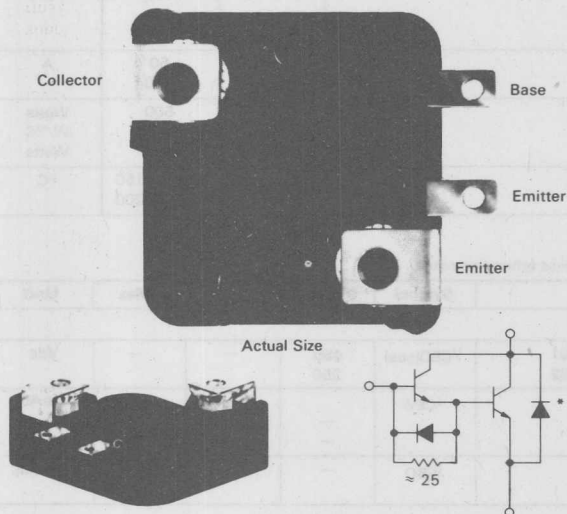
shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the MJ10100 is 100 occurrences. Another factor is the form of turn-off bias. For the MJ10100, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

**MOTOROLA****MJ10101
MJ10102****Designer's Data Sheet****50 KVA HIGH SPEED SWITCHMODE TRANSISTOR
100-Ampere Operating Current**

The MJ10101 Darlington transistor is designed for industrial service under practical operating environments requiring fast switching speed for highly efficient systems operating at high frequency such as inverters, PWM controllers and other high frequency systems operating from 230 V lines.

**MAXIMUM RATINGS****Mechanical Ratings**

Rating	Value	Unit
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	°C/W
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Mica Insulators available as separate items.

0.003" thick. Motorola Part Number B12387B001.

0.006" thick. Motorola Part Number B12387B002.

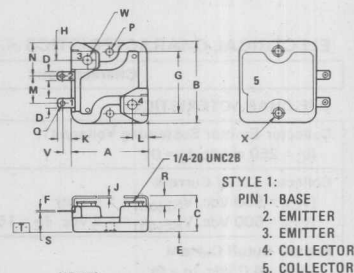
Notes:

1. A Belleville washer of 0.472" O.D., 0.205" I.D., 0.024" thick and 150 pounds flat is recommended such as P/N AM125206 available from National Disc Spring Div., 385 Hillside Ave., Hillside N.J. 07205.

2. The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75".

**100 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
350 and 450 VOLTS
500 WATTS**
**Designer's Data for
"Worst-Case" Conditions**

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.

**NOTES:**

1. DIMENSION A AND B ARE DATUMS.

2. \overline{T} IS SEATING PLANE.

3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:

$$\pm 0.36 (0.014) \text{ T A B}$$

4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	—	26.67	—	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31 BSC	—	1.705 BSC	—
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01

MAXIMUM RATINGS (Continued)

Electrical Ratings				
Rating	Symbol	Value	Unit	
Collector-Emitter Voltage MJ10101 MJ10102	V_{CE0}	450 350	Vdc	
Collector-Emitter Voltage ($R_{BE} = 10 \text{ Ohms}$)	V_{CER}	500	Vdc	
Collector-Base Voltage	V_{CB}	500	Vdc	
Emitter-Base Voltage	V_{EB}	8.0	Vdc	
Collector Current — Operating, $T_C = 87.5^\circ\text{C}$ — Continuous, $T_C = 25^\circ\text{C}$ — Peak Repetitive, $T_C = 25^\circ\text{C}$ — Peak Nonrepetitive, $T_C = 25^\circ\text{C}$	I_C	100 150 300 500	A	
Base Current — Continuous — Peak Nonrepetitive	I_B	50 100	A	
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C For 1-minute overload	P_D	500 4.0 667	Watts W/ $^\circ\text{C}$ Watts	
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	-55 to +150 -55 to +200	$^\circ\text{C}$	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 250 \text{ mAdc}, I_B = 0$) MJ10101 MJ10102	$V_{CE0(sus)}$	450 350	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 500 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 500 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	2.0 10	mAdc
Emitter Cutoff Current ($V_{EB} = 4.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	—	5.0	mAdc

SAFE OPERATING AREA

Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figure 13
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figure 14
Overload SOA	OLSOA	See Figures 16 and 17

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 100 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 100 \text{ A}, V_{CE} = 10 \text{ V}$)	h_{FE}	50 60	— —	— —	
Collector-Emitter Saturation Voltage ($I_C = 100 \text{ Adc}, I_B = 3.3 \text{ A}$) ($I_C = 150 \text{ Adc}, I_B = 12 \text{ A}$) ($I_C = 100 \text{ Adc}, I_B = 3.3 \text{ A}, T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.0 3.3 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 100 \text{ Adc}, I_B = 3.3 \text{ Adc}$) ($I_C = 100 \text{ Adc}, I_B = 3.3 \text{ Adc}, T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	3.0 3.0	Vdc

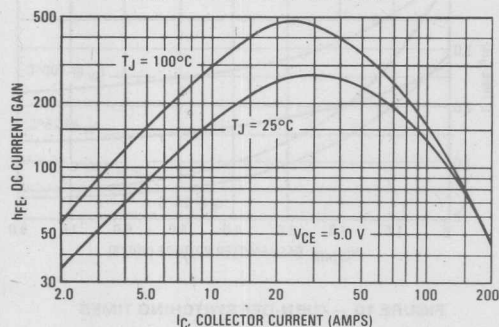
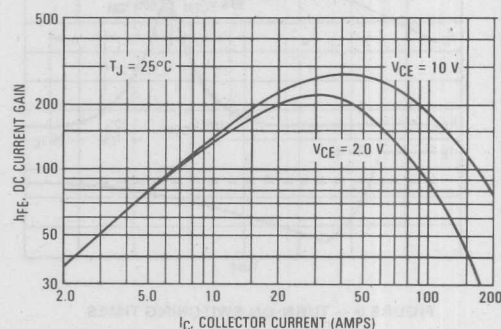
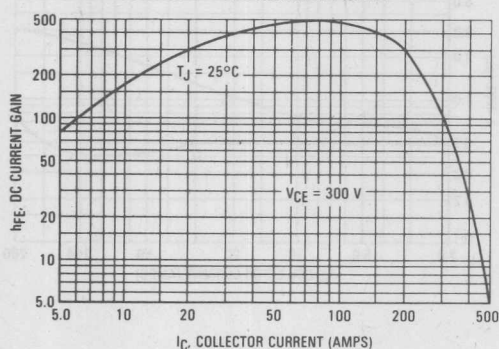
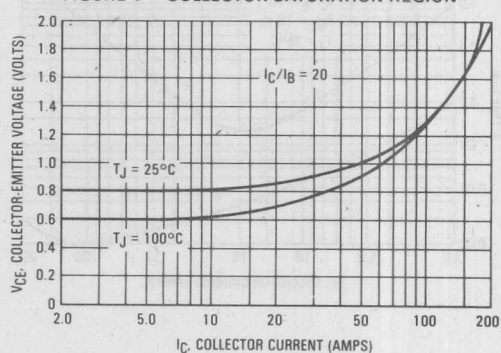
DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f_{test} = 1.0 \text{ kHz}$)	C_{ob}	—	—	4000	pF
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(1) Pulse Test. Pulse width of $300 \mu\text{s}$, duty cycle $\leq 2.0\%$.

ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit		
SWITCHING CHARACTERISTICS							
Resistive Load							
Delay Time	$(V_{CC} = 250\text{ Vdc}, I_C = 100\text{ A}, I_{B1} = 3.3\text{ A}, V_{BE(off)} = 5.0\text{ V}, t_p = 50\text{ }\mu\text{s}$ Duty Cycle $\leq 2.0\%$)	t_d	—	0.03	μs		
Rise Time		t_r	—	0.9	μs		
Storage Time		t_s	—	1.5	3.75	μs	
Fall Time		t_f	—	0.4	1.25	μs	
Inductive Load, Clamped							
Storage Time	$(I_{CM} = 100\text{ A}, V_{BE(off)} = 5.0\text{ V}, V_{CEM} = 250\text{ V}$ $I_{B1} = 3.3\text{ A})$	$T_J = 100^\circ\text{C}$	t_{sv}	—	2.5	7.5	μs
Crossover Time			t_c	—	0.8	3.0	μs
Storage Time		$T_J = 25^\circ\text{C}$	t_{sv}	—	1.5	3.75	μs
Crossover Time			t_c	—	0.5	1.5	μs
C-E DIODE CHARACTERISTICS							
Power Dissipation ($I_B = 0$)		P_D	—	—	250	W	
Forward Voltage (1) ($I_F = 100\text{ A}$)		V_F	—	1.7	5.0	V	
Reverse Recovery Current		$(I_F = 100\text{ A}, di/dt = 100\text{ A}/\mu\text{s})$	$I_{RM(rec)}$	—	20	50	A
Reverse Recovery Time				t_{rr}	—	0.4	1.0
Forward Turn-On Time (Compliance Voltage = 250 V, $I_F = 100\text{ A}$)		t_{on}	—	0.1	0.5	μs	
Single Cycle Surge Current (60 Hz)		I_{FSM}	—	—	500	A	

(1) Pulse Test. Pulse width of 300 μs , duty cycle $\leq 2.0\%$.**TYPICAL ELECTRICAL CHARACTERISTICS****FIGURE 1 — DC CURRENT GAIN****FIGURE 2 — DC CURRENT GAIN****FIGURE 3 — DC CURRENT GAIN****FIGURE 4 — COLLECTOR SATURATION REGION**

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

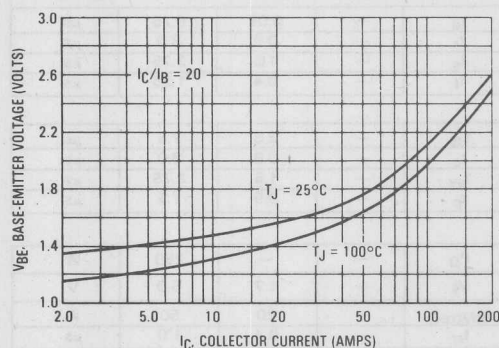
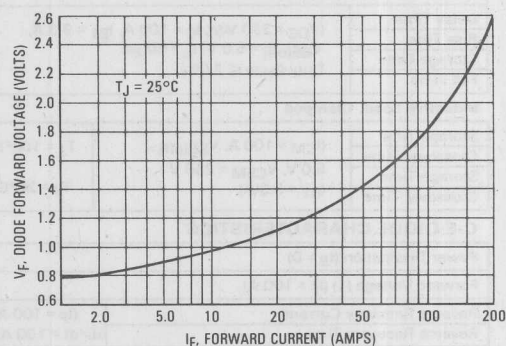


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

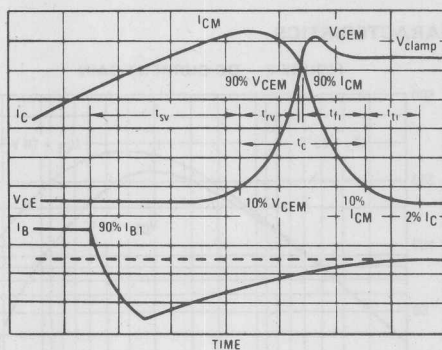


FIGURE 8 — INDUCTIVE SWITCHING TIMES

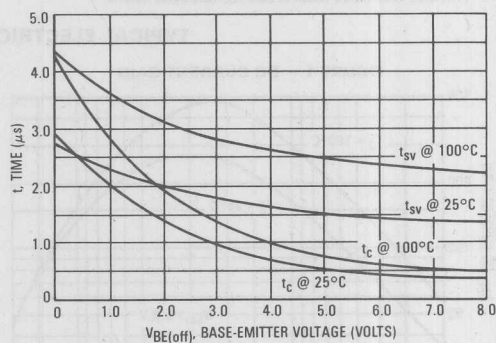


FIGURE 9 — TURN-ON SWITCHING TIMES

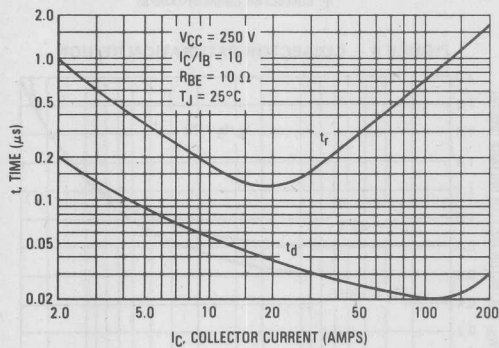


FIGURE 10 — TURN-OFF SWITCHING TIMES

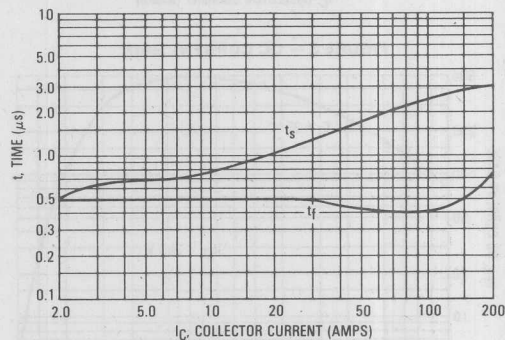


TABLE 1 — RBSOA AND INDUCTIVE SWITCHING DRIVER SCHEMATIC

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
INPUT CONDITIONS		DRIVER SCHEMATIC For inductive loads pulse width is adjusted to obtain specified I_C 		TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching circuit as the input to the resistive test circuit.
CIRCUIT VALUES	$L_{coil} = 10 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CEO(sus)}$			$V_{CC} = 250 \text{ V}$ $R_L = 2.5 \Omega$ Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT		OUTPUT WAVEFORMS	RESISTIVE TEST CIRCUIT
			 t_1 Adjusted to Obtain I_C $t_1 = \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_1 = \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	

*Adjust — V such that $V_{BE(off)} = 5 \text{ V}$ except as required for RBSOA (Figure 14).

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{RV} = Voltage Rise Time, 10—90% V_{CEM}
- t_{fi} = Current Fall Time, 90—10% I_{CM}
- t_{ti} = Current Tail, 10—2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform

is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$PSWT = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{RV} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{SV}) which are guaranteed at 100°C.

FIGURE 11 — PEAK REVERSE BASE CURRENT

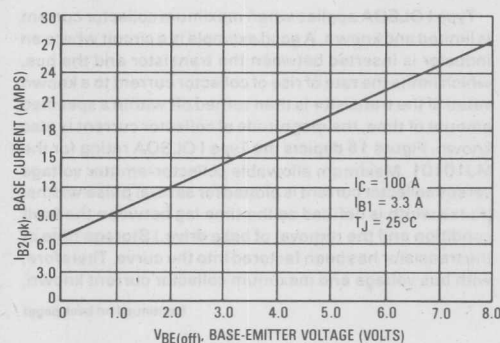
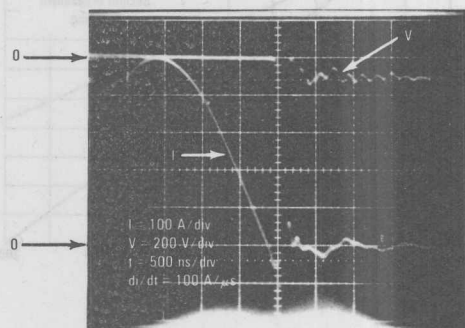


FIGURE 12 — REVERSE RECOVERY WAVEFORM



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM RATED FORWARD BIAS, SAFE OPERATING AREA

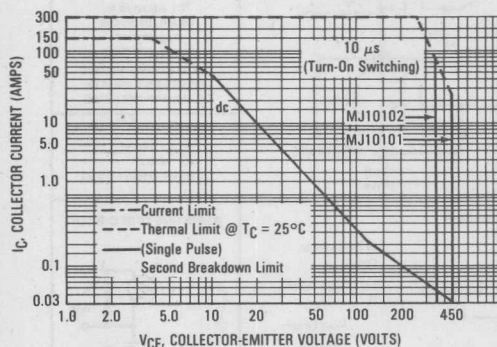


FIGURE 14 — MAXIMUM REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

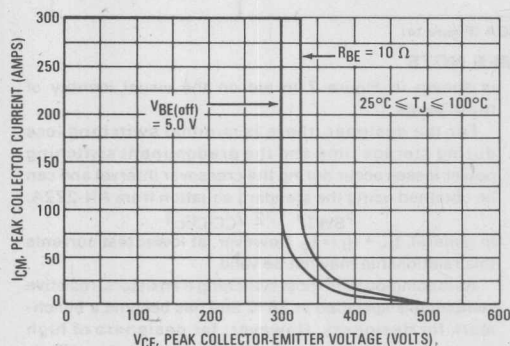
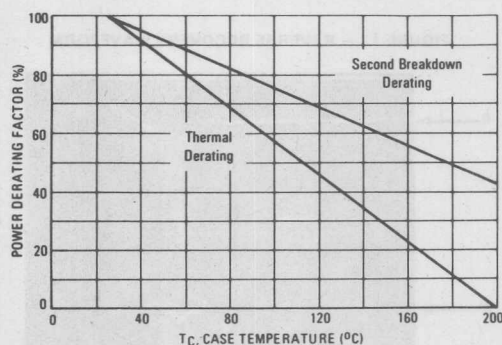


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 20. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

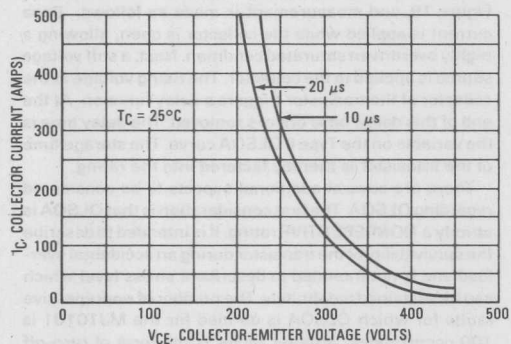
TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the MJ10101. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known,

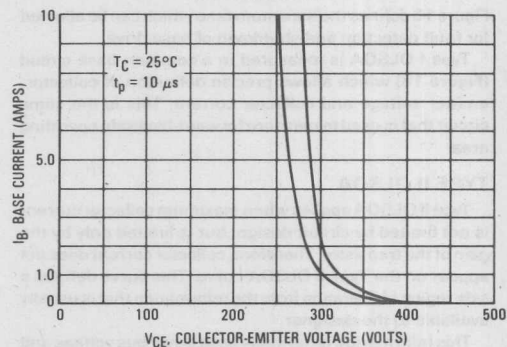
(continued on back page)

OVERLOAD CHARACTERISTICS

**FIGURE 16 — OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)**



**FIGURE 17 — OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)**



**FIGURE 18 — OVERLOAD SOA TEST CIRCUIT
TYPE I**

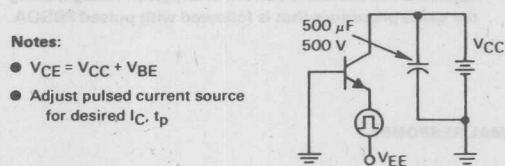
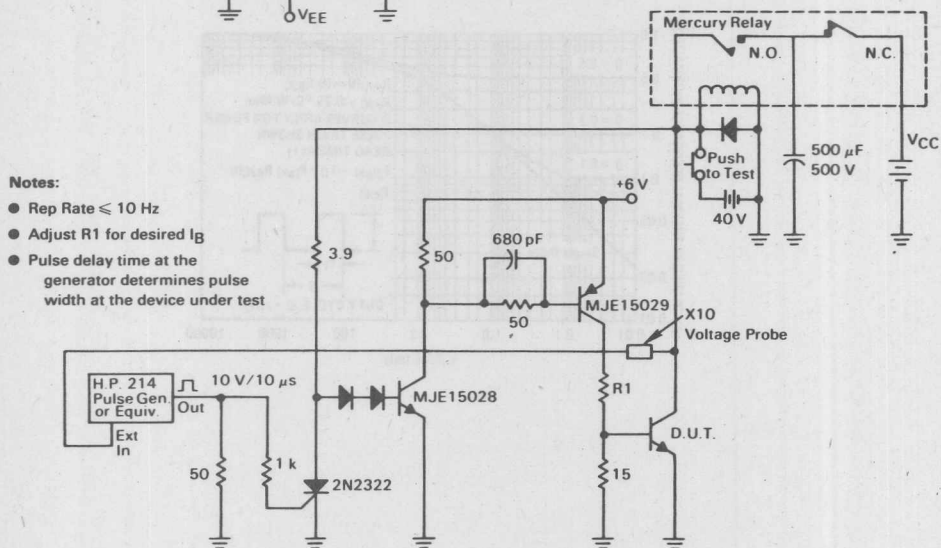


FIGURE 19 — OVERLOAD SOA TEST CIRCUIT
TYPE II



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as

shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the MJ10101 is 100 occurrences. Another factor is the form of turn-off bias. For the MJ10101, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

FIGURE 20 — THERMAL RESPONSE

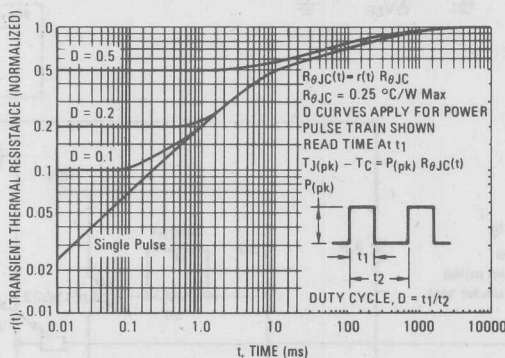


FIGURE 21

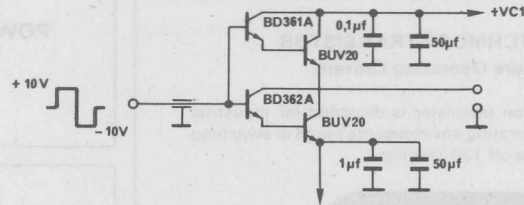


FIGURE 22

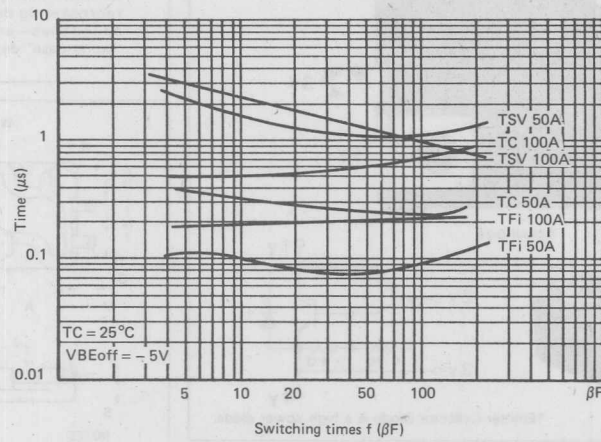
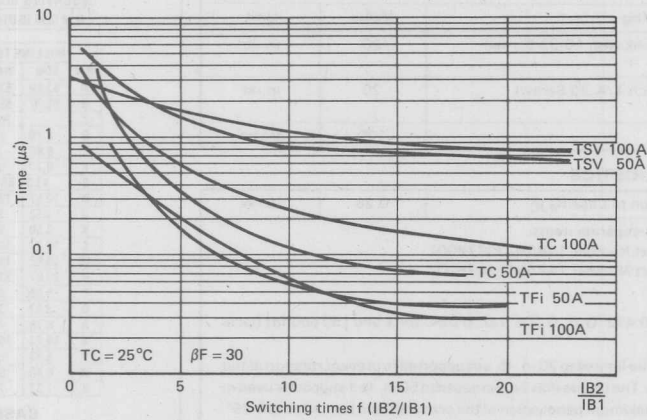


FIGURE 23

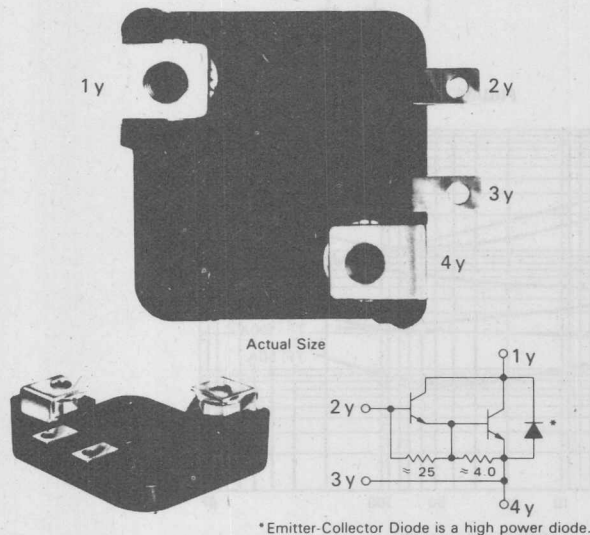




Designer's Data Sheet

50 KVA SWITCHMODE TRANSISTOR 200-Ampere Operating Current

The MJ10200 Darlington transistor is designed for industrial service under practical operating environments found in switching high power inductive loads off 120-Volt lines.



MAXIMUM RATINGS

Mechanical Ratings		
Rating	Value	Unit
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	$^{\circ}\text{C}/\text{W}$
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Mica Insulators available as separate items.
0.003" thick. Motorola Part Number 14ASB12387B001.
0.006" thick. Motorola Part Number 14ASB12387B002

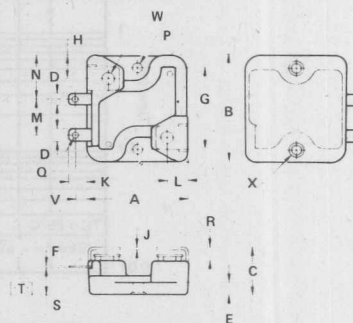
Notes:

1. A Belleville washer of 0.472" O.D., 0.205" I.D., 0.024" thick and 150 pounds flat is recommended.
2. The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75".

200 AMPERE NPN SILICON POWER DARLINGTON TRANSISTOR 250 VOLTS 500 WATTS

Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.



NOTES:

1. DIMENSION A AND B ARE DATUMS.
2. T IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:

$$\pm 0.036 (0.014) T A B$$

DIM	MIN	MAX	MIN	MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C		26.67		1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31	BSC	1.705	BSC
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01

MAXIMUM RATINGS (Continued)

Electrical Ratings			
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	250	Vdc
Collector-Emitter Voltage ($R_{BE} = 10 \text{ Ohms}$)	V_{CER}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Operating, $T_C = 50^\circ\text{C}$ — Continuous, $T_C = 25^\circ\text{C}$ — Peak Repetitive, $T_C = 25^\circ\text{C}$ — Peak Nonrepetitive, $T_C = 25^\circ\text{C}$	I_C	200 300 600 1000	A
Base Current — Continuous — Peak Nonrepetitive	I_B	50 100	A
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C For 1-minute overload	P_D	500 4.0 667	Watts W/ $^\circ\text{C}$ Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	-55 to +150 -55 to 200	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 250 \text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 300 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 300 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	—	—	2.0 10	mAdc
Collector Cutoff Current ($V_{CE} = 300 \text{ Vdc}$, $R_{BE} = 10 \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	10	mAdc
Emitter Cutoff Current ($V_{EB} = 4.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	650	mAdc

SAFE OPERATING AREA

Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figure 13
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figure 14
Overload SOA	OLSOA	See Figures 16 and 17

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 200 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 200 \text{ A}$, $V_{CE} = 10 \text{ V}$)	h_{FE}	75 90	— —	— —	— —
Collector-Emitter Saturation Voltage ($I_C = 200 \text{ Adc}$, $I_B = 5.5 \text{ A}$) ($I_C = 200 \text{ Adc}$, $I_B = 5.5 \text{ A}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— —	— —	2.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 200 \text{ Adc}$, $I_B = 5.5 \text{ Adc}$) ($I_C = 200 \text{ Adc}$, $I_B = 5.5 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	3.5 3.5	Vdc

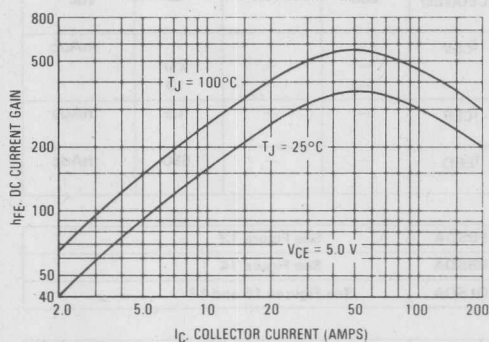
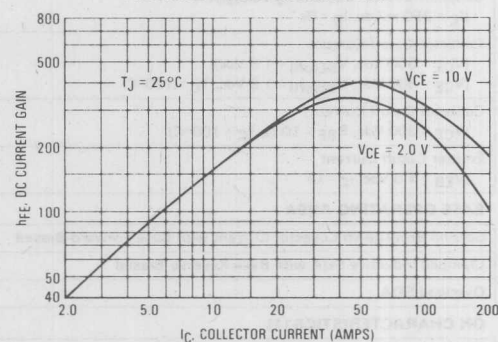
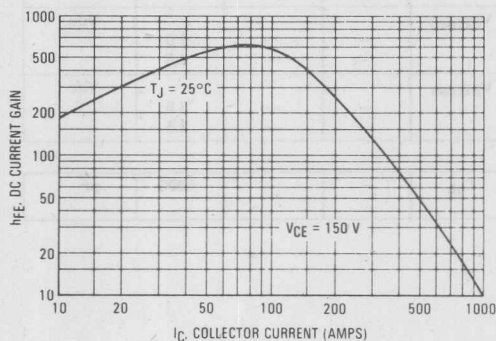
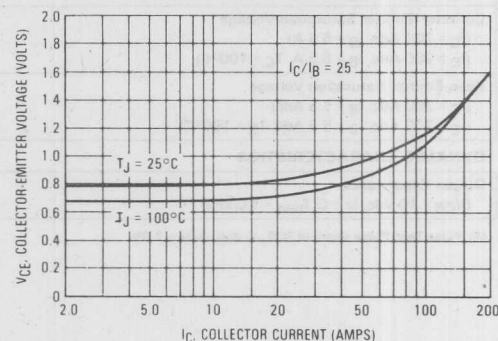
DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0 \text{ kHz}$)	C_{ob}	—	—	4000	pF
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(1) Pulse Test. Pulse width of 300 μs , duty cycle $\approx 2.0\%$.

ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit	
SWITCHING CHARACTERISTICS							
Resistive Load							
Delay Time	$(V_{CC} = 150 \text{ Vdc}, I_C = 200 \text{ A}, I_{B1} = 5.5 \text{ A},$ $R_{BE} = 10 \Omega, t_p = 50 \mu\text{s},$ $\text{Duty Cycle} \leq 2.0\%)$	t_d	—	0.035	0.25	μs	
Rise Time		t_r	—	1.2	4.0	μs	
Storage Time		t_s	—	6.3	20	μs	
Fall Time		t_f	—	2.5	8.0	μs	
Inductive Load, Clamped							
Storage Time	$(I_{CM} = 200 \text{ A},$ $V_{CEM} = 150 \text{ V}, R_{BE} = 10 \Omega,$ $I_{B1} = 5.5 \text{ A})$	$T_J = 100^\circ\text{C}$	t_{sv}	—	9.0	30	μs
Crossover Time		$T_J = 25^\circ\text{C}$	t_c	—	3.3	12	μs
Storage Time			t_{sv}	—	6.5	20	μs
Crossover Time			t_c	—	2.3	8.0	μs
C-E DIODE CHARACTERISTICS							
Power Dissipation ($I_B = 0$)		P_D	—	—	250	W	
Forward Voltage (1) ($I_F = 200 \text{ A}$)		V_F	—	1.4	2.0	V	
Reverse Recovery Time ($d_i/d_t = 25 \text{ A}/\mu\text{s}, I_F = 200 \text{ A}$)		t_{rr}	—	2.5	8.0	μs	
Forward Turn-On Time (Compliance Voltage = 250 V, $I_F = 100 \text{ A}$)		t_{on}	—	1.0	3.5	μs	
Single Cycle Surge Current ($f = 60 \text{ Hz}$)		I_{FSM}	—	—	500	A	

(1) Pulse Test. Pulse width of 300 μs , duty cycle $\leq 2.0\%$.**TYPICAL ELECTRICAL CHARACTERISTICS****FIGURE 1 — DC CURRENT GAIN****FIGURE 2 — DC CURRENT GAIN****FIGURE 3 — DC CURRENT GAIN****FIGURE 4 — COLLECTOR SATURATION REGION**

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

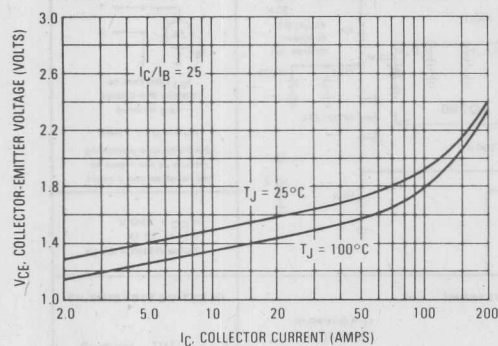
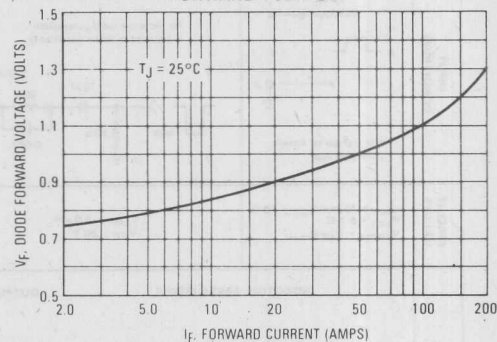


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

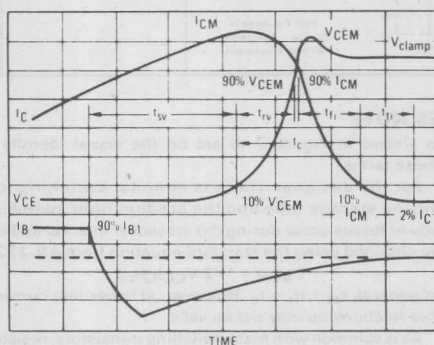


FIGURE 8 — TYPICAL INDUCTIVE SWITCHING TIMES

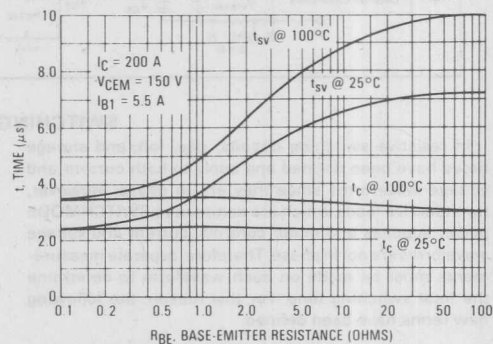


FIGURE 9 — TYPICAL TURN-ON SWITCHING TIMES

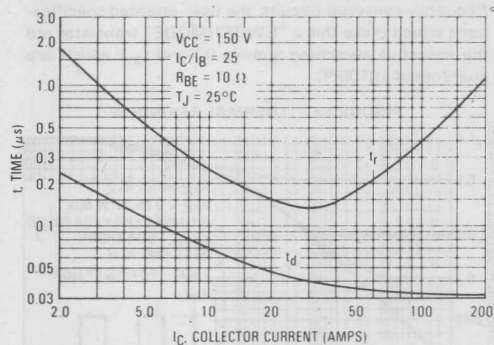


FIGURE 10 — TURN-OFF SWITCHING TIMES

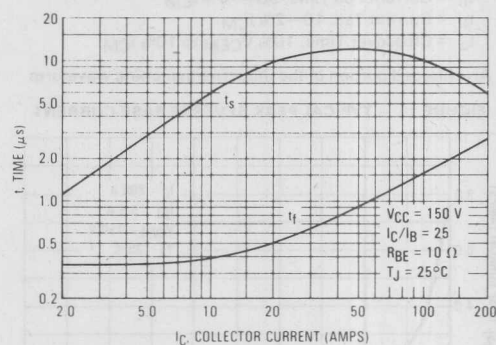


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO} (sus)	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain I_C = 250 mA</p>	<p>DRIVER SCHEMATIC</p> <p>For inductive loads pulse width is adjusted to obtain specified I_C</p>	<p>TURN ON TIME</p> <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME</p> <p>Use inductive switching circuit as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 10 mH V_{CC} = 10 V</p> <p>R_{coil} = 0.7 Ω</p> <p>V_{clamp} = V_{CEO}(sus)</p>	<p>L_{coil} = 3.0 μH</p> <p>V_{CC} = 20 V</p>	<p>V_{CC} = 150 V</p> <p>R_L = .75 Ω</p> <p>Pulse Width = 25 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> $t_1 = \frac{L_{coil} (I_{CM})}{V_{CC}}$ $t_2 = \frac{L_{coil} (I_{CM})}{V_{clamp}}$ <p>Test Equipment Scope Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

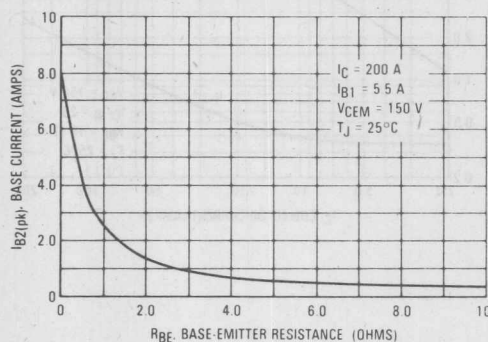
SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{RV} = Voltage Rise Time, 10—90% V_{CEM}
- t_{fi} = Current Fall Time, 90—10% I_{CM}
- t_{ti} = Current Tail, 10—2% I_{CM}
- t_C = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform

FIGURE 11 — TYPICAL PEAK REVERSE BASE CURRENT



is shown in Figure 7 to aid on the visual identity of these terms.

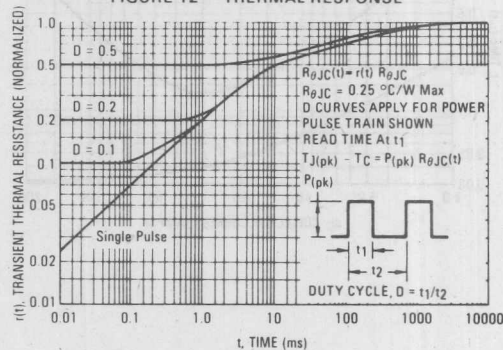
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_C) f$$

In general, t_{rv} + t_{fi} = t_C. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_C and t_{SV}) which are guaranteed at 100°C.

FIGURE 12 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

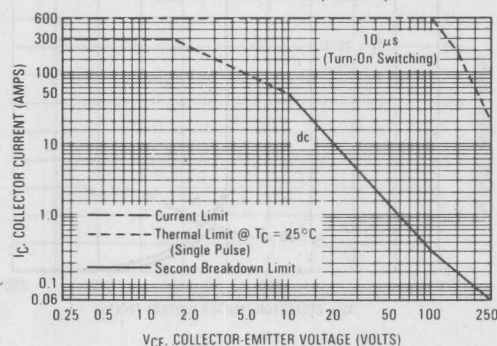


FIGURE 14 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

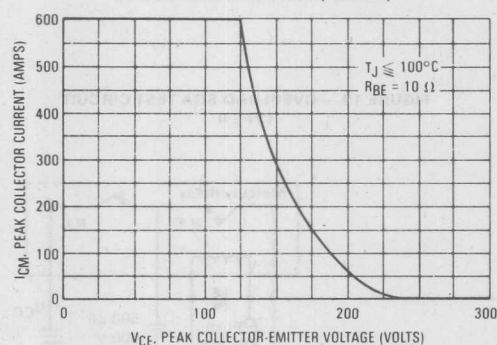
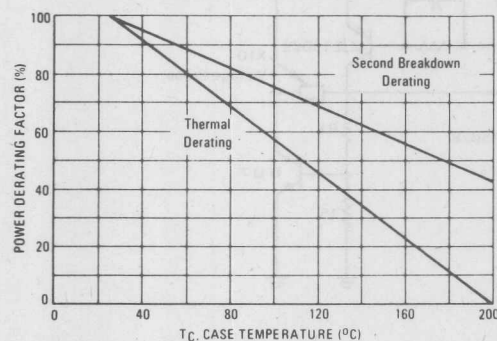


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the MJ10200. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known,

(continued on back page)

OVERLOAD CHARACTERISTICS

FIGURE 16 — RATED OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)

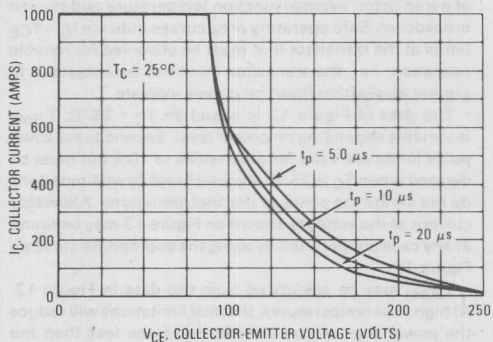


FIGURE 17 -- RATED OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)

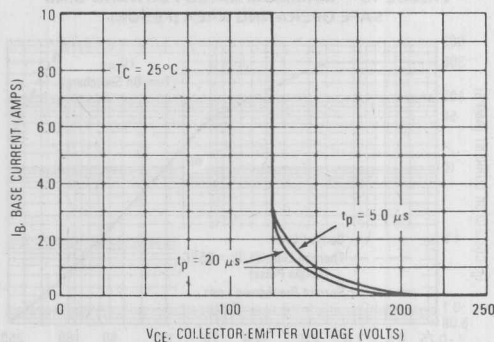


FIGURE 18 — OVERLOAD SOA TEST CIRCUIT
TYPE I

- Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C , t_p

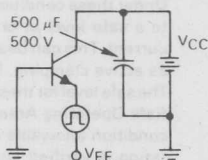


FIGURE 19 — OVERLOAD SQA TEST CIRCUIT
TYPE II

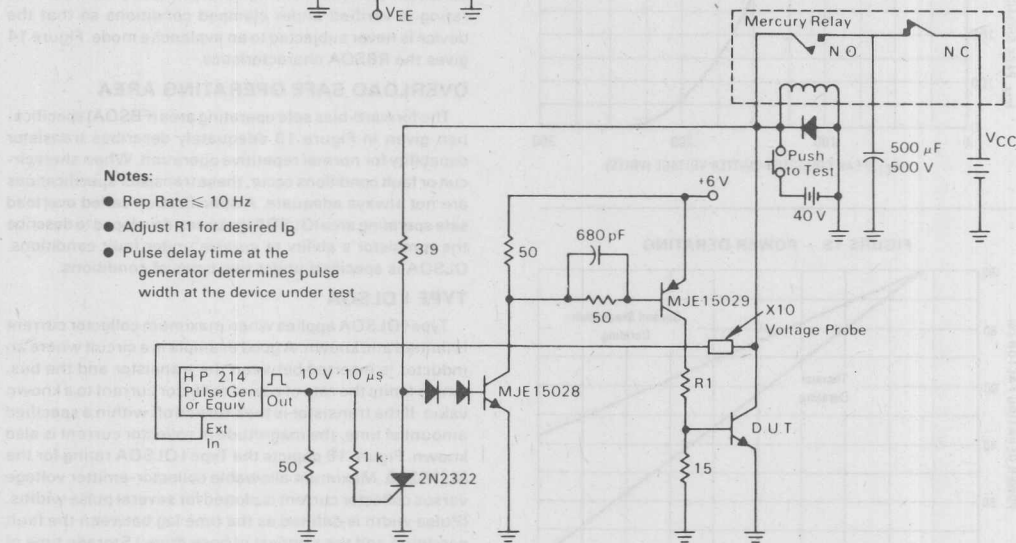
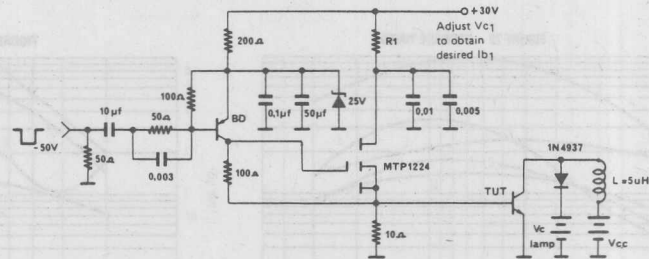
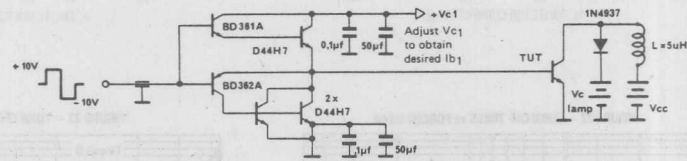


TABLE 2 — TYPICAL SWITCHING CHARACTERISTICS vs BASE DRIVE CIRCUITS

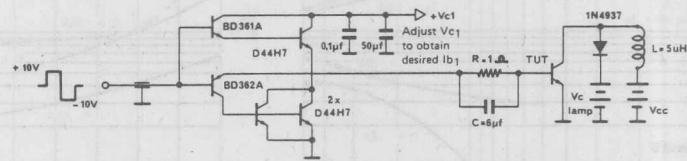
CIRCUIT A



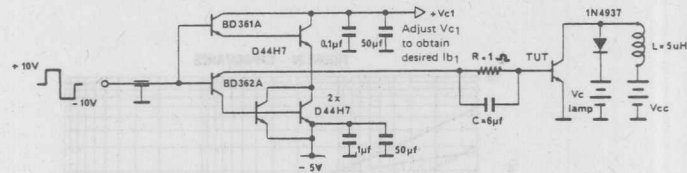
CIRCUIT B



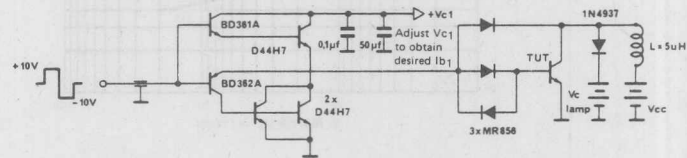
CIRCUIT C



CIRCUIT D



CIRCUIT E



TYPICAL SWITCHING CHARACTERISTICS vs BASE DRIVE CIRCUITS

FIGURE 20 - STORAGE TIMES

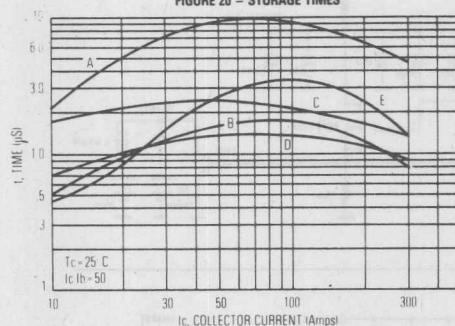


FIGURE 21 - FALL TIMES

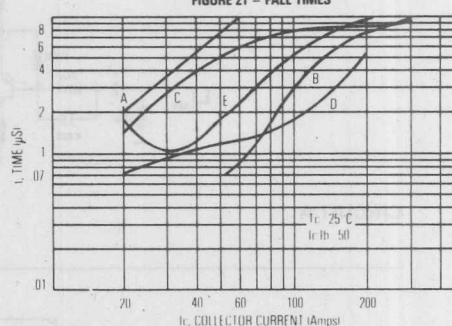


FIGURE 22 - TURN-OFF TIMES vs FORCED GAIN

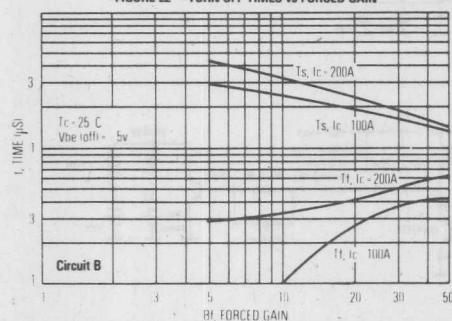
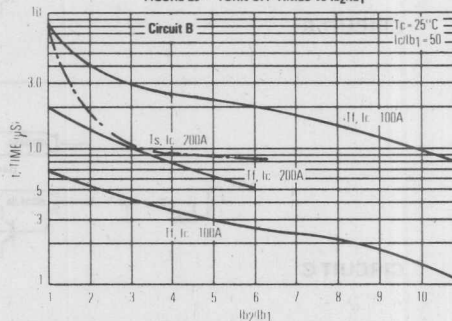
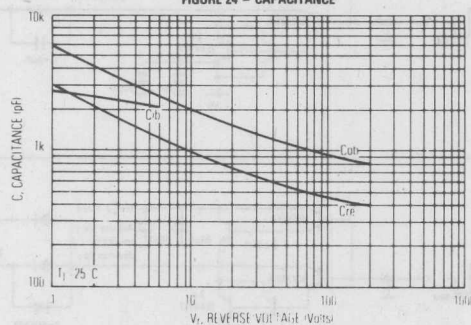
FIGURE 23 - TURN-OFF TIMES vs I_b/I_b1 

FIGURE 24 - CAPACITANCE



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as

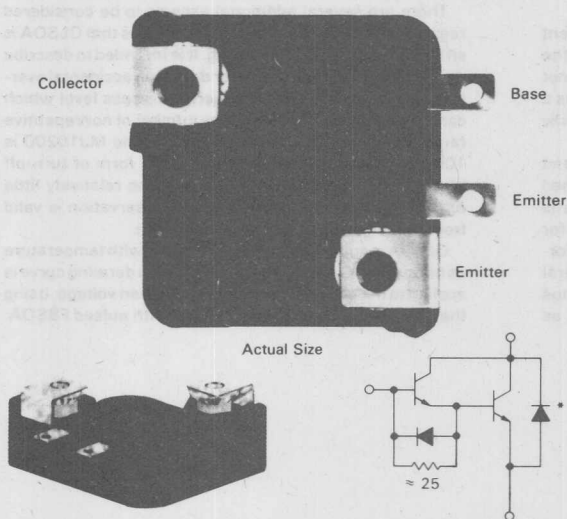
shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the MJ10200 is 100 occurrences. Another factor is the form of turn-off bias. For the MJ10200, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

**MOTOROLA****MJ10201
MJ10202****Designer's Data Sheet****50 KVA HIGH SPEED SWITCHMODE TRANSISTOR
200-Ampere Operating Current**

The MJ10201 Darlington transistor is designed for industrial service under practical operating environments requiring fast switching speed for highly efficient systems operating at high frequency such as inverters, PWM controllers and other high frequency system operating from 120 V lines or batteries.



*Emitter-Collector Diode is a fast recovery, high power diode.

MAXIMUM RATINGS**Mechanical Ratings**

Rating	Value	Unit
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	$^{\circ}\text{C}/\text{W}$
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Mica Insulators available as separate items.
0.003" thick. Motorola Part Number B12387B001.
0.006" thick. Motorola Part Number B12387B002.

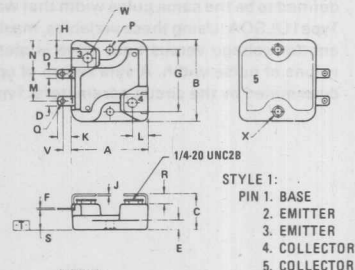
Notes:

1. A Belleville washer of 0.472" O.D., 0.205" I.D., 0.024" thick and 150 pounds flat is recommended such as P/N AM125206 available from National Disc Spring Div., 385 Hillside Ave., Hillside N.J. 07205.
2. The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75".

**200 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
200 and 250 VOLTS
500 WATTS**

**Designer's Data for
"Worst-Case" Conditions**

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.

**NOTES:**

1. DIMENSION A AND B ARE DATUMS.
2. \square IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
 $\phi 0.36 (0.014) \text{ (M)} \text{ T A (M) B (M)}$
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	—	26.67	—	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31	BSC	1.705	BSC
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.67	0.290	0.310

CASE 346-01

MAXIMUM RATINGS (Continued)

Electrical Ratings				
Rating		Symbol	Value	Unit
Collector-Emitter Voltage	MJ10201	V_{CEO}	250	Vdc
	MJ10202		200	
Collector-Emitter Voltage ($R_{BE} = 10 \text{ Ohms}$)		V_{CER}	300	Vdc
Collector-Base Voltage		V_{CB}	300	Vdc
Emitter-Base Voltage		V_{EB}	8.0	Vdc
Collector Current — Operating, $T_C = 50^\circ\text{C}$ — Continuous, $T_C = 25^\circ\text{C}$ — Peak Repetitive, $T_C = 25^\circ\text{C}$ — Peak Nonrepetitive, $T_C = 25^\circ\text{C}$		I_C	200	A
			300	
			600	
			1000	
Base Current — Continuous — Peak Nonrepetitive		I_B	50	A
			100	
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C For 1-minute overload		P_D	500	Watts
			4.0	W/ $^\circ\text{C}$
			667	Watts
Operating Junction and Storage Temperature Range For 1-minute overload		T_J, T_{stg}	-55 to +150 -55 to +200	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 250 \text{ mAdc}, I_B = 0$)	$V_{CEO(sus)}$	250 200	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 500 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 500 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	2.0 10	mAdc
Emitter Cutoff Current ($V_{EB} = 4.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	—	5.0	mAdc

SAFE OPERATING AREA

Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figure 13
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figure 14
Overload SOA	OLSOA	See Figures 16 and 17

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 200 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 200 \text{ A}, V_{CE} = 10 \text{ V}$)	h_{FE}	75 90	— —	— —	
Collector-Emitter Saturation Voltage ($I_C = 200 \text{ Adc}, I_B = 5.5 \text{ A}$) ($I_C = 200 \text{ Adc}, I_B = 5.5 \text{ A}, T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— —	— —	2.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 200 \text{ Adc}, I_B = 5.5 \text{ Adc}$) ($I_C = 200 \text{ Adc}, I_B = 5.5 \text{ Adc}, T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	3.5 3.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f_{test} = 1.0 \text{ kHz}$)	C_{ob}	—	—	4000	pF
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(1) Pulse Test. Pulse width of 300 μs , duty cycle $\leq 2.0\%$.

ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit		
SWITCHING CHARACTERISTICS							
Resistive Load							
Delay Time	$(V_{CC} = 150\text{ Vdc}, I_C = 200\text{ A}, I_{B1} = 5.5\text{ A},$ $t_p = 50\text{ }\mu\text{s}, V_{BE(off)} = 5.0\text{ V},$ Duty Cycle $\leq 2.0\%$)	t_d	—	0.035	μs		
Rise Time		t_r	—	1.2	4.0	μs	
Storage Time		t_s	—	1.4	4.0	μs	
Fall Time		t_f	—	0.25	1.0	μs	
Inductive Load, Clamped							
Storage Time	$(I_{CM} = 200\text{ A},$ $V_{CEM} = 150\text{ V}, I_{B1} = 5.5\text{ A},$ $I_{B2} = 5.5\text{ A})$	$T_J = 100^\circ\text{C}$	t_{sv}	—	2.8	8.0	μs
Crossover Time		$T_J = 100^\circ\text{C}$	t_c	—	1.4	4.0	μs
Storage Time		$T_J = 25^\circ\text{C}$	t_{sv}	—	2.2	6.5	μs
Crossover Time		$T_J = 25^\circ\text{C}$	t_c	—	1.0	3.0	μs
C-E DIODE CHARACTERISTICS							
Power Dissipation ($I_B = 0$)		P_D	—	—	250	W	
Forward Voltage (1) ($I_F = 200\text{ A}$)		V_F	—	2.5	5.0	V	
Reverse Recovery Time ($d_i/d_t = 25\text{ A}/\mu\text{s}, I_F = 200\text{ A}$)		t_{rr}	—	0.4	1.0	μs	
Forward Turn-On Time (Compliance Voltage = 200 V, $I_F = 100\text{ A}$)		t_{on}	—	0.4	1.0	μs	
Single Cycle Surge Current ($f = 60\text{ Hz}$)		I_{FSM}	—	—	500	A	
Reverse Recovery Current ($I_F = 200\text{ A}, d_i/d_t = 200\text{ A}/\mu\text{s}$)		$I_{RM(REC)}$	—	50	100	A	

(1) Pulse Test. Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2.0\%$.**TYPICAL ELECTRICAL CHARACTERISTICS**

FIGURE 1 — DC CURRENT GAIN

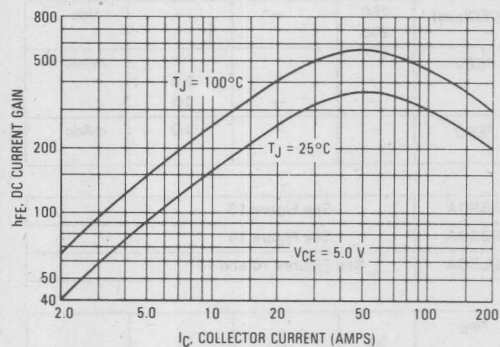


FIGURE 2 — DC CURRENT GAIN

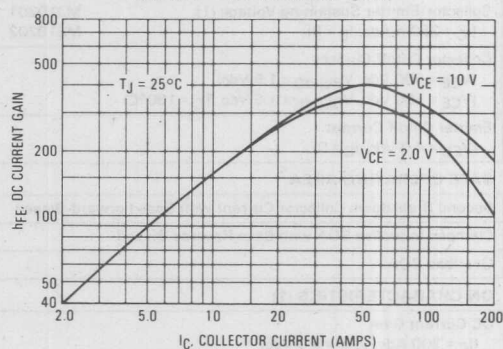


FIGURE 3 — DC CURRENT GAIN

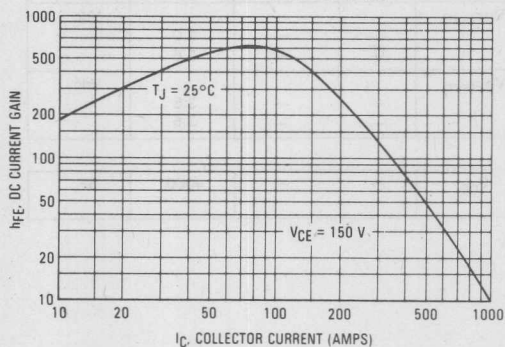
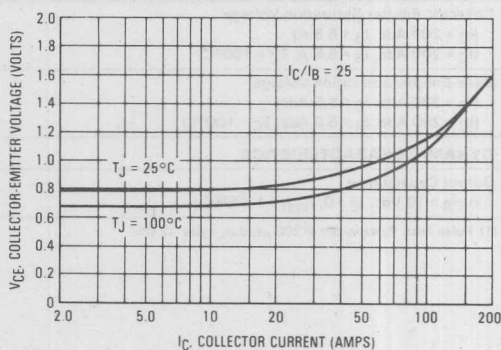


FIGURE 4 — COLLECTOR SATURATION REGION



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

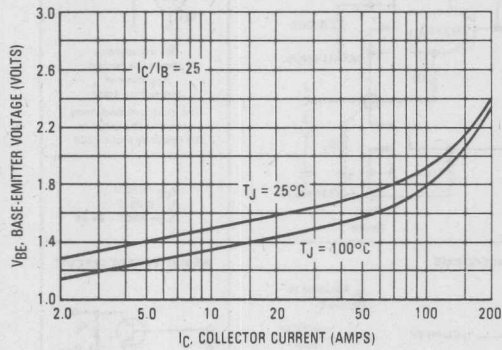
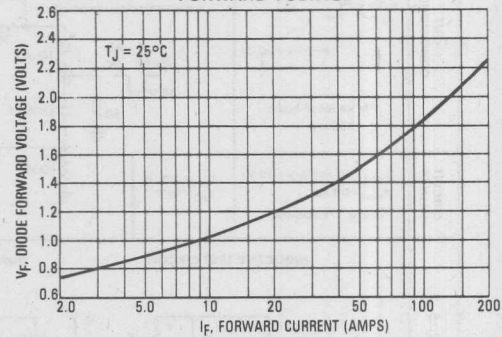


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

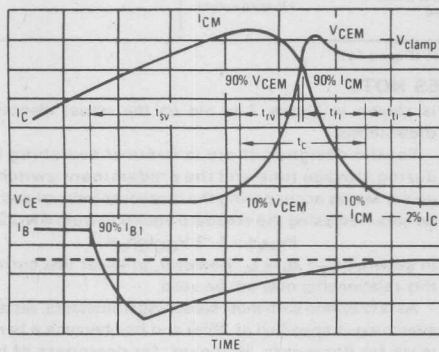


FIGURE 8 — INDUCTIVE SWITCHING TIMES

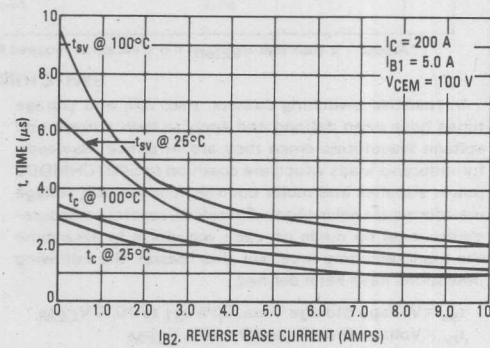


FIGURE 9 — TYPICAL TURN-ON SWITCHING TIMES

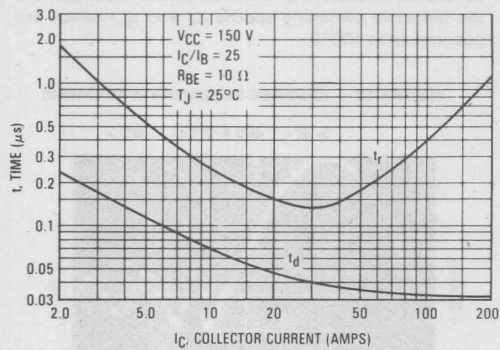


FIGURE 10 — TURN-OFF SWITCHING TIMES

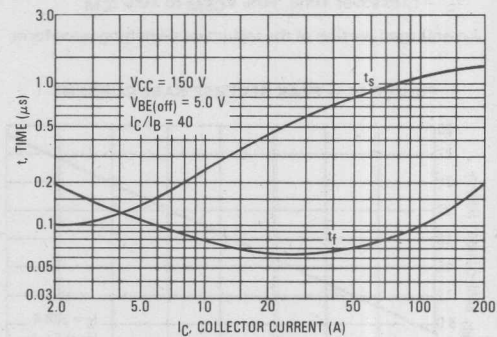
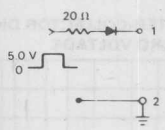
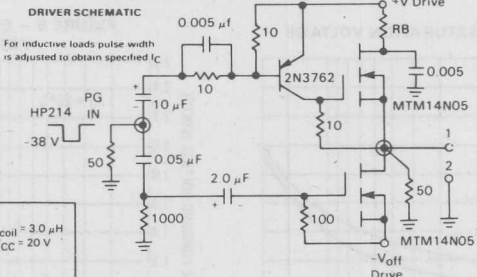
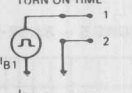
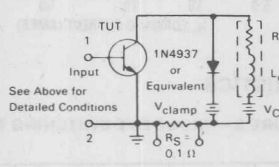
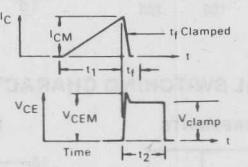
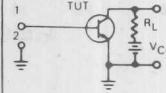


TABLE 1 — RBSOA AND INDUCTIVE SWITCHING DRIVER SCHEMATIC

	V _{CEO} (sus)	RBSOA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 250 mA</p>	DRIVER SCHEMATIC For inductive loads pulse width is adjusted to obtain specified I _C 		TURN ON TIME  <p>I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching circuit as the input to the resistive test circuit</p>
CIRCUIT VALUES	L _{coil} = 10 mH V _{CC} = 10 V R _{coil} = 0.7 Ω V _{clamp} = V _{CEO} (sus)	L _{coil} = 3.0 μH V _{CC} = 20 V		V _{CC} = 150 V R _L = 0.75 Ω Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  <p>See Above for Detailed Conditions R_S = 0.1 Ω</p>	OUTPUT WAVEFORMS  <p>t₁ Adjusted to Obtain I_C $t_1 = \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_1 = \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent</p>		RESISTIVE TEST CIRCUIT 

*Adjust — V such that $V_{BE(off)} = 5$ V except as required for RBSOA (Figure 14).

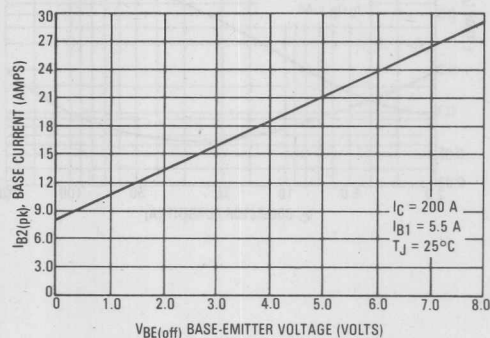
SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{rV} = Voltage Rise Time, 10—90% V_{CEM}
- t_{fi} = Current Fall Time, 90—10% I_{CM}
- t_{ti} = Current Tail, 10—2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform

FIGURE 11 — PEAK REVERSE BASE CURRENT



is shown in Figure 7 to aid on the visual identity of these terms.

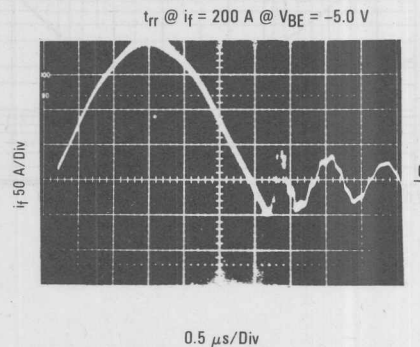
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rV} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{SV}) which are guaranteed at 100°C.

FIGURE 12 — REVERSE RECOVERY WAVEFORM



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

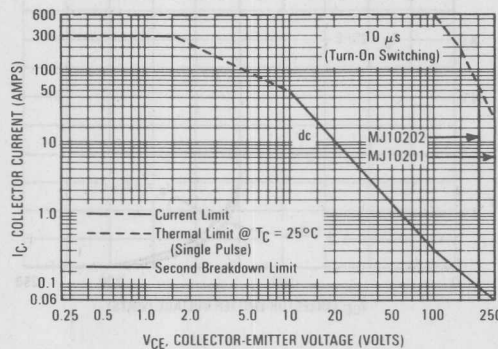


FIGURE 14 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA (RBSOA)

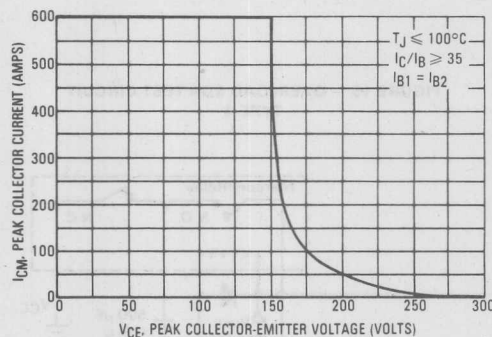
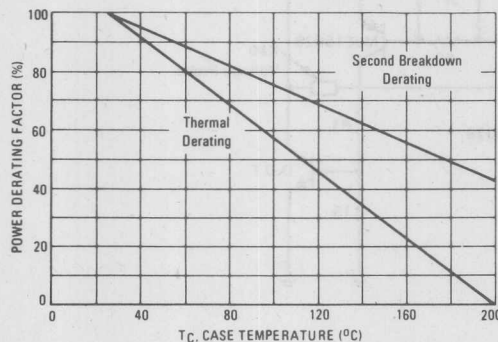


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 20. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the devices. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known,

(continued on back page)

OVERLOAD CHARACTERISTICS

FIGURE 16 — RATED OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)

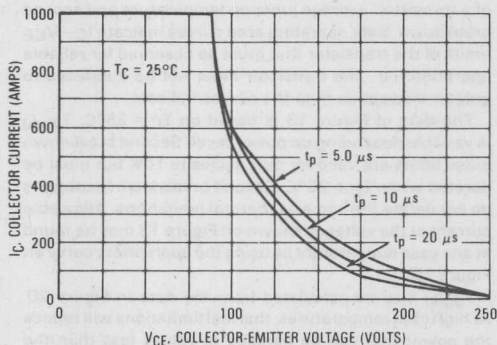


FIGURE 17 — RATED OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)

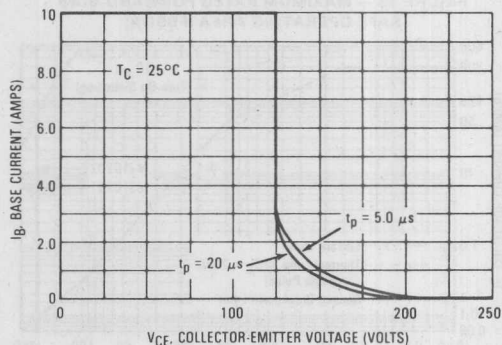


FIGURE 18 — OVERLOAD SOA TEST CIRCUIT
TYPE I

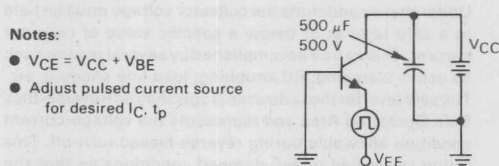
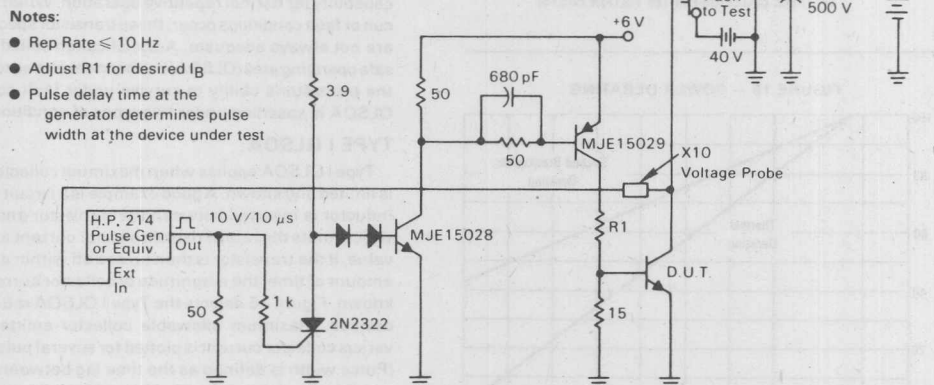


FIGURE 19 — OVERLOAD SOA TEST CIRCUIT
TYPE II



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as

shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the devices are 100 occurrences. Another factor is the form of turn-off bias. For the devices, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

FIGURE 20 — THERMAL RESPONSE

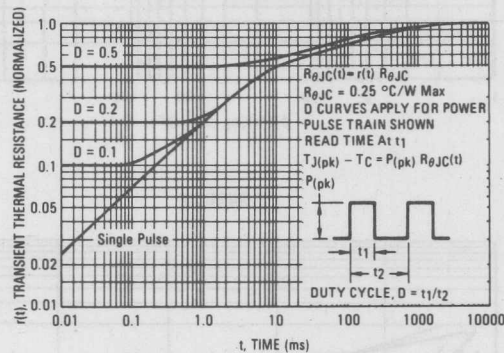


FIGURE 21

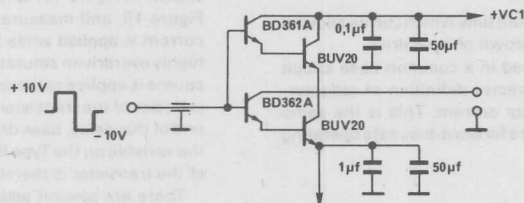


FIGURE 22

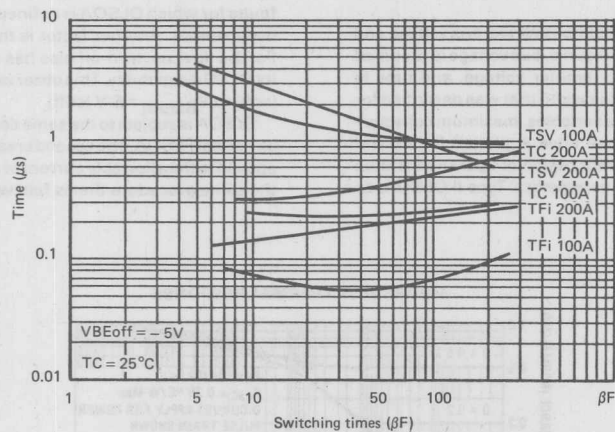
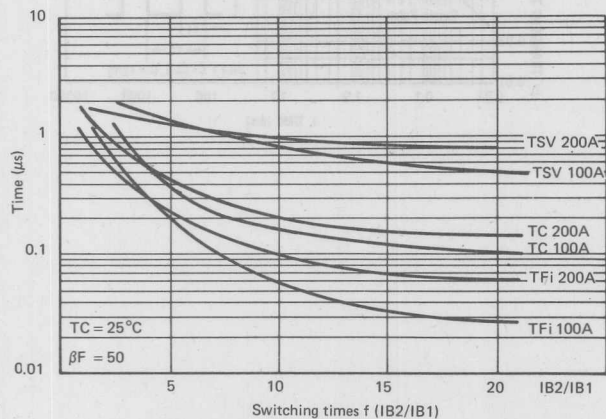


FIGURE 23





Designer's Data Sheet

SWITCHMODE III SERIES NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16004 is a selected high-gain version of the MJ16002 for applications where drive current is limited.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 50 ns Inductive Fall Time — 75°C (Typ)
 - 70 ns Inductive Crossover Time — 75°C (Typ)
 - 500 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
— Peak (1)	I_{CM}	10	
Base Current — Continuous	I_B	4.0	Adc
— Peak (1)	I_{BM}	8.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125	Watts
— @ $T_C = 100^\circ\text{C}$		71.5	
Derate above 25°C		0.714	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

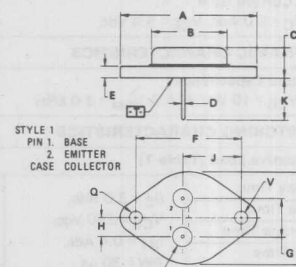
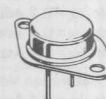
5 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
 2. \square IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.

FOR LEADS:
 $\phi .13 (0.005) \text{ T } V \text{ () } Q \text{ ()}$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.91	1.09	0.036	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3 TYPE



MJ16002

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.0 2.5 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	5.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	200	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	(I _C = 3.0 Adc, V _{CC} = 250 Vdc, I _{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I _{B2} = 0.8 Adc, R _{B2} = 8.0 Ω)	t _d	—	30	100	ns
Rise Time			t _r	—	100	300	
Storage Time			t _s	—	1000	3000	
Fall Time		(V _{BE(off)} = 5.0 Vdc)	t _f	—	60	300	
Storage Time			t _s	—	400	—	
Fall Time			t _f	—	130	—	
Inductive Load (Table 2)							
Storage Time	(I _C = 3.0 Adc, I _{B1} = 0.4 Adc, V _{BE(off)} = 5.0 Vdc, V _{CE(pk)} = 400 Vdc)	(T _J = 100°C)	t _{sv}	—	500	1600	ns
Fall Time			t _{fi}	—	100	200	
Crossover Time			t _c	—	120	250	
Storage Time		(T _J = 150°C)	t _{sv}	—	600	—	
Fall Time			t _{fi}	—	120	—	
Crossover Time			t _c	—	160	—	

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

$$\beta_{FI} = \frac{I_C}{I_{B1}}$$

MJ16004

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 0.15\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.0 2.5 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	200	pF
--	----------	---	---	-----	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$I_{IC} = 3.0\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 0.3\text{ Adc}$, $PW = 30\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$	$(I_{B2} = 0.6\text{ Adc}$, $R_{B2} = 8.0\text{ }\Omega)$	t_d	—	30	100	ns
Rise Time			t_r	—	130	300	
Storage Time			t_s	—	800	2700	
Fall Time			t_f	—	80	350	
Storage Time			t_s	—	250	—	
Fall Time	t_f		—	60	—		
		$(V_{BE(off)} = 5.0\text{ Vdc})$					

Inductive Load (Table 2)

Storage Time	$I_C = 3.0\text{ Adc}$, $I_{B1} = 0.3\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$	$(T_J = 100^\circ\text{C})$	t_{sv}	—	400	1300	ns
Fall Time			t_{fi}	—	80	150	
Crossover Time			t_c	—	90	200	
Storage Time		$(T_J = 150^\circ\text{C})$	t_{sv}	—	450	—	
Fall Time			t_{fi}	—	100	—	
Crossover Time			t_c	—	110	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

$$\beta_{fi} = \frac{I_C}{I_{B1}}$$

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

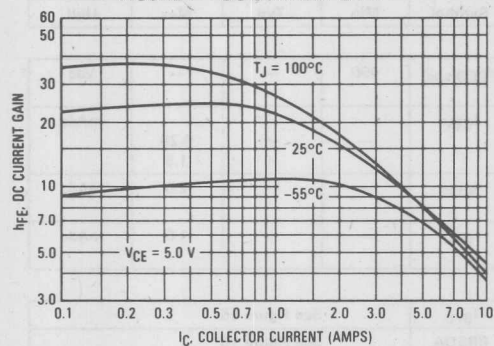


FIGURE 2 — COLLECTOR SATURATION REGION

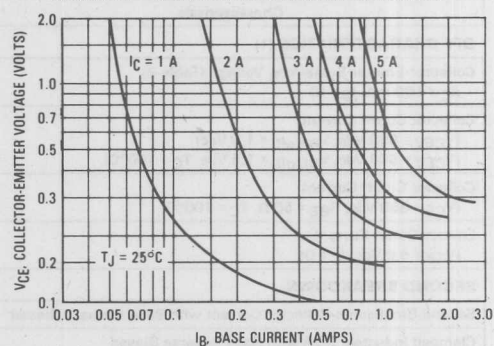


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

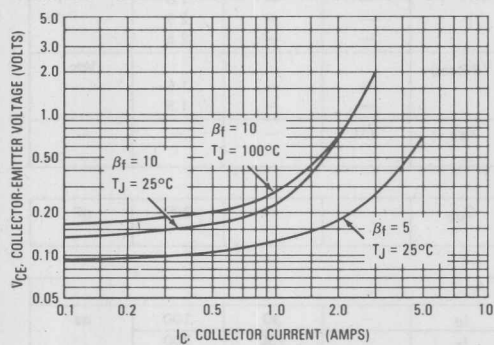


FIGURE 4 — BASE-EMITTER VOLTAGE

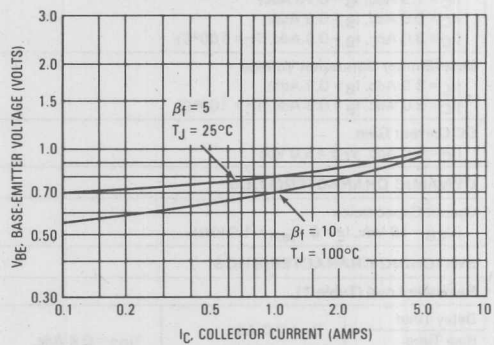


FIGURE 5 — COLLECTOR CUTOFF REGION

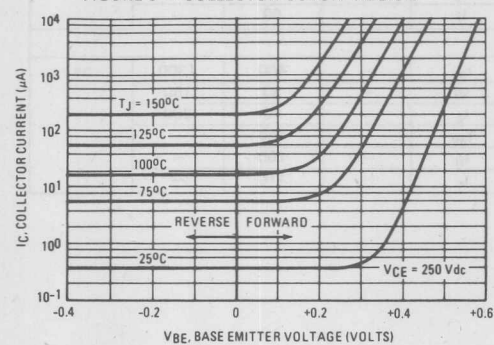
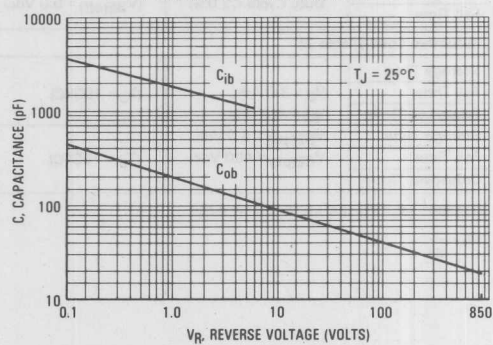


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

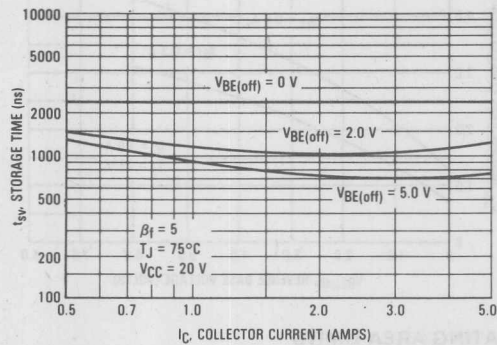


FIGURE 8 — STORAGE TIME

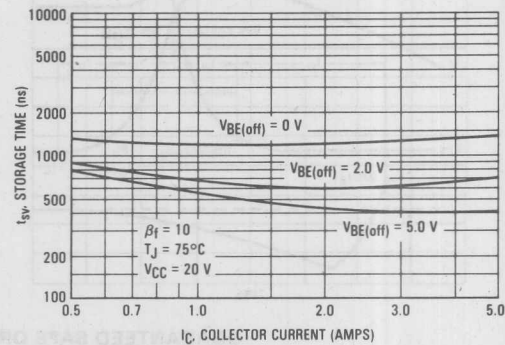


FIGURE 9 — COLLECTOR CURRENT FALL TIME

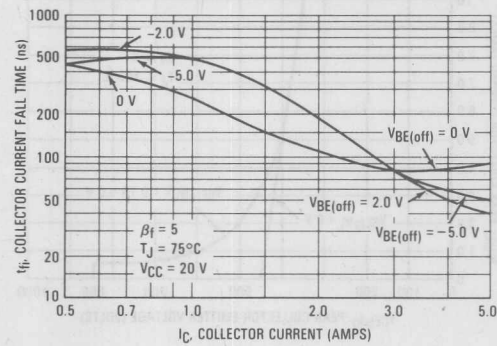


FIGURE 10 — COLLECTOR CURRENT FALL TIME

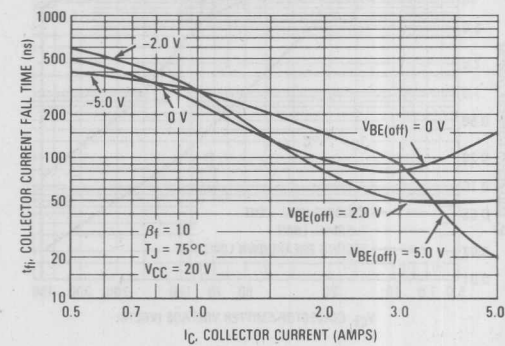


FIGURE 11 — CROSSOVER TIME

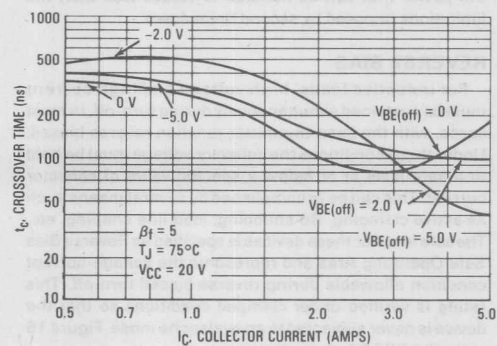


FIGURE 12 — CROSSOVER TIME

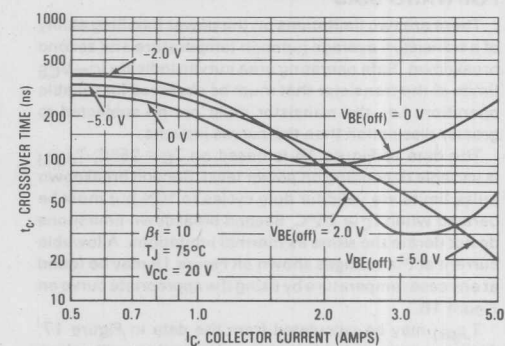


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

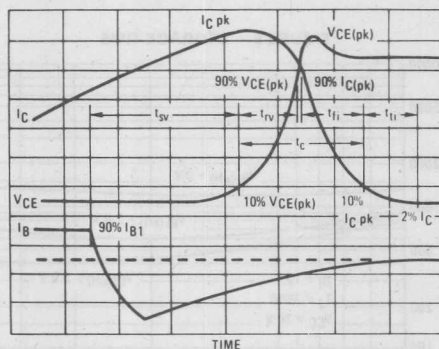
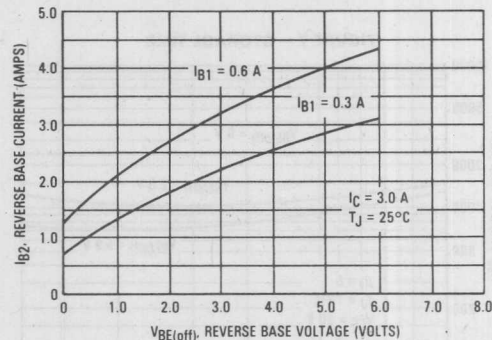


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

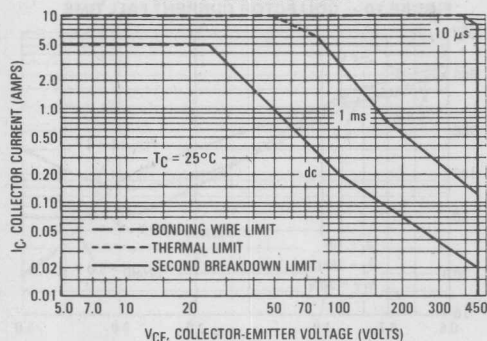
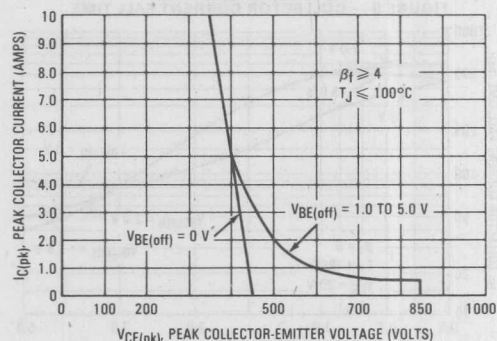


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce

the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

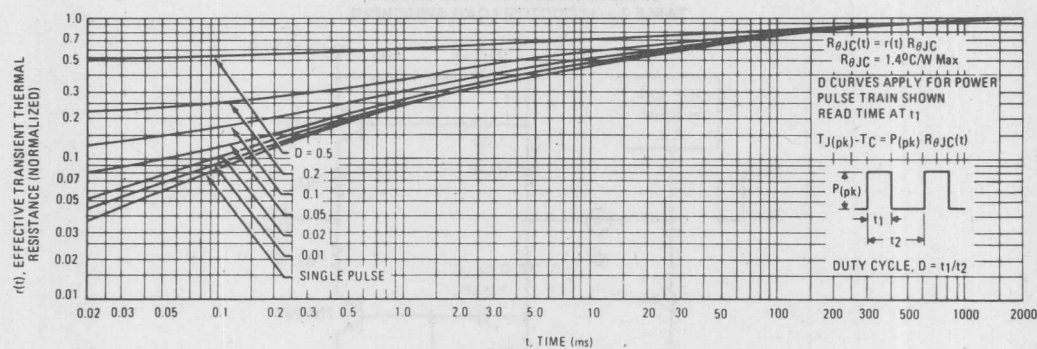


FIGURE 18 — POWER DERATING

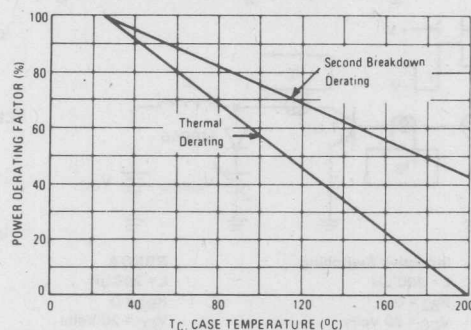
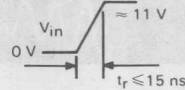
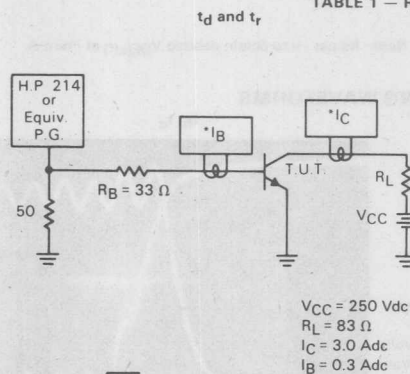
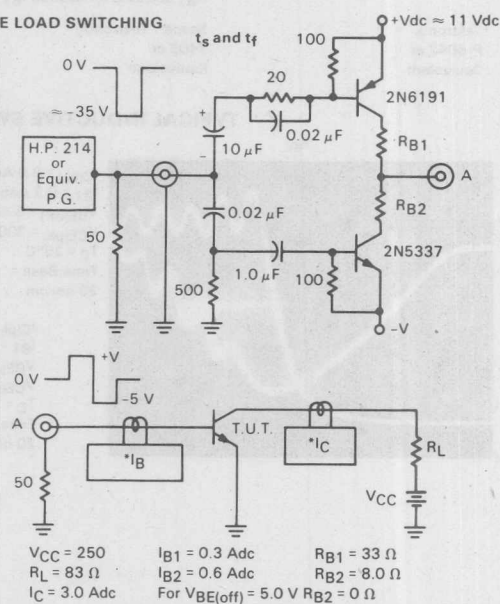


TABLE 1 — RESISTIVE LOAD SWITCHING



*Tektronix
P-6042 or
Equivalent



*Note: Adjust $-V$ to obtain desired $V_{BE(\text{off})}$ at Point A.



MOTOROLA

**MJ16006
MJ16008**

Designer's Data Sheet

SWITCHMODE III SERIES NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16008 is a selected high-gain version of the MJ16006 for applications where drive current is limited.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 90 ns Inductive Fall Time — 75°C (Typ)
 - 90 ns Inductive Crossover Time — 75°C (Typ)
 - 450 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
— Peak (1)	I_{CM}	16	
Base Current — Continuous	I_B	6.0	Adc
— Peak (1)	I_{BM}	12	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
@ $T_C = 100^\circ\text{C}$		85.5	
Derate above 25°C		0.86	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

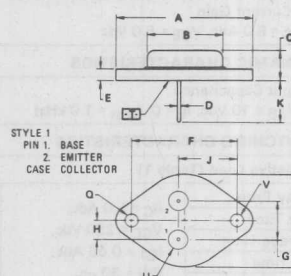
8 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
 2. \square IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
- FOR LEADS:
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.91	1.09	0.036	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	18.89 BSC		0.685 BSC	
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	26.67	—	1.050
N	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3 TYPE

MJ16006

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 0.66\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 0.66\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.66\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 0.66\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 8.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	5.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	350	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$(I_C = 5.0\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 0.66\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	$(I_{B2} = 1.3\text{ Adc}$, $R_{B2} = 4.0\ \Omega$)	t_d	—	20	50	ns
Rise Time			t_r	—	85	250	
Storage Time			t_s	—	1000	2500	
Fall Time			t_f	—	70	250	
Storage Time			t_s	—	500	—	
Fall Time			t_f	—	100	—	

Inductive Load (Table 2)

Storage Time	$(I_C = 5.0\text{ Adc}$, $I_{B1} = 0.66\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	$(T_J = 100^\circ\text{C})$	t_{sv}	—	700	1800	ns
Fall Time			t_{fi}	—	80	200	
Crossover Time			t_c	—	150	250	
Storage Time		$(T_J = 150^\circ\text{C})$	t_{sv}	—	800	—	
Fall Time			t_{fi}	—	80	—	
Crossover Time			t_c	—	200	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

$$*\beta_f = \frac{I_C}{I_{B1}}$$

MJ16008

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	$RBSOA$	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 0.5\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 0.5\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 8.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 1.0\text{ kHz}$)	C_{ob}	—	—	350	pF
---	----------	---	---	-----	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$(I_C = 5.0\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 0.5\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	$(I_{B2} = 1.0\text{ Adc}$, $R_{B2} = 4.0\ \Omega)$	t_d	—	20	50	ns
Rise Time			t_r	—	100	250	
Storage Time			t_s	—	900	2200	
Fall Time			t_f	—	70	250	
Storage Time		$(V_{BE(off)} = 5.0\text{ Vdc})$	t_s	—	400	—	
Fall Time			t_f	—	50	—	

Inductive Load (Table 2)

Storage Time	$(I_C = 5.0\text{ Adc}$, $I_{B1} = 0.5\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	$(T_J = 100^\circ\text{C})$	t_{sv}	—	500	1400	ns
Fall Time			t_{fi}	—	70	150	
Crossover Time			t_c	—	100	200	
Storage Time		$(T_J = 150^\circ\text{C})$	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	100	—	
Crossover Time			t_c	—	150	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

$$\beta_{\text{eff}} = \frac{I_C}{I_{B1}}$$

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

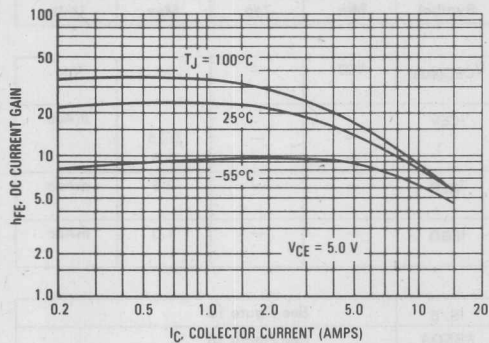


FIGURE 2 — COLLECTOR SATURATION REGION

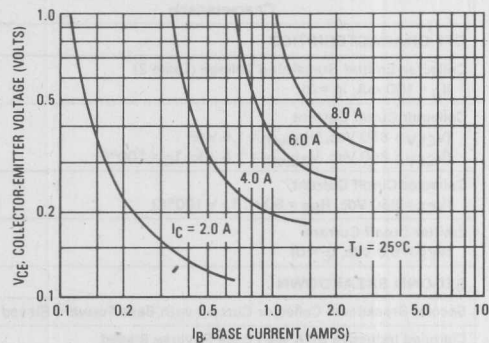


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

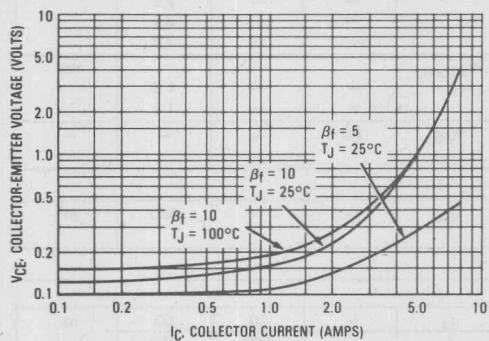


FIGURE 4 — BASE-EMITTER VOLTAGE

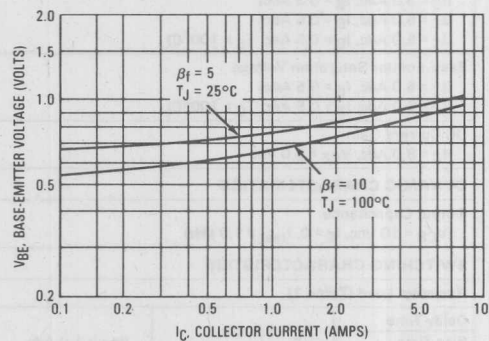


FIGURE 5 — COLLECTOR CUTOFF REGION

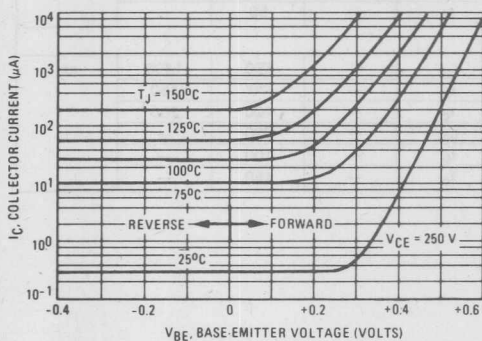
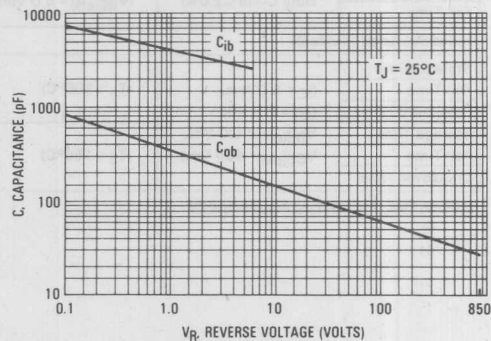


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

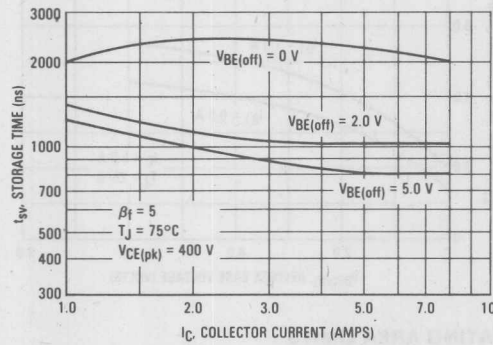


FIGURE 8 — STORAGE TIME

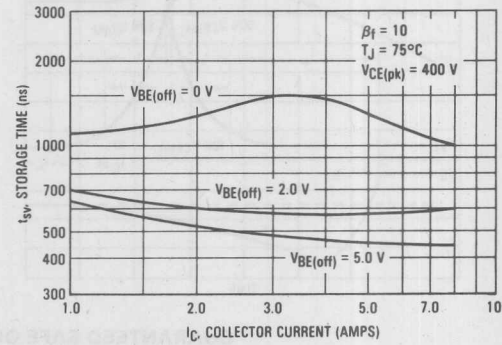


FIGURE 9 — COLLECTOR CURRENT FALL TIME

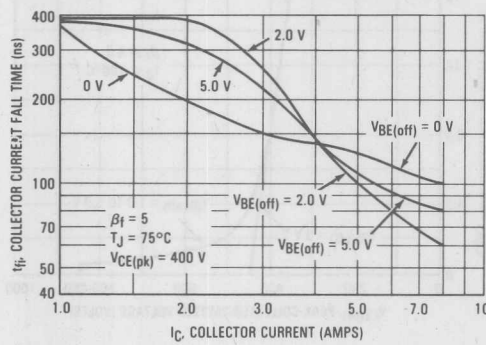


FIGURE 10 — COLLECTOR CURRENT FALL TIME

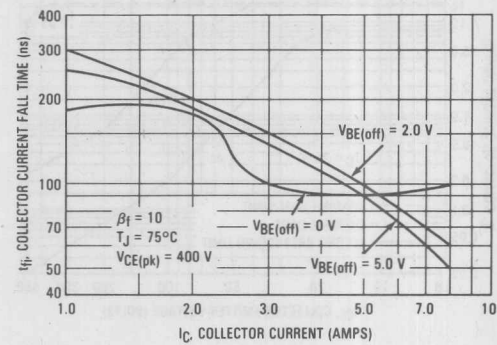


FIGURE 11 — CROSSOVER TIME

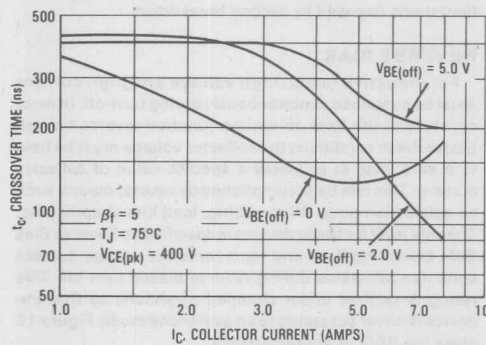


FIGURE 12 — CROSSOVER TIME

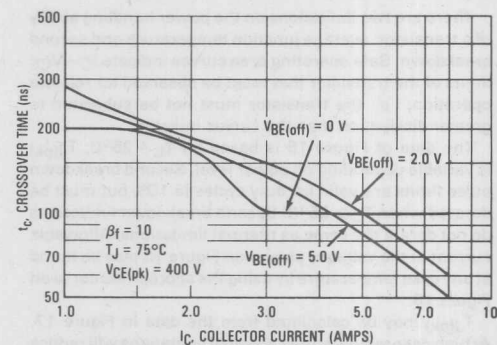


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

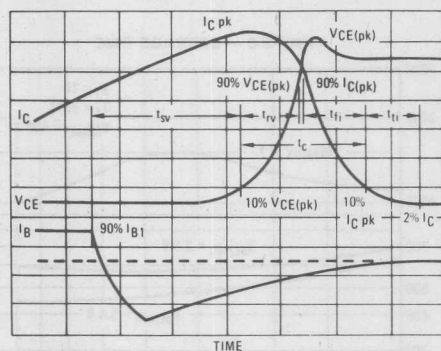
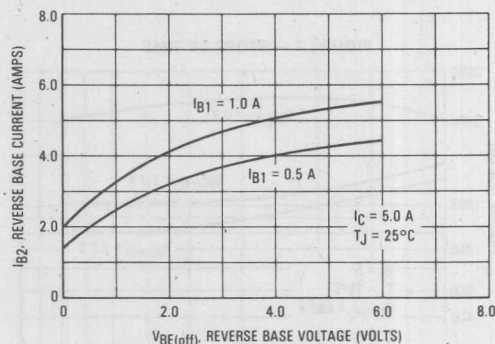
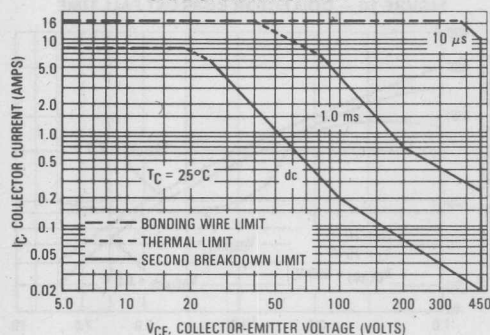
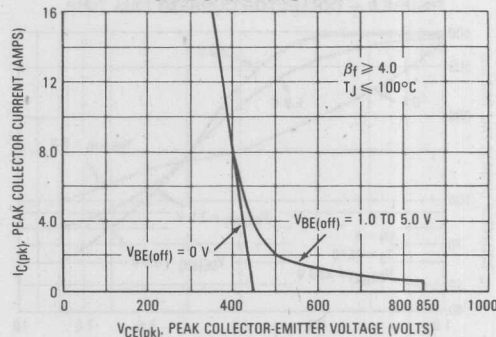


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS
SAFE OPERATING AREAFIGURE 16 — MAXIMUM REVERSE BIAS
SAFE OPERATING AREA

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_J(pk)$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce

the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 – THERMAL RESPONSE

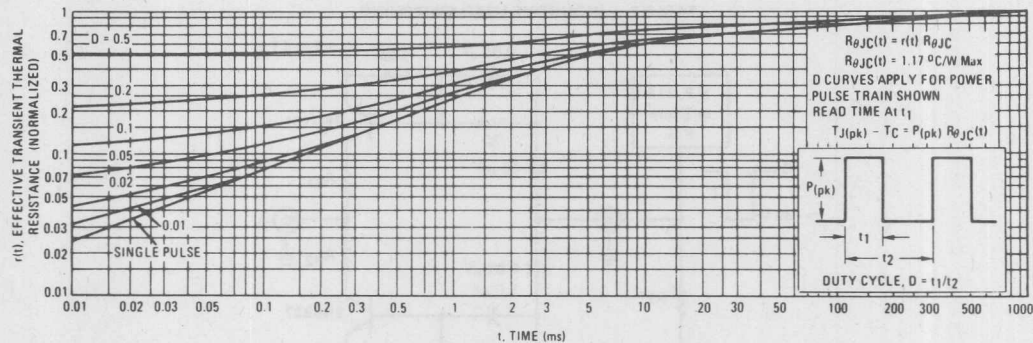


FIGURE 18 — POWER DERATING

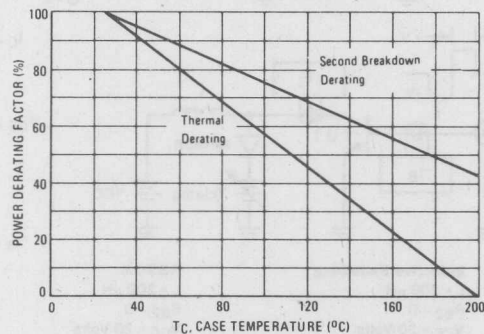
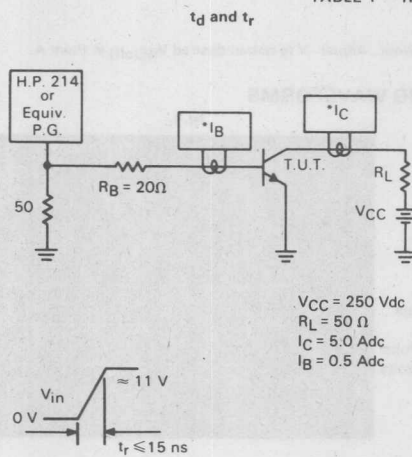
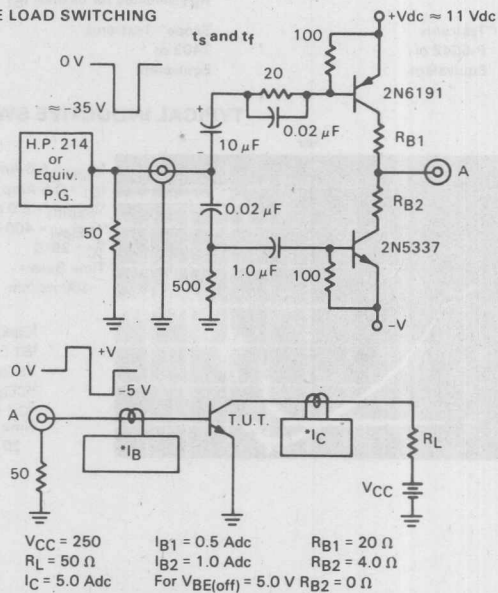


TABLE 1 — RESISTIVE LOAD SWITCHING

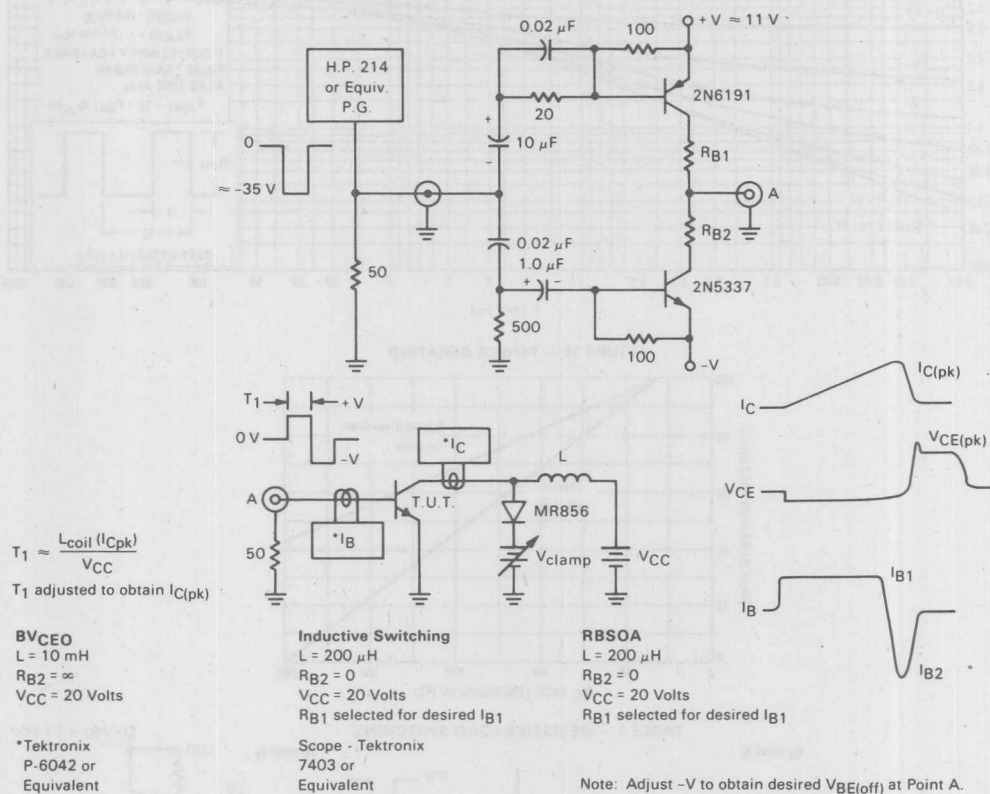


*Tektronix
P-6042 or
Equivalent



*Note: Adjust $-V$ to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



Designers Data Sheet

**SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS**

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16012 is a selected high-gain version of the MJ16010 for applications where drive current is limited.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 30 ns Inductive Fall Time — 75°C (Typ)
 - 50 ns Inductive Crossover Time — 75°C (Typ)
 - 600 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20.	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ @ $T_C = 100^\circ C$ Derate above $25^\circ C$	P_D	175 100 1.0	Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^{\circ}\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^{\circ}\text{C}$

(1) Pulse Test: Pulse Width = 5 ms. Duty Cycle = 10%

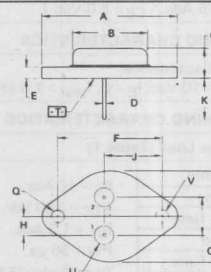
15 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



NOTES

1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Ø:

$\frac{1}{16}$	0.13 (0.005) M	T	V M
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FOR LEADS.

ϕ	$\phi.13 (0.005) \text{ (M) T}$	$V \text{ (M)}$	Q
--------	---------------------------------	-----------------	-----

4. DIMENSIONS AND TOLERANCES PER
ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3 TYPE

MJ16010

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 2.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	1.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	$RBSOA$	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.7\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.3\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.3\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.3\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.3\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 15\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	5.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	400	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	$(I_C = 10\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 1.3\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	$(I_{B2} = 2.6\text{ Adc}$, $R_B = 1.6\ \Omega)$	t_d	—	20	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	1200	—	
Fall Time		$(V_{BE(off)} = 5.0\text{ Vdc})$	t_f	—	200	—	
Storage Time			t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	$(I_C = 10\text{ Adc}$, $I_{B1} = 1.3\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	$(T_C = 100^\circ\text{C})$	t_{sv}	—	800	1800	ns
Fall Time			t_{fi}	—	50	200	
Crossover Time			t_c	—	90	250	
Storage Time		$(T_C = 150^\circ\text{C})$	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

MJ16012

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 2.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	1.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 15\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 1.0\text{ kHz}$)	C_{ob}	—	—	400	pF
---	----------	---	---	-----	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$(I_C = 10\text{ Adc}, V_{CC} = 250\text{ Vdc}, I_{B1} = 1.0\text{ Adc}, PW = 30\ \mu\text{s}, \text{Duty Cycle} \leq 2.0\%)$	$(I_{B2} = 2.0\text{ Adc}, R_B = 1.6\ \Omega)$	t_d	—	20	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	900	—	
Fall Time			t_f	—	150	—	
Storage Time		$(V_{BE(off)} = 5.0\text{ Vdc})$	t_s	—	500	—	
Fall Time			t_f	—	40	—	

Inductive Load (Table 2)

Storage Time	$(I_C = 10\text{ Adc}, I_{B1} = 1.0\text{ Adc}, V_{BE(off)} = 5.0\text{ Vdc}, V_{CE(pk)} = 400\text{ Vdc})$	$(T_C = 100^\circ\text{C})$	t_{sv}	—	650	1500	ns
Fall Time			t_{fi}	—	30	150	
Crossover Time		$(T_C = 150^\circ\text{C})$	t_c	—	50	200	
Storage Time			t_{sv}	—	850	—	
Fall Time			t_{fi}	—	30	—	
Crossover Time			t_c	—	70	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

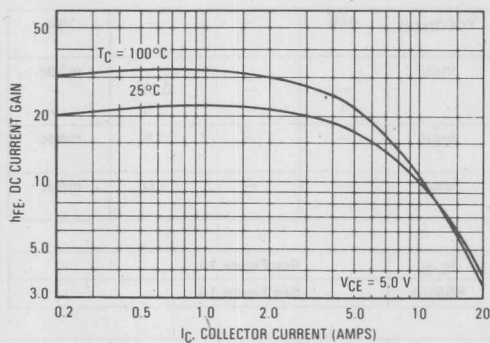


FIGURE 2 — COLLECTOR SATURATION REGION

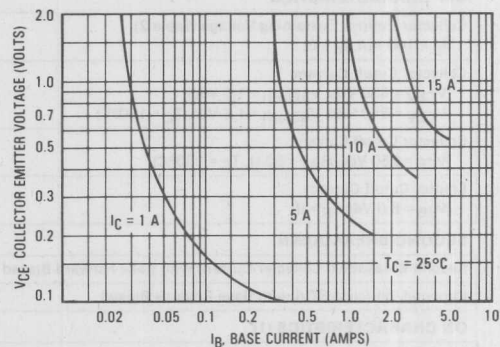


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

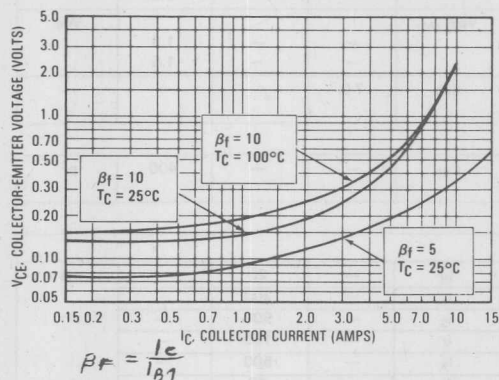


FIGURE 4 — BASE-EMITTER VOLTAGE

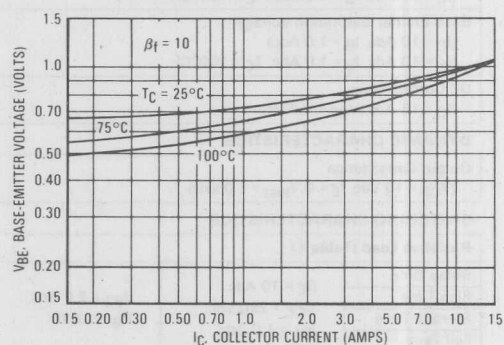


FIGURE 5 — COLLECTOR CUTOFF REGION

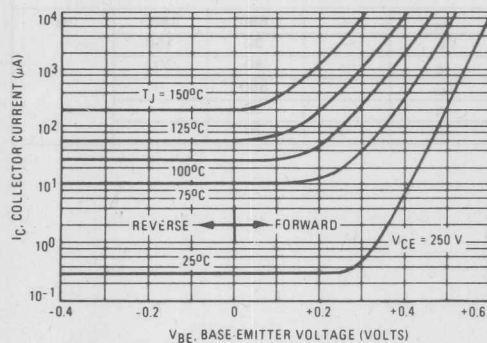
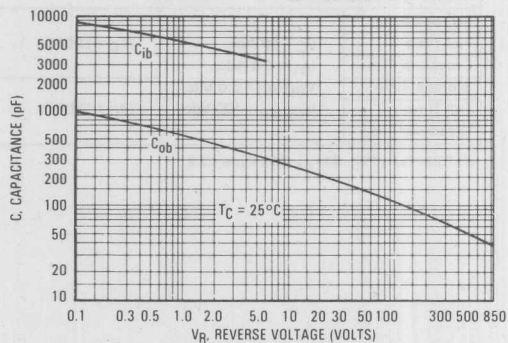


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

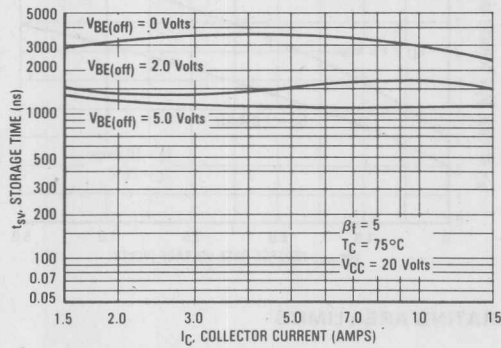


FIGURE 8 — STORAGE TIME

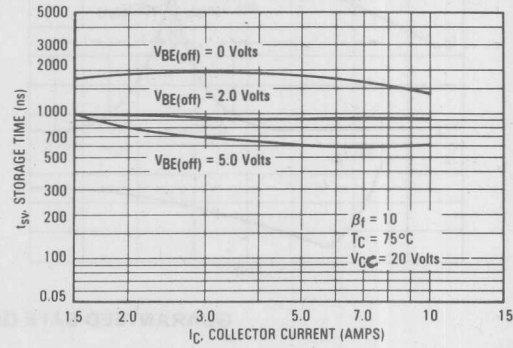


FIGURE 9 — COLLECTOR CURRENT FALL TIME

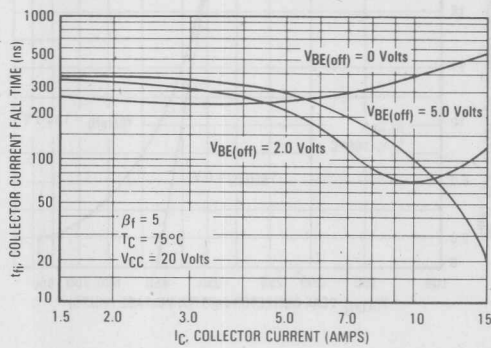


FIGURE 10 — COLLECTOR CURRENT FALL TIME

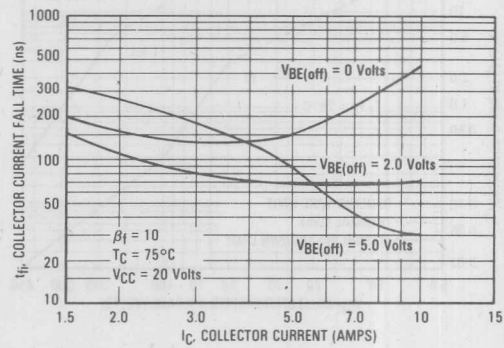


FIGURE 11 — CROSSOVER TIME

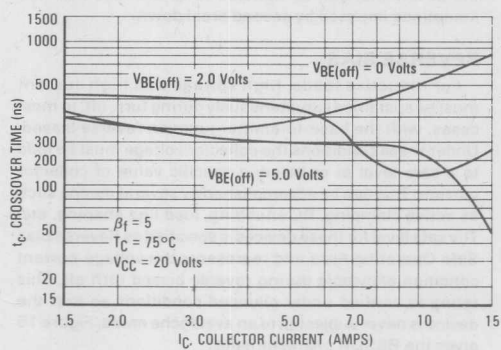


FIGURE 12 — CROSSOVER TIME

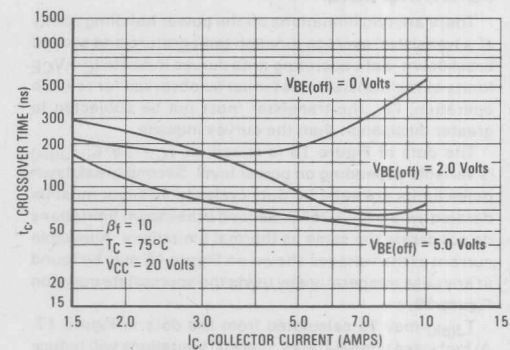


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

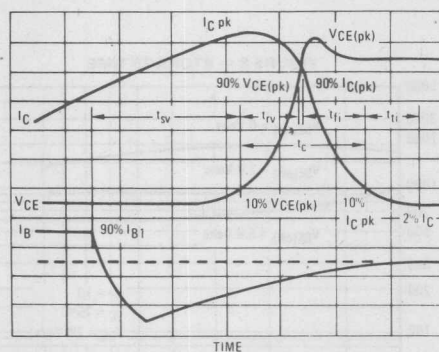
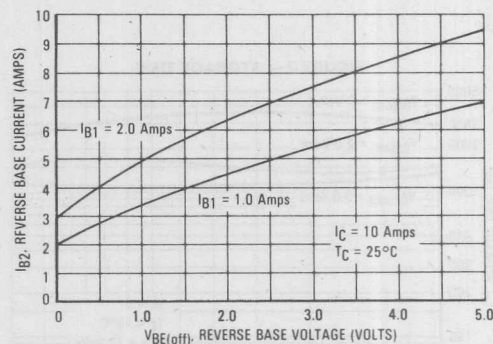
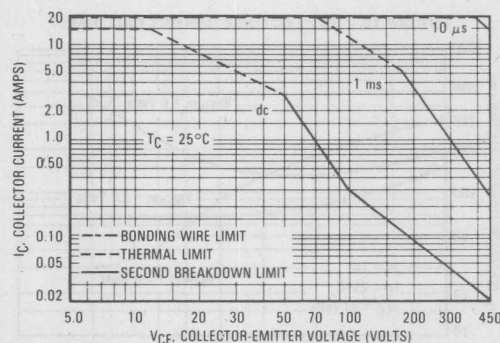
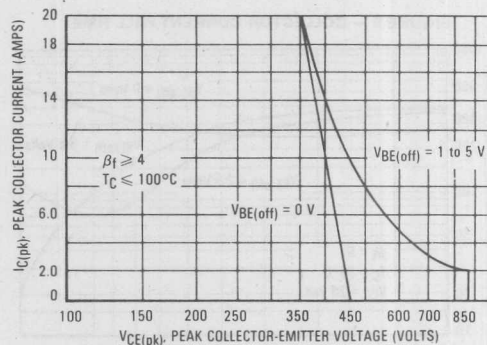


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS
SAFE OPERATING AREAFIGURE 16 — MAXIMUM REVERSE BIAS
SAFE OPERATING AREA

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce

the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

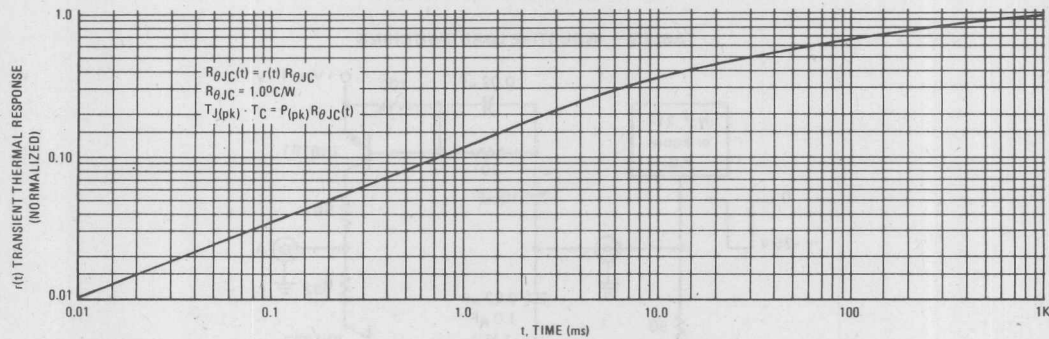


FIGURE 18 — POWER DERATING

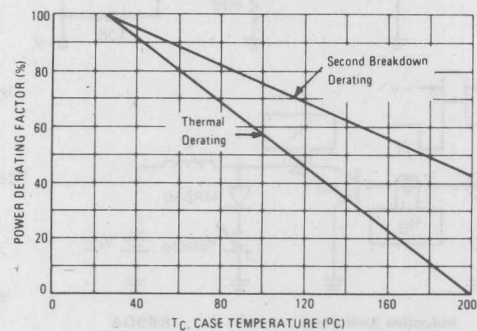
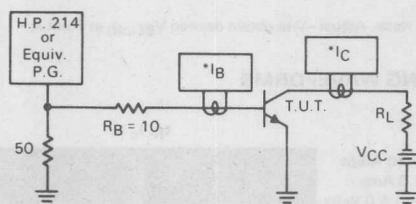
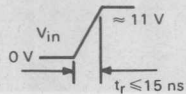


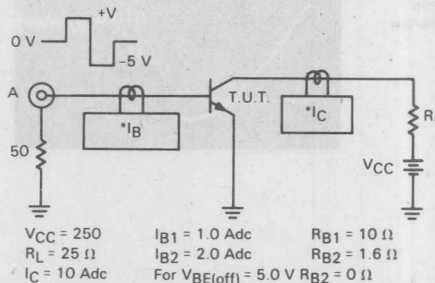
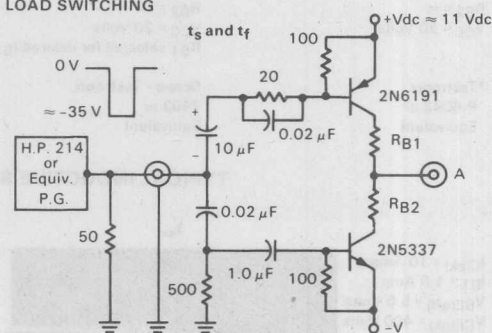
TABLE 1 — RESISTIVE LOAD SWITCHING

 t_d and t_r 

$V_{CC} = 250 \text{ Vdc}$
 $R_L = 25 \Omega$
 $I_C = 10 \text{ Adc}$
 $I_B = 1.0 \text{ Adc}$

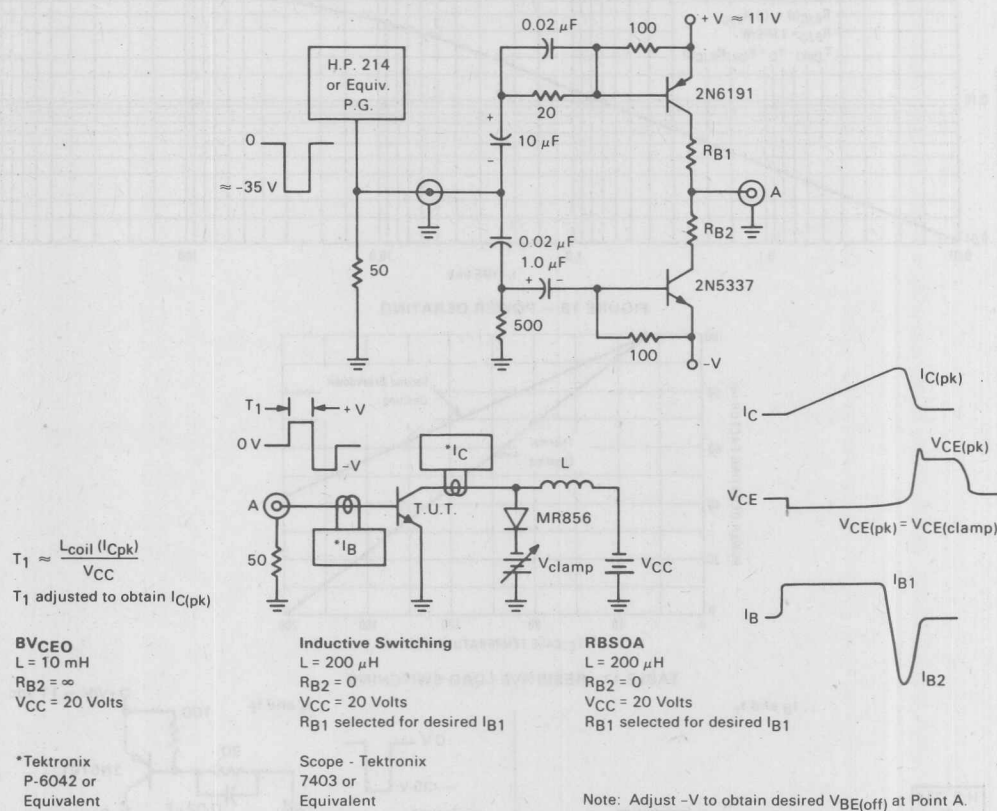


*Tektronix
 P-6042 or
 Equivalent

 t_s and t_f 

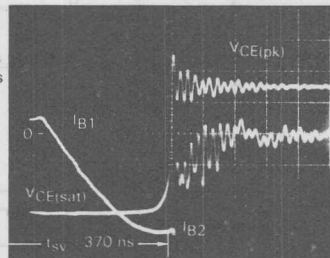
*Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING

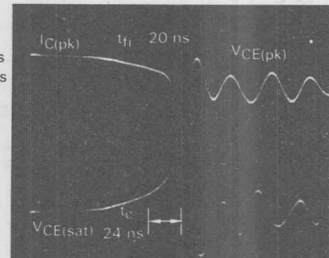


TYPICAL INDUCTIVE SWITCHING WAVEFORMS

$I_{C(pk)} = 10 \text{ Amps}$
 $I_{B1} = 1.0 \text{ Amp}$
 $V_{BE}(\text{off}) = 5.0 \text{ Volts}$
 $V_{CE(pk)} = 400 \text{ Volts}$
 $T_C = 25^\circ\text{C}$
 Time Base =
 100 ns/cm



$I_{C(pk)} = 10 \text{ Amps}$
 $I_{B1} = 1.0 \text{ Amp}$
 $V_{BE}(\text{off}) = 5.0 \text{ Volts}$
 $V_{CE(pk)} = 400 \text{ Volts}$
 $T_C = 25^\circ\text{C}$
 Time Base =
 20 ns/cm





MOTOROLA

NPN
MJE200

PNP
MJE210

COMPLEMENTARY SILICON POWER PLASTIC TRANSISTORS

... designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage —
 $V_{CE(sus)} = 25 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain — $h_{FE} = 70 \text{ (Min) @ } I_C = 500 \text{ mAdc}$
= 45 (Min) @ $I_C = 2.0 \text{ Adc}$
= 10 (Min) @ $I_C = 5.0 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$
= 0.75 Vdc (Max) @ $I_C = 2.0 \text{ Adc}$
- High Current-Gain — Bandwidth Product —
 $f_T = 65 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakage — $I_{CBO} = 100 \text{ nAdc @ Rated } V_{CB}$

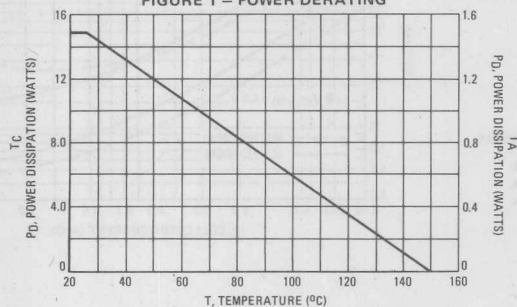
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	40	Vdc
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous Peak	I_C	5.0 10	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	15 0.12	Watts W/ $^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5 0.012	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

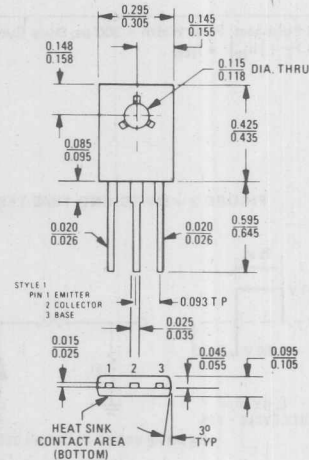
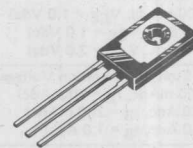
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	$^\circ\text{C/W}$

FIGURE 1 — POWER DERATING



5 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

25 VOLTS
15 WATTS



CASE 77-03

NPN • MJE200
PNP • MJE210

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 10 \text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	25	—	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$, $T_J = 125^\circ\text{C}$)	I_{CBO}	—	100 100	nAdc μAdc
Emitter Cutoff Current ($V_{BE} = 8.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (1) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$)	h_{FE}	70 45 10	— 180 —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 500 \text{ mAdc}$, $I_B = 50 \text{ mAdc}$) ($I_C = 2.0 \text{ Adc}$, $I_B = 200 \text{ mAdc}$) ($I_C = 5.0 \text{ Adc}$, $I_B = 1.0 \text{ Adc}$)	$V_{CE(sat)}$	— — —	0.3 0.75 1.8	Vdc
Base-Emitter Saturation Voltage (1) ($I_C = 5.0 \text{ Adc}$, $I_B = 1.0 \text{ Adc}$)	$V_{BE(sat)}$	—	2.5	Vdc
Base-Emitter On Voltage (1) ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (2) ($I_C = 100 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{\text{test}} = 10 \text{ MHz}$)	f_T	65	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	— —	80 120	pF

(1) Pulse test: Pulse Width = 300 μs , Duty Cycle $\approx 2.0\%$.

(2) $f_T = |h_{fe}| \cdot f_{\text{test}}$

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

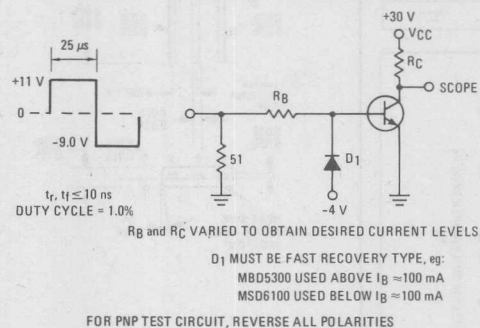


FIGURE 3 — TURN-ON TIME

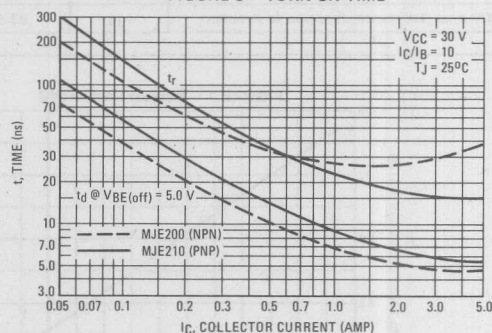


FIGURE 4 – THERMAL RESPONSE

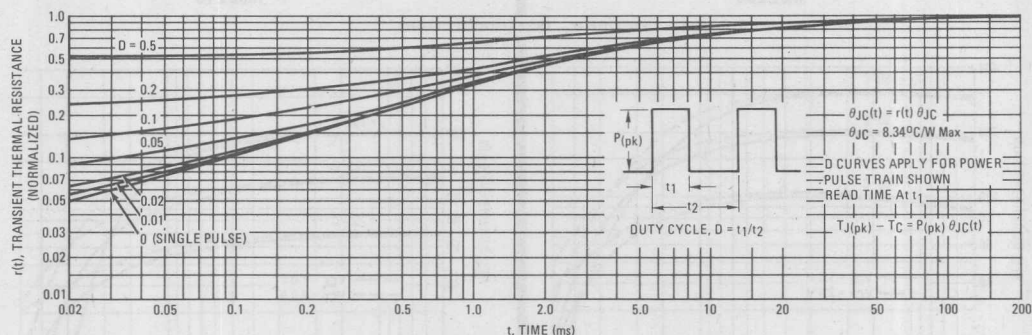
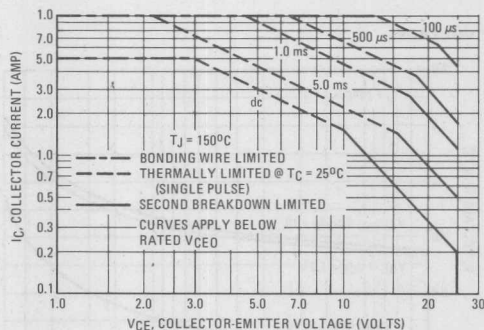


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

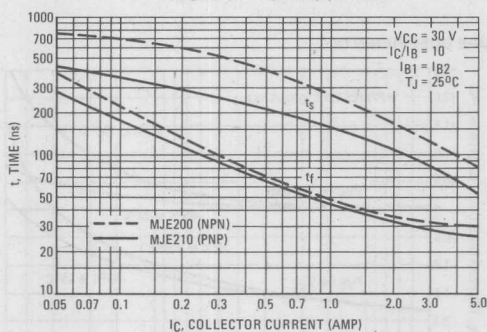
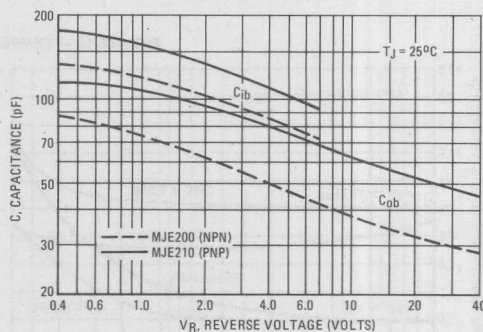


FIGURE 7 – CAPACITANCE



NPN • MJE200
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NPN
MJE200

PNP
MJE210

FIGURE 8 – DC CURRENT GAIN

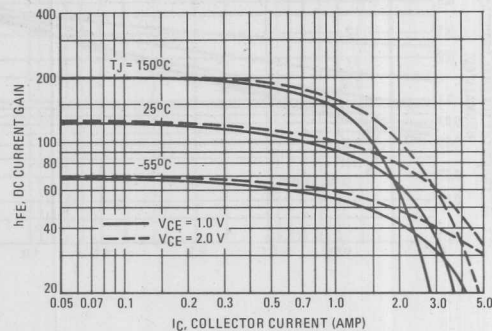
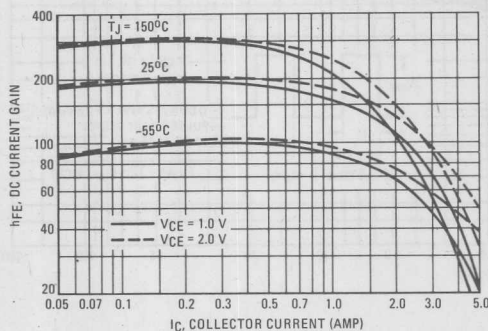


FIGURE 9 – "ON" VOLTAGE

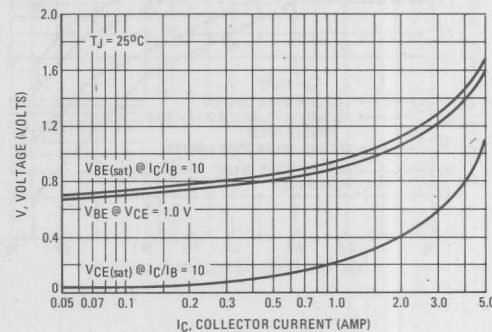
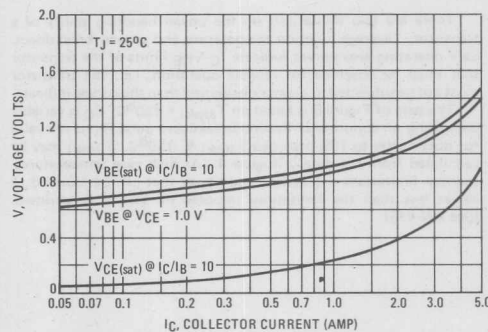
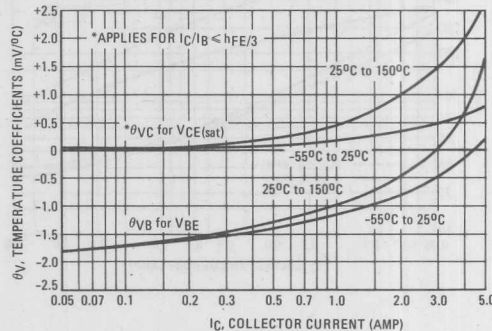
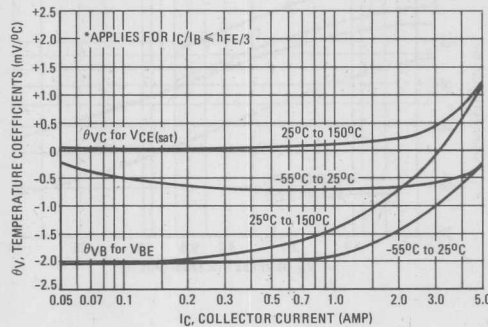


FIGURE 10 – TEMPERATURE COEFFICIENTS



COMPLEMENTARY SILICON POWER PLASTIC TRANSISTORS

... designed for low power audio amplifier and low-current, high-speed switching applications.

- High Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 80 \text{ Vdc (Min) – MJE240/2, MJE250/2}$
 $= 100 \text{ Vdc (Min) – MJE243/4, MJE253/4}$
- High DC Current Gain @ $I_C = 200 \text{ mAdc}$
 $h_{FE} = 40\text{--}200 \text{ – MJE240, MJE250}$
 $= 40\text{--}120 \text{ – MJE241, 243, MJE251, 253}$
 $= 25 \text{ (Min) – MJE242, 44, MJE252, 54}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$
- High Current Gain Bandwidth Product –
 $f_T = 40 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakages
 $I_{CBO} = 100 \text{ nAdc (Max) @ Rated } V_{CB}$

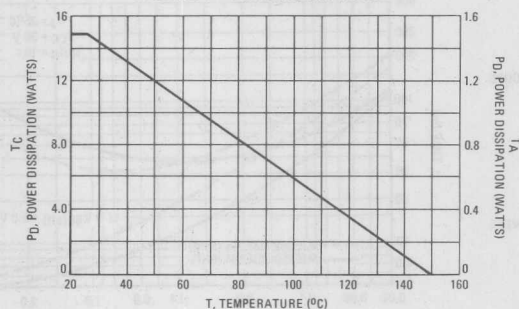
MAXIMUM RATINGS

Rating	Symbol	MJE240 MJE241 MJE242 MJE250 MJE251 MJE252	MJE243 MJE244 MJE253 MJE254	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}		7.0	Vdc
Collector Current – Continuous	I_C	4.0	8.0	Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	15 0.12		Watts W/ $^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5 0.012		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	$^\circ\text{C/W}$

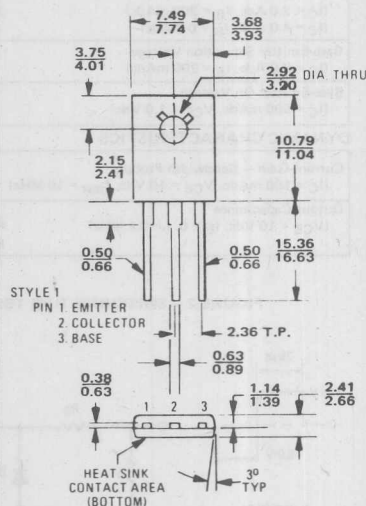
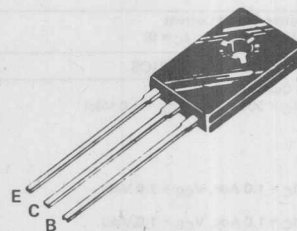
FIGURE 1 – POWER DERATING



4 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

80, 100 VOLTS
 15 WATTS



When mounting the device, torque not to exceed 0.07 m·kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
 All dimensions in millimeters

CASE 77-04

NPN • MJE240 thru MJE244
PNP • MJE250 thru MJE254

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ($I_C = 10\text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	80	—	Vdc
MJE240, MJE241, MJE242, MJE250, MJE251, MJE252 MJE243, MJE244 MJE253, MJE254		100	—	
Collector Cutoff Current ($V_{CB} = 80\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	0.1	μAdc
($V_{CB} = 100\text{ Vdc}$, $I_E = 0$)		—	0.1	
($V_{CE} = 80\text{ Vdc}$, $I_E = 0$, $T_C = 125^\circ\text{C}$)		—	0.1	mAdc
($V_{CE} = 100\text{ Vdc}$, $I_E = 0$, $T_C = 125^\circ\text{C}$)		—	0.1	
MJE240, MJE241, MJE242, MJE250, MJE251, MJE252, MJE243, MJE244 MJE253, MJE254				
Emitter Cutoff Current ($V_{BE} = 7.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 200\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	40	200	—
MJE240, MJE250 MJE241, MJE251, MJE243, MJE253 MJE242, MJE252, MJE244, MJE254		40	120	
($I_C = 1.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$)		25	—	
($I_C = 1.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$)		20	—	
($I_C = 2.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$)		10	—	
MJE240, MJE250 MJE241, MJE251, MJE243, MJE253 MJE242, MJE252 MJE244, MJE254 MJE240, MJE250		15	—	
Collector-Emitter Saturation Voltage ($I_C = 500\text{ mAdc}$, $I_B = 50\text{ mAdc}$)	$V_{CE(sat)}$	—	0.3	Vdc
($I_C = 1.0\text{ Adc}$, $I_B = 100\text{ mAdc}$)		—	0.6	
($I_C = 2.0\text{ Adc}$, $I_B = 200\text{ mAdc}$)		—	0.8	
($I_C = 4.0\text{ Adc}$, $I_B = 0.8\text{ Adc}$)		—	2.5	
All Types				
Base-Emitter Saturation Voltage ($I_C = 2.0\text{ Adc}$, $I_B = 200\text{ mAdc}$)	$V_{BE(sat)}$	—	1.8	Vdc
Base-Emitter On Voltage ($I_C = 500\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product ($I_C = 100\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 10\text{ MHz}$)	f_T	40	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	—	50	pF
MJE240/MJE244 MJE250/MJE254		—	70	

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

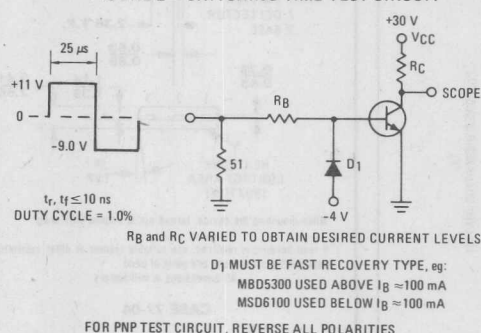


FIGURE 3 — TURN-ON TIME

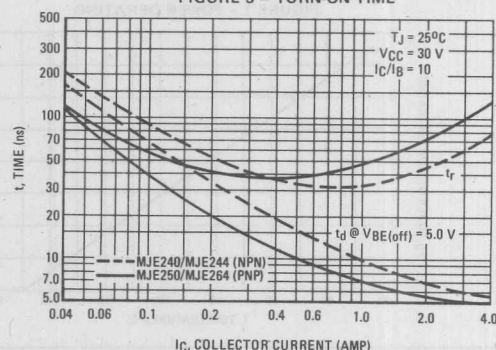


FIGURE 4 – THERMAL RESPONSE

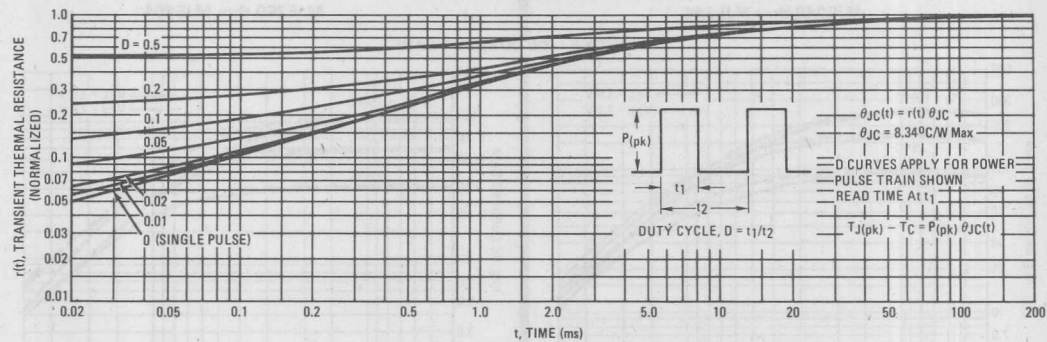
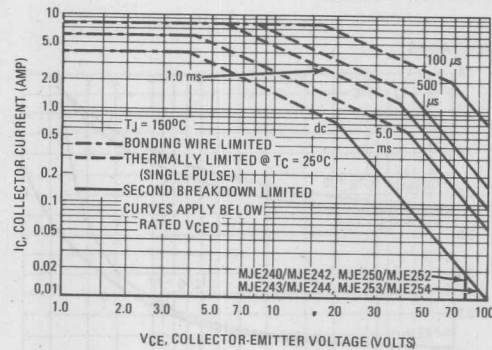


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_J(pk) = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(pk) \leq 150^\circ\text{C}$. $T_J(pk)$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

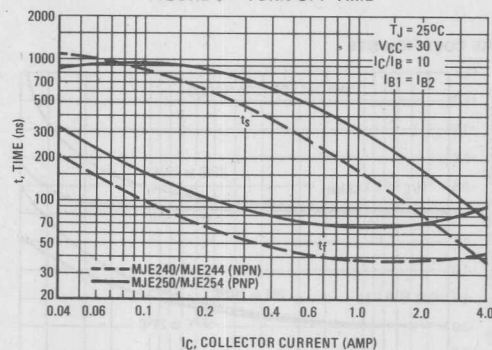
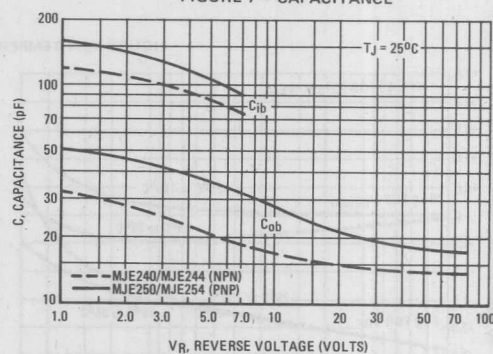


FIGURE 7 – CAPACITANCE



NPN • MJE240 thru MJE244
PNP • MJE250 thru MJE254

NPN
MJE240 thru MJE244

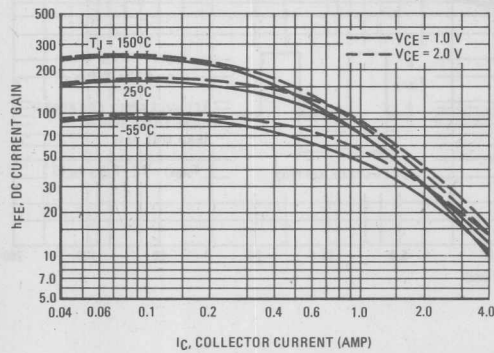


FIGURE 8 - DC CURRENT GAIN

PNP
MJE250 thru MJE254

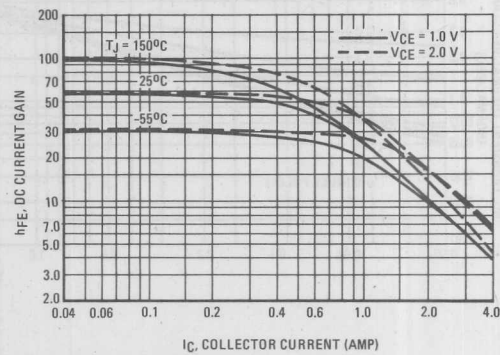


FIGURE 9 - "ON" VOLTAGES

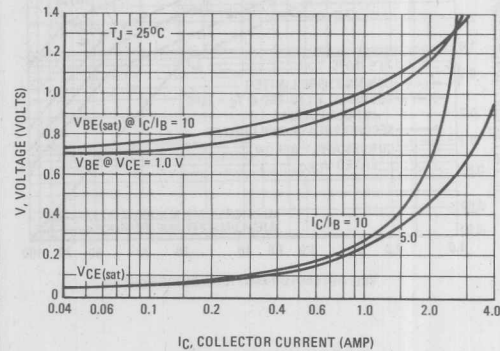
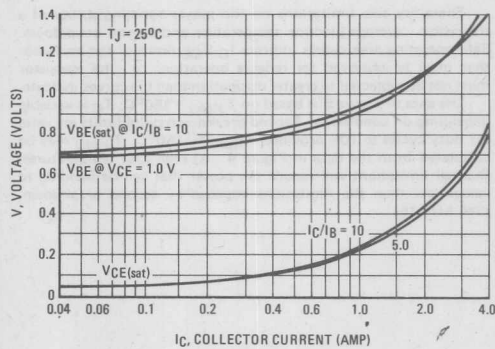
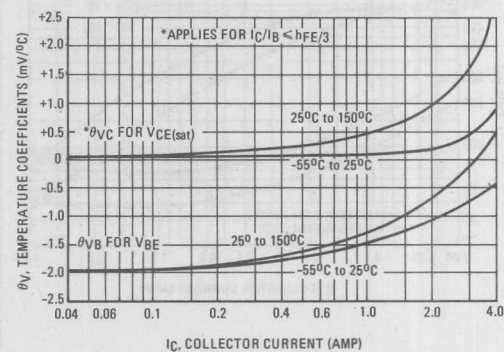
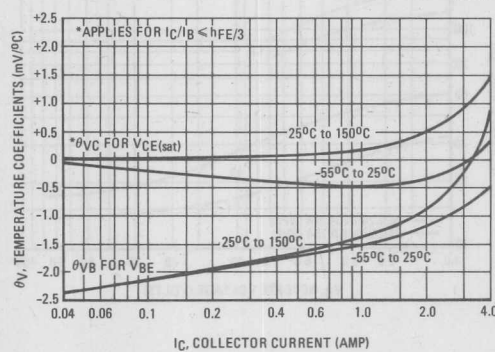


FIGURE 10 - TEMPERATURE COEFFICIENTS



**MOTOROLA****MJE340****PLASTIC MEDIUM POWER NPN
SILICON TRANSISTOR**

... designed for power output stages for television, radio, phonograph and other consumer product applications.

- Suitable for Transformerless, Line-Operated Equipment
- Thermopad Δ Construction Provides High Power Dissipation Rating for High Reliability

**0.5 AMPERE
POWER TRANSISTOR****NPN SILICON****300 VOLTS****MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CE0}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
MJE340			
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20.8 0.167	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	MJE340	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.0	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

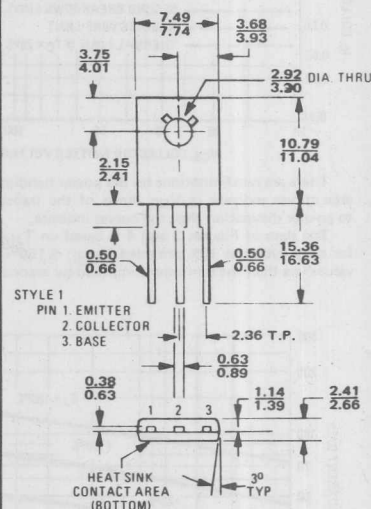
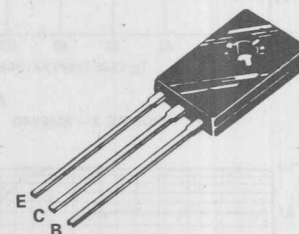
Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 1.0$ mAdc, $I_E = 0$)	$V_{CE0(sus)}$	300	—	Vdc
Collector Cutoff Current ($V_{CE} = 300$ Vdc, $I_E = 0$)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current ($V_{EB} = 3.0$ Vdc, $I_C = 0$)	I_{EBO}	—	100	μAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = 50$ mAdc, $V_{CE} = 10$ Vdc)	h_{FE}	30	240	—
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When mounting the device, torque not to exceed 0.07 m·kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-04

FIGURE 1 — POWER TEMPERATURE DERATING

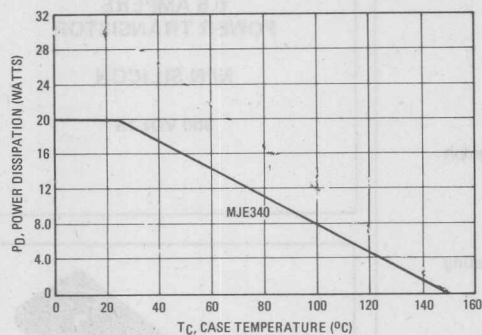
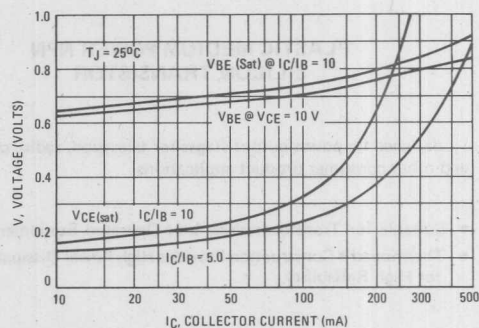
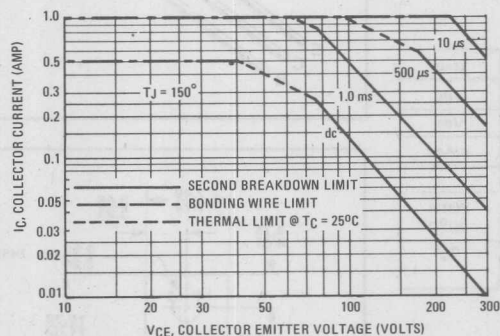


FIGURE 2 — "ON" VOLTAGES



ACTIVE-REGION SAFE OPERATING AREA

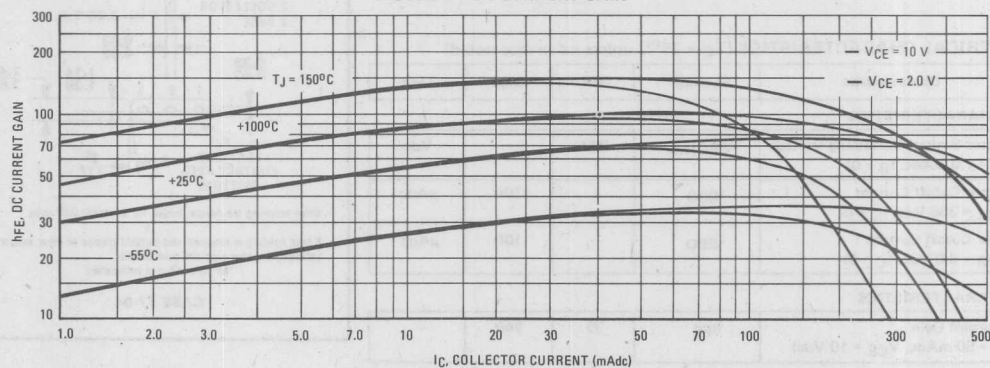
FIGURE 3 — MJE340



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)} = 150^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 5 — DC CURRENT GAIN





MOTOROLA

MJE5850 MJE5851 MJE5852

Designers Data Sheet

SWITCHMODE SERIES PNP SILICON POWER TRANSISTORS

The MJE5850, MJE5851 and the MJE5852 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

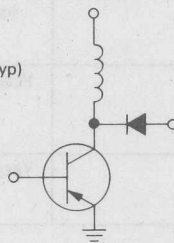
Fast Turn-Off Times

100 ns Inductive Fall Time @ 25°C (Typ)
125 ns Inductive Crossover Time @ 25°C (Typ)

Operating Temperature Range -65 to +150°C

100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



MAXIMUM RATINGS

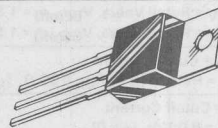
Rating	Symbol	MJE 5850	MJE 5851	MJE 5852	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	350	400	450	Vdc
Emitter Base Voltage	V_{EB}		6.0		Vdc
Collector Current — Continuous	I_C		8.0		Adc
Peak (1)	I_{CM}		16		
Base Current — Continuous	I_B		4.0		Adc
Peak (1)	I_{BM}		8.0		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D		80		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

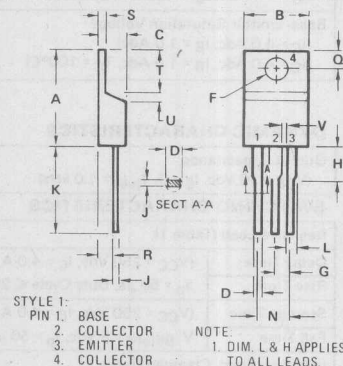
(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

8 AMPERE
PNP SILICON
POWER TRANSISTORS
300, 350, 400 VOLTS
80 WATTS



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 10\text{ mA}$, $I_B = 0$)	MJE5850 MJE5851 MJE5852 $V_{CEO(sus)}$	300 350 400	— — —	— — —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased Clamped Inductive SOA with base reverse biased	$I_{S/b}$ RBSOA	See Figure 12 See Figure 13			
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***ON CHARACTERISTICS**

DC Current Gain ($I_C = 2.0\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	15 5	— —	— —	—
Collector-Emitter Saturation Voltage ($I_C = 4.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 8.0\text{ Adc}$, $I_B = 3.0\text{ Adc}$) ($I_C = 4.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.0 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 4.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 4.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	270	—	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)					
Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 4.0\text{ A}$, $I_{B1} = 1.0\text{ A}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2\%$)	t_d	—	0.025	0.1 μs
Rise Time		t_r	—	0.100	0.5 μs
Storage Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 4.0\text{ A}$, $I_{B1} = 1.0\text{ A}$,	t_s	—	0.60	2.0 μs
Fall Time	$V_{BE(off)} = 5\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2\%$)	t_f	—	0.11	0.5 μs
Inductive Load, Clamped (Table 1)					
Storage Time	$(I_{CM} = 4\text{ A}$, $V_{CEM} = 250\text{ V}$, $I_{B1} = 1.0\text{ A}$,	t_{sv}	—	0.8	3.0 μs
Crossover Time	$V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_c	—	0.4	1.5 μs
Fall Time		t_{fi}	—	0.1	— μs
Storage Time	$(I_{CM} = 4\text{ A}$, $V_{CEM} = 250\text{ V}$, $I_{B1} = 1.0\text{ A}$,	t_{sv}	—	0.5	— μs
Crossover Time	$V_{BE(off)} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_c	—	0.125	— μs
Fall Time		t_{fi}	—	0.1	— μs

* Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

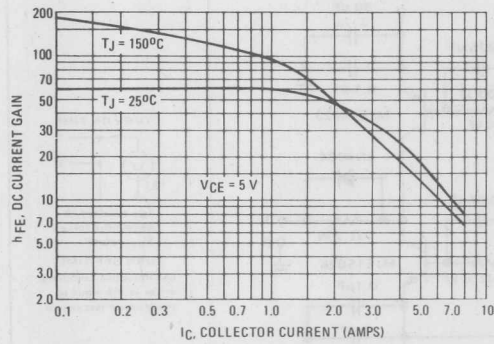


FIGURE 2 — COLLECTOR SATURATION REGION

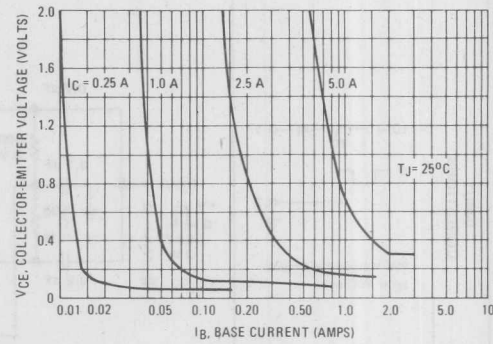


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

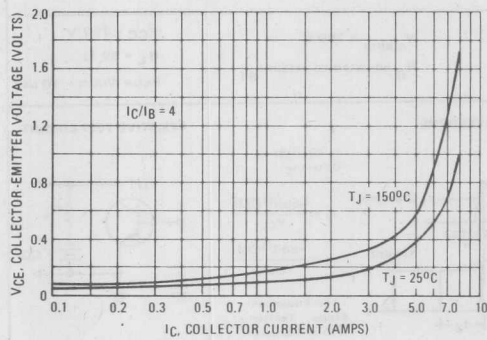


FIGURE 4 — BASE-EMITTER VOLTAGE

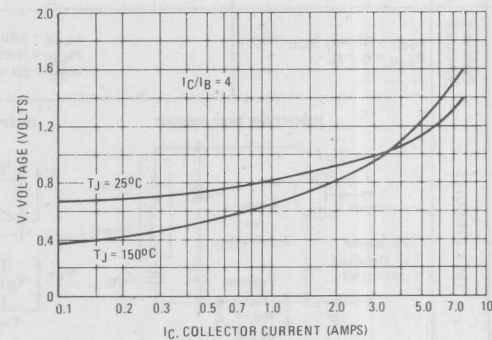


FIGURE 5 — COLLECTOR CUTOFF REGION

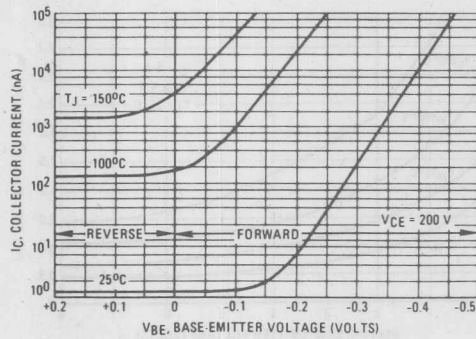


FIGURE 6 — CAPACITANCE

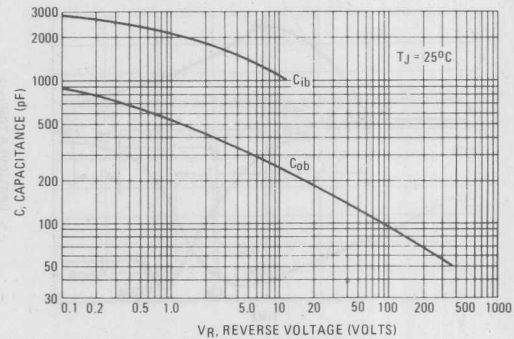


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

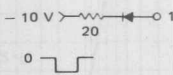
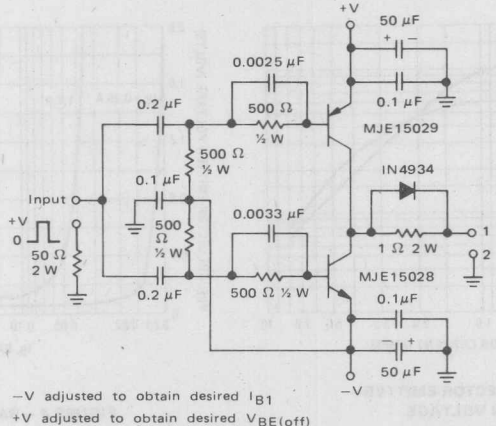
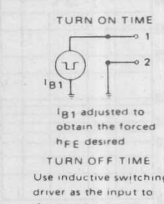
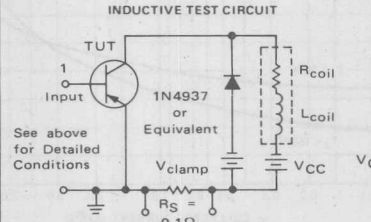
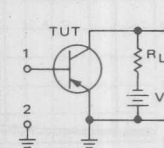
	$V_{CEO}(\text{sus})$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>	 <p>—V adjusted to obtain desired I_{B1} +V adjusted to obtain desired $V_{BE}(\text{off})$</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{\text{coil}} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{\text{coil}} = 0.7 \Omega$	$L_{\text{coil}} = 180 \mu\text{H}$ $R_{\text{coil}} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{\text{clamp}} = 250 \text{ V}$ R_B adjusted to attain I_{B1}	$V_{CC} = 250 \text{ V}$ $R_L = 62 \Omega$ Pulse Width = $10 \mu\text{s}$
TEST CIRCUITS	 <p>INDUCTIVE TEST CIRCUIT</p> <p>See above for Detailed Conditions</p> <p>1N4937 or Equivalent</p> <p>$R_S = 0.1 \Omega$</p> <p>OUTPUT WAVEFORMS</p> <p>I_C vs Time: I_{CM}, t_f Clamped, t_1, t_2</p> <p>V_{CE} vs Time: V_{CEM}, V_{clamp}, t_1, t_2</p> <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 = \frac{L_{\text{coil}}(I_{CM})}{V_{CC}}$</p> <p>$t_2 = \frac{L_{\text{coil}}(I_{CM})}{V_{\text{clamp}}}$</p> <p>Test Equipment Scope Tektronix 475 or Equivalent</p>	 <p>RESISTIVE TEST CIRCUIT</p>	

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

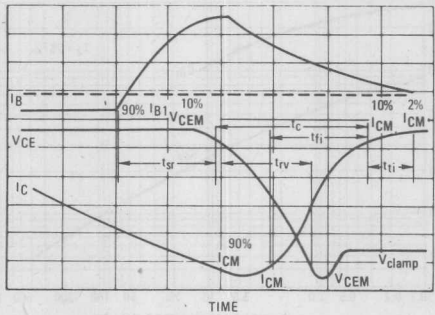
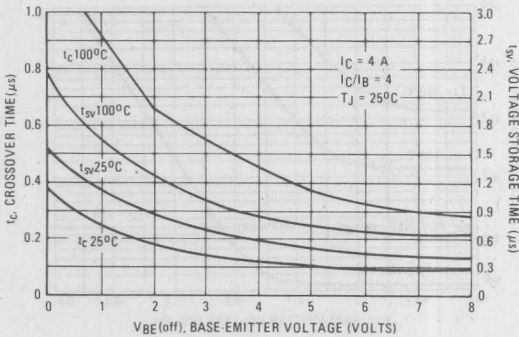


FIGURE 8 — INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{rv} = Voltage Rise Time, 10–90% V_{CEM}

t_{fi} = Current Fall Time, 90–10% I_{CM}

t_{ti} = Current Tail, 10–2% I_{CM}

t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform

is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C t_c / f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 9 – TURN-ON SWITCHING TIMES

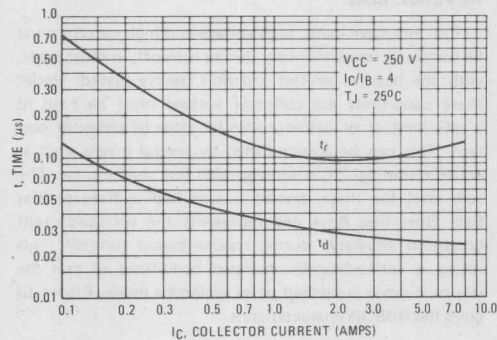
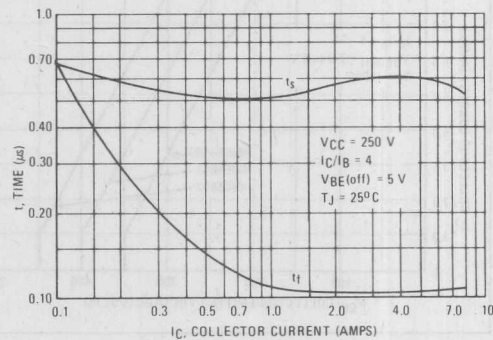
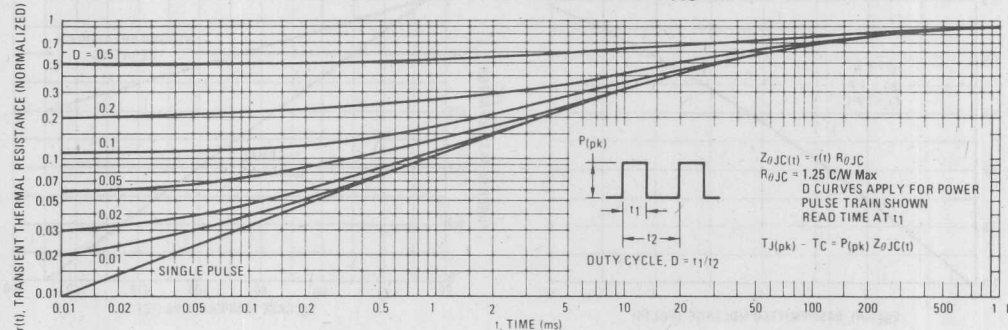


FIGURE 10 – TURN-OFF SWITCHING TIMES

FIGURE 11 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

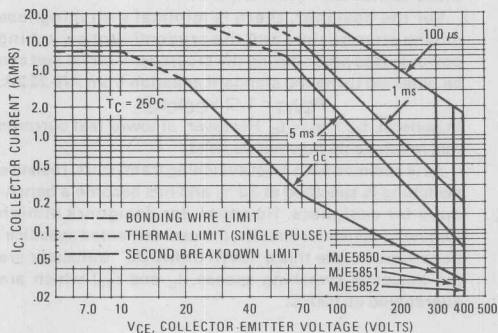


FIGURE 13 — RBSOA, MAXIMUM REVERSE BIAS SAFE OPERATING AREA

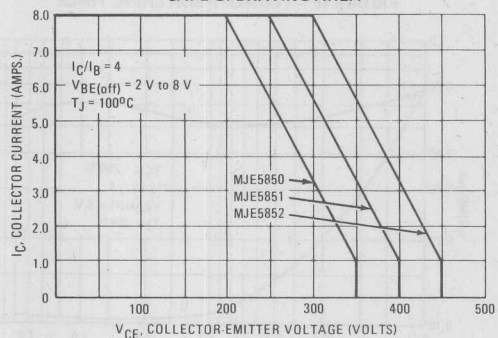
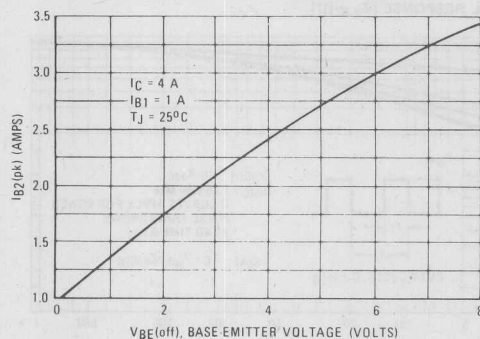


FIGURE 14 PEAK REVERSE BASE CURRENT



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

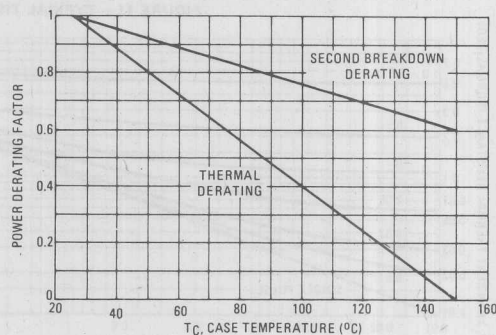
The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

FIGURE 15 — FORWARD BIAS POWER DERATING



**MOTOROLA****MJE13002 • MJ4360
MJE13003 • MJ4361****Designers' Data Sheet****SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTORS**

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- Reverse Biased SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100 $^\circ\text{C}$... t_c @ 1 A, 100 $^\circ\text{C}$ is 290 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

MAXIMUM RATINGS

Rating	Symbol	MJE13002	MJE13003	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous	I_C	1.5		Adc
— Peak (1)	I_{CM}	3		Adc
Base Current — Continuous	I_B	0.75		Adc
— Peak (1)	I_{BM}	1.5		Adc
Emitter Current — Continuous	I_E	2.25		Adc
— Peak (1)	I_{EM}	4.5		Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.4		Watts
Derate above 25 $^\circ\text{C}$		11.2		mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	40		Watts
Derate above 25 $^\circ\text{C}$		320		mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

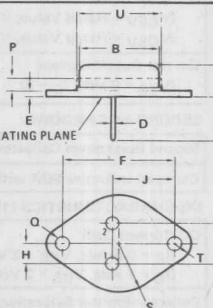
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	89	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.**Designer's Data for "Worst Case" Conditions**

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

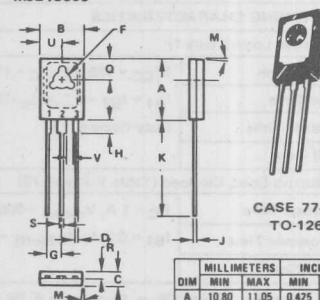
**1.5 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
40 WATTS****MJ4360
MJ4361****CASE 80-02
TO-66**

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC
Dimensions and
Notes Apply.

**MJE13002
MJE13003****CASE 77-03
TO-126**

STYLE 3
PIN 1. BASE
2. COLLECTOR
3. EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.19	0.115	0.125
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	36 TYP	—	36 TYP	—
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	—	0.040	—

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage ($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	300 400	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	— —	— —	1 5	mAdc
Emitter Cutoff Current ($V_{EB} = 9\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 12			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$) ($I_C = 1\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$)	h_{FE}	8 5	— —	40 25	—
Collector-Emitter Saturation Voltage ($I_C = 0.5\text{ Adc}$, $I_B = 0.1\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$) ($I_C = 1.5\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — — —	— — — —	0.5 1 3 1	Vdc
Base-Emitter Saturation Voltage ($I_C = 0.5\text{ Adc}$, $I_B = 0.1\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— — —	— — —	1 1.2 1.1	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product ($I_C = 100\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ MHz}$)	f_T	4	10	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	—	21	—	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 125\text{ Vdc}, I_C = 1\text{ A},$ $I_{B1} = I_{B2} = 0.2\text{ A}, t_p = 25\text{ }\mu\text{s},$ Duty Cycle $\leq 1\%$)	t_d	—	0.05	0.1	μs
Rise Time		t_r	—	0.5	1	μs
Storage Time		t_s	—	2	4	μs
Fall Time		t_f	—	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Storage Time	$(I_C = 1\text{ A}, V_{\text{clamp}} = 300\text{ Vdc},$ $I_{B1} = 0.2\text{ A}, V_{BE(\text{off})} = 5\text{ Vdc}, T_C = 100^{\circ}\text{C})$	t_{SV}	—	1.7	4	μs
Crossover Time		t_C	—	0.29	0.75	μs
Fall Time		t_{fi}	—	0.15	—	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 1 — DC CURRENT GAIN

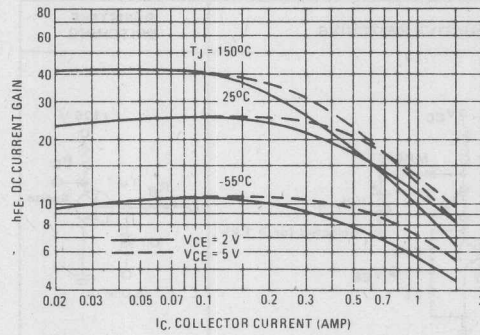


FIGURE 2 — COLLECTOR SATURATION REGION

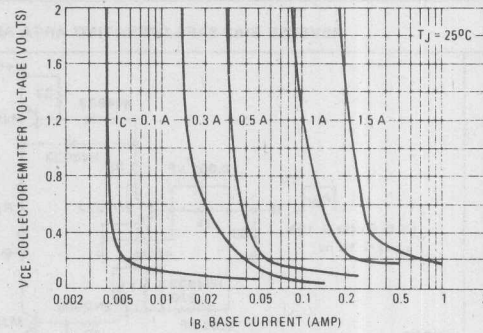


FIGURE 3 — BASE-EMITTER VOLTAGE

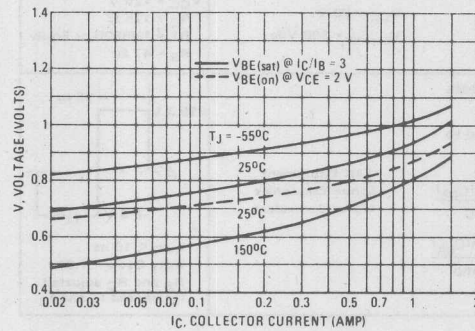


FIGURE 4 — COLLECTOR-EMITTER SATURATION REGION

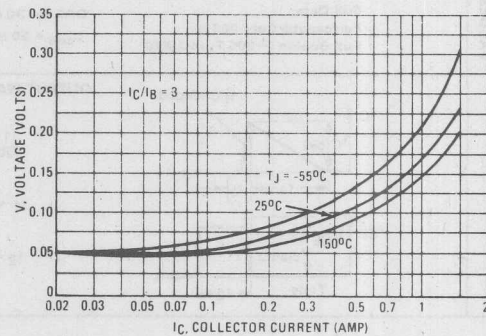


FIGURE 5 — COLLECTOR CUTOFF REGION

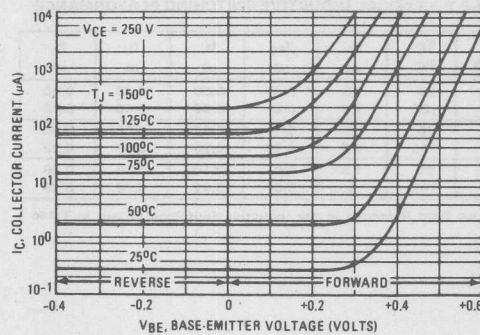


FIGURE 6 — CAPACITANCE

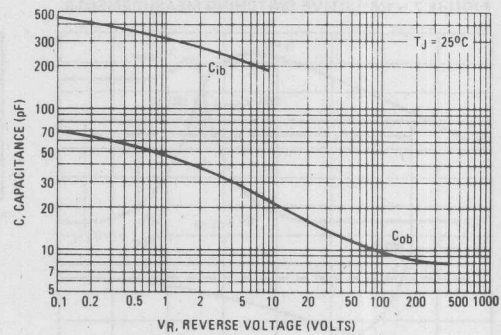


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING			RESISTIVE SWITCHING
TEST CIRCUITS	<p>Duty Cycle $\leq 10\%$ $t_r, t_f < 10 \text{ ns}$</p> <p>NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}</p>			<p>*Selected for $> 1 \text{ kV}$</p>
CIRCUIT VALUES	<p>Coil Data: Ferroxcube Core #6656 Full Bobbin (~200 Turns) #20</p> <p>GAP for 30 mH/2A L_{coil} = 50 mH</p> <p>V_{CC} = 20 V V_{clamp} = 300 Vdc</p>			<p>V_{CC} = 125 V R_C = 125 Ω D1 = 1N5820 or Equivalent R_B = 47 Ω</p>
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{\text{coil}} (I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{\text{coil}} (I_{Cpk})}{V_{\text{clamp}}}$ <p>Test Equipment Scope-Tektronics 475 or Equivalent</p>			<p>t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C</p>

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

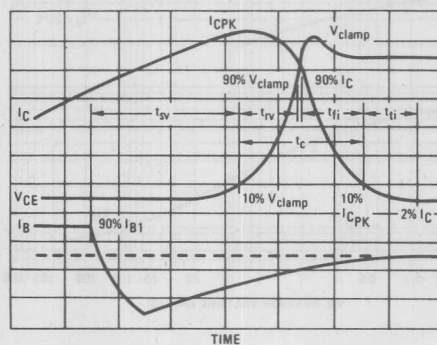


TABLE 2 - TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I _C AMP	T _C °C	t _{sv} μs	t _{rv} μs	t _{fi} μs	t _{fi} μs	t _c μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rV} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fI} = Current Fall Time, 90–10% I_C
- t_{tI} = Current Tail, 10–2% I_C
- t_C = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_C) f$$

In general, $t_{rV} + t_{fI} \approx t_C$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_C and t_{SV}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

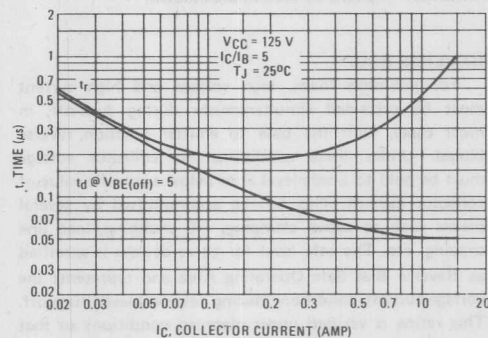


FIGURE 9 – TURN-OFF TIME

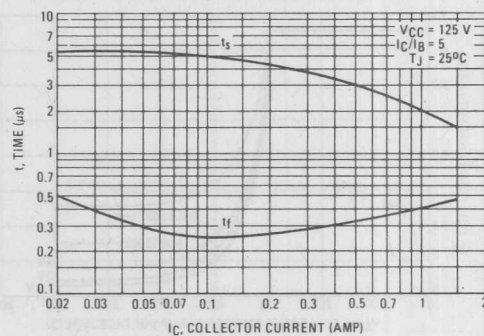
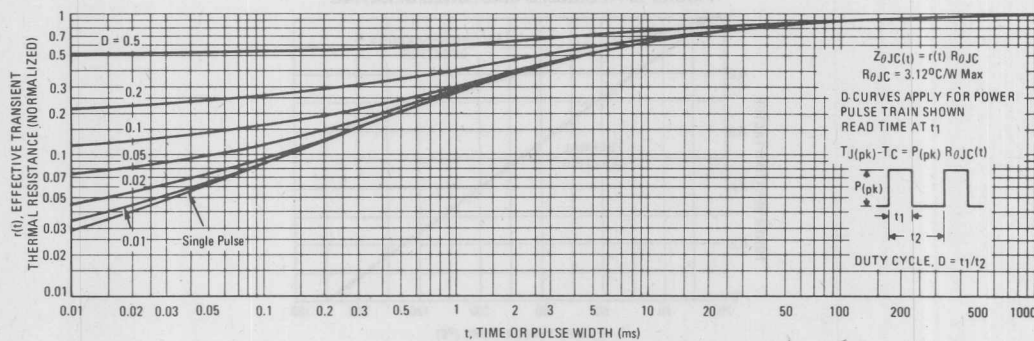


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATION AREA

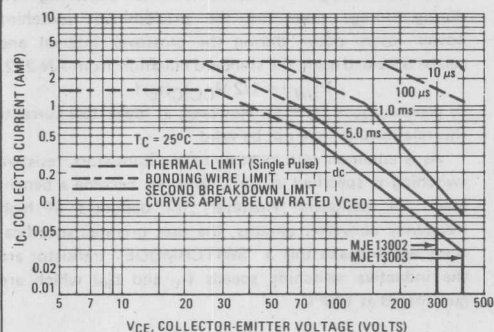


FIGURE 12 — REVERSE BIAS SAFE OPERATING AREA

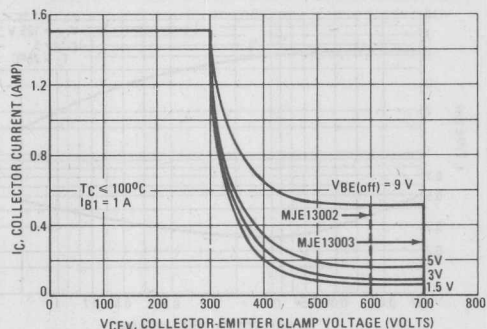
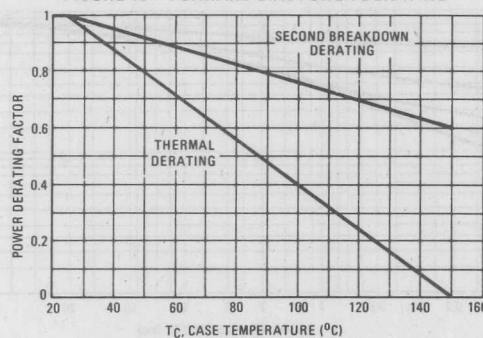


FIGURE 13 — FORWARD BIAS POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.


MOTOROLA
MJE13004 • MJ4380
MJE13005 • MJ4381

Designers' Data Sheet

SWITCHMODE[▲] SERIES NPN SILICON POWER TRANSISTORS

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulator's, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 2 to 4 Amp, 25 and 100°C
... t_c @ 3A, 100°C is 180 ns (Typ)
- 700-V Blocking Capability
- SOA and Switching Applications Information.

MAXIMUM RATINGS

Rating	Symbol	MJE13004 MJ4380	MJE13005 MJ4381	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous	I_C	4		Adc
— Peak (1)	I_{CM}	8		
Base Current — Continuous	I_B	2		Adc
— Peak (1)	I_{BM}	4		
Emitter Current — Continuous	I_E	6		Adc
— Peak (1)	I_{EM}	12		
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2		Watts
		16		mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75		Watts
		600		mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

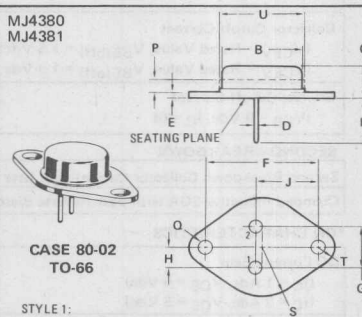
Designer's Data for "Worst Case" Conditions

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

4 AMPERE NPN SILICON POWER TRANSISTORS

300 and 400 VOLTS
75 WATTS

MJ4380
MJ4381

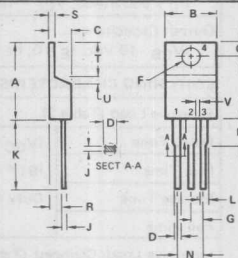


CASE 80-02
TO-66

STYLE 1:
PIN 1: BASE
2: EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

MJE13004
MJE13005



CASE 221A-02
TO-220AB

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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***OFF CHARACTERISTICS**

Collector-Emitter Sustaining Voltage ($I_C = 10\text{ mA}$, $I_B = 0$)	MJ4380, MJE13004 MJ4381, MJE13005	$V_{CEO(sus)}$	300 400	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)		I_{CEV}	— —	— —	1 5	mAdc
Emitter Cutoff Current ($V_{EB} = 9\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	—	1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 11
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 12

***ON CHARACTERISTICS**

DC Current Gain ($I_C = 1\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 2\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	10 8	— —	60 40	—
Collector-Emitter Saturation Voltage ($I_C = 1\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 4\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — — —	— — — —	0.5 0.6 1 1	Vdc
Base-Emitter Saturation Voltage ($I_C = 1\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— — —	— — —	1.2 1.6 1.5	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product ($I_C = 500\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ MHz}$)	f_T	4	—	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	—	65	—	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 2)						
Delay Time	(V _{CC} = 125 Vdc, I _C = 2 A, I _{B1} = I _{B2} = 0.4 A, t _p = 25 μs, Duty Cycle ≤ 1%)	t _d	—	0.025	0.1	μs
Rise Time		t _r	—	0.3	0.7	μs
Storage Time		t _s	—	1.7	4	μs
Fall Time		t _f	—	0.4	0.9	μs
Inductive Load, Clamped (Table 2, Figure 13)						
Voltage Storage Time	(I _C = 2 A, V _{clamp} = 300 Vdc, I _{B1} = 0.4 A, V _{BE(off)} = 5 Vdc, T _C = 100°C)	t _{sv}	—	0.9	4	μs
Crossover Time		t _c	—	0.32	0.9	μs
Fall Time		t _{fi}	—	0.16	—	μs

*Pulse Test: Pulse Width = $300\text{ }\mu\text{s}$, Duty Cycle = 2%.

FIGURE 1 — DC CURRENT GAIN

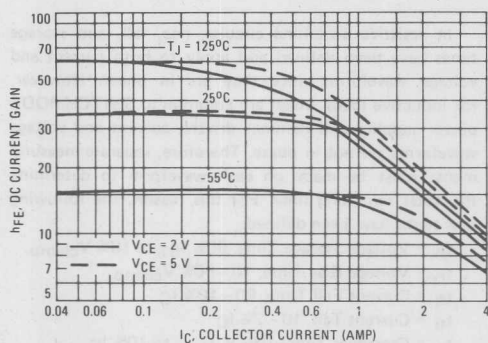


FIGURE 2 — COLLECTOR SATURATION REGION

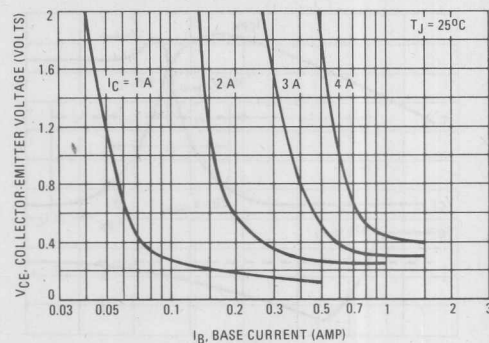


FIGURE 3 — BASE-EMITTER VOLTAGE

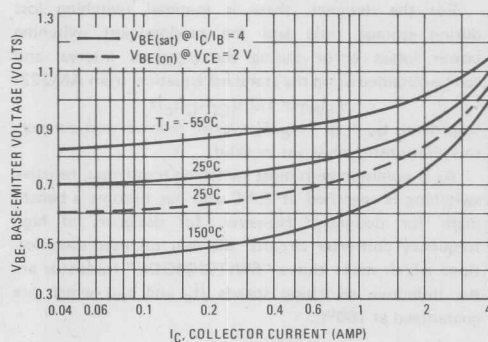


FIGURE 4 — COLLECTOR-EMITTER SATURATION VOLTAGE

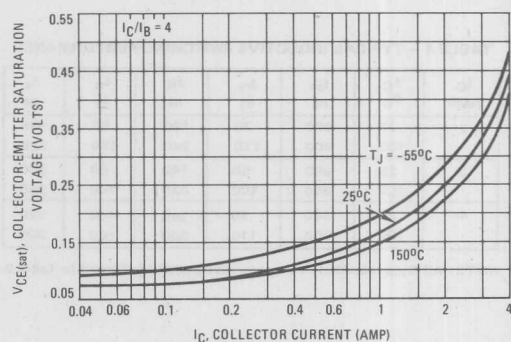


FIGURE 5 — COLLECTOR CUTOFF REGION

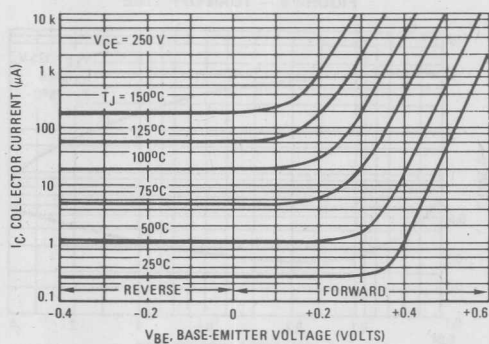


FIGURE 6 — CAPACITANCE

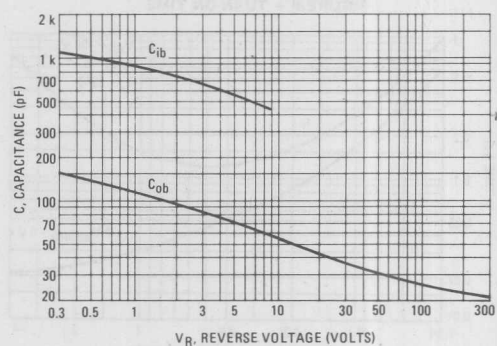


FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

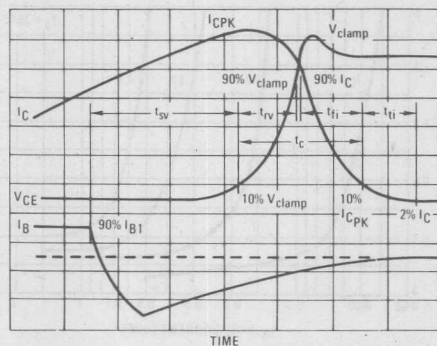


TABLE 1 — TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
2	25	600	70	100	80	180
	100	900	110	240	130	320
3	25	650	60	140	60	200
	100	950	100	330	100	350
4	25	550	70	160	100	220
	100	850	110	350	160	390

NOTE: All Data recorded in the inductive Switching Circuit in Table 2.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

 t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
 t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
 t_{fi} = Current Fall Time, 90–10% I_C
 t_{ti} = Current Tail, 10–2% I_C
 t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

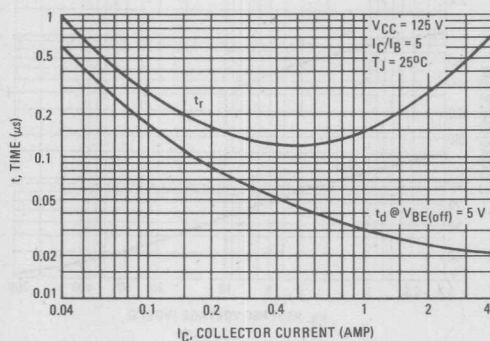


FIGURE 9 — TURN-OFF TIME

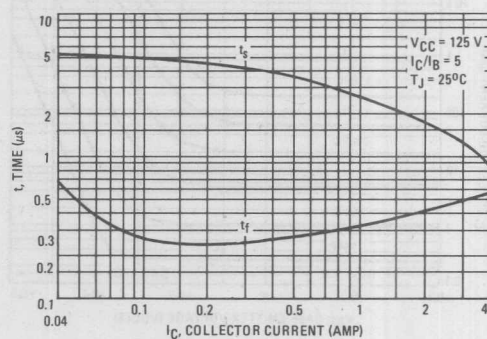


TABLE 2 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

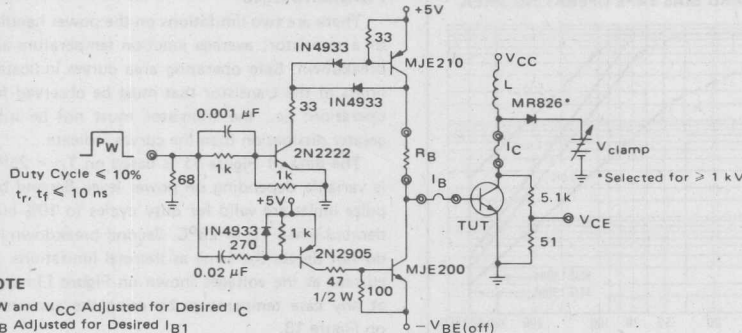
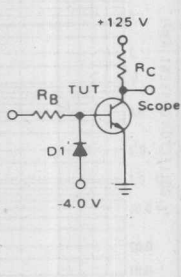
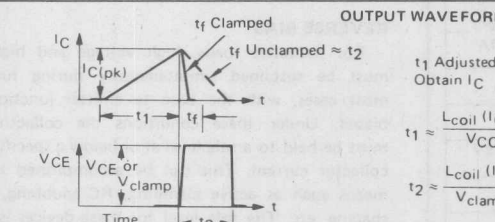
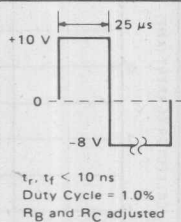
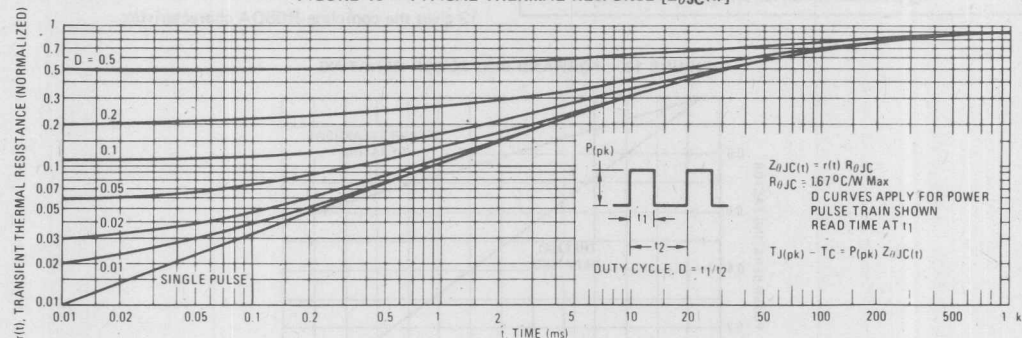
TEST CIRCUITS	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
	 <p>NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}</p>	
CIRCUIT VALUES	<p>Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16</p> <p>GAP for 200 μH/20A $L_{coil} = 200 \mu$H</p> <p>$V_{CC} = 20$ V $V_{clamp} = 300$ Vdc</p>	<p>$V_{CC} = 125$ V $R_C = 62 \Omega$ D1 = 1N5820 or Equiv $R_B = 22 \Omega$</p>
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> $t_1 = \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 = \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	 <p>$t_r, t_f < 10$ ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C</p>

FIGURE 10 — TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]



The Safe Operating Area Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATING AREA

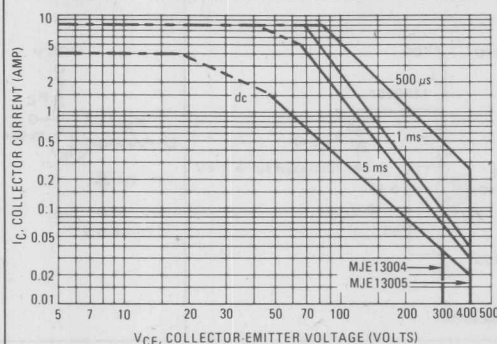
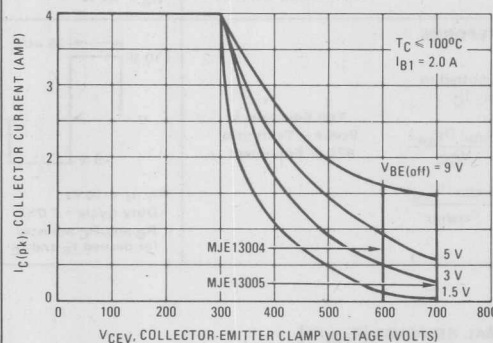


FIGURE 12 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

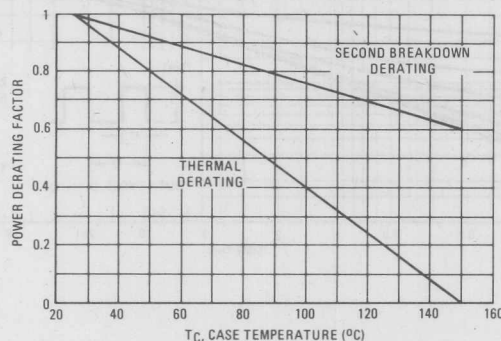
The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

FIGURE 13 — FORWARD BIAS POWER DERATING



**MOTOROLA****MJE13006****MJE13007****Designers' Data Sheet****SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTORS**

The MJE13006 and MJE13007 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 3 to 8 Amp, 25 and 100°C
... t_c @ 5A, 100°C is 136 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

MAXIMUM RATINGS

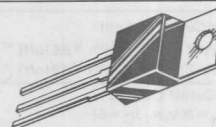
Rating	Symbol	MJE13006	MJE13007	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous	I_C	8		Adc
— Peak (1)	I_{CM}	16		
Base Current — Continuous	I_B	4		Adc
— Peak (1)	I_{BM}	8		
Emitter Current — Continuous	I_E	12		Adc
— Peak (1)	I_{EM}	24		
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2	16	Watts mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	80	640	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

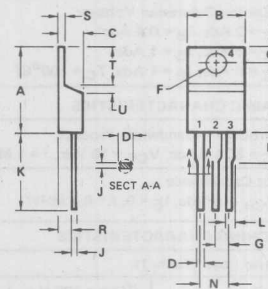
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

**8 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
80 WATTS**

**Designer's Data for
"Worst Case" Conditions**

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:

1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

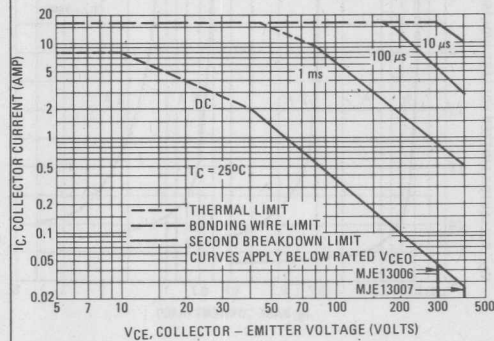
CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I _C = 10 mA, I _B = 0)	MJE13006 MJE13007 V _{CEO(sus)}	300 400	— —	— —	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	— —	— —	1 5	mAdc
Emitter Cutoff Current (V _{EB} = 9 Vdc, I _C = 0)	I _{EBO}	—	—	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	I _{S/b}	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased	—	See Figure 2			
*ON CHARACTERISTICS					
DC Current Gain (I _C = 2 Adc, V _{CE} = 5 Vdc) (I _C = 5 Adc, V _{CE} = 5 Vdc)	h _{FE}	8 6	— —	40 30	—
Collector-Emitter Saturation Voltage (I _C = 2 Adc, I _B = 0.4 Adc) (I _C = 5 Adc, I _B = 1 Adc) (I _C = 8 Adc, I _B = 2 Adc) (I _C = 5 Adc, I _B = 1 Adc, T _C = 100°C)	V _{CE(sat)}	— — — —	— — — —	1 1.5 3 2	Vdc
Base-Emitter Saturation Voltage (I _C = 2 Adc, I _B = 0.4 Adc) (I _C = 5 Adc, I _B = 1 Adc) (I _C = 5 Adc, I _B = 1 Adc, T _C = 100°C)	V _{BE(sat)}	— — —	— — —	1.2 1.6 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I _C = 500 mA, V _{CE} = 10 Vdc, f = 1 MHz)	f _T	4	—	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	—	110	—	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	V _{CC} = 125 Vdc, I _C = 5 A, I _{B1} = I _{B2} = 1 A, t _p = 25 μs, Duty Cycle ≤ 1%	t _d	—	0.05	0.1 μs
Rise Time		t _r	—	0.5	1 μs
Storage Time		t _s	—	1	3 μs
Fall Time		t _f	—	0.15	0.7 μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time	I _C = 5 A, V _{clamp} = 300 Vdc,	t _{sv}	—	0.86	2.3 μs
Crossover Time	I _{B1} = 1 A, V _{BE(off)} = 5 Vdc, T _C = 100°C)	t _c	—	0.14	0.7 μs

*Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 2 — REVERSE BIAS SWITCHING SAFE OPERATING AREA

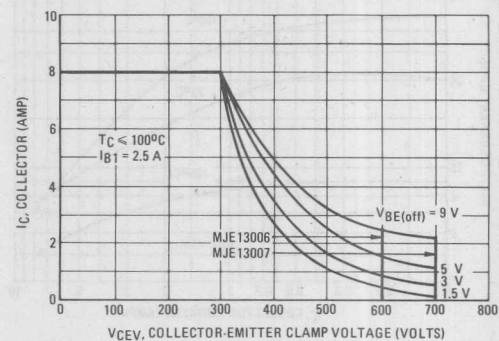
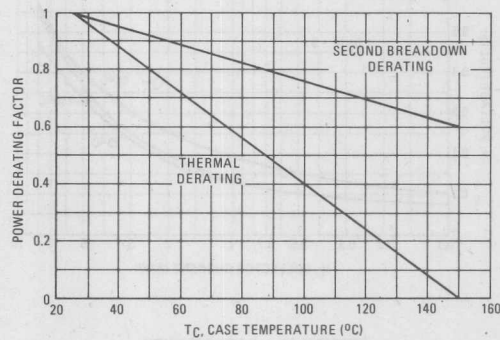


FIGURE 3 — FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_J(\text{pk})$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 — TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

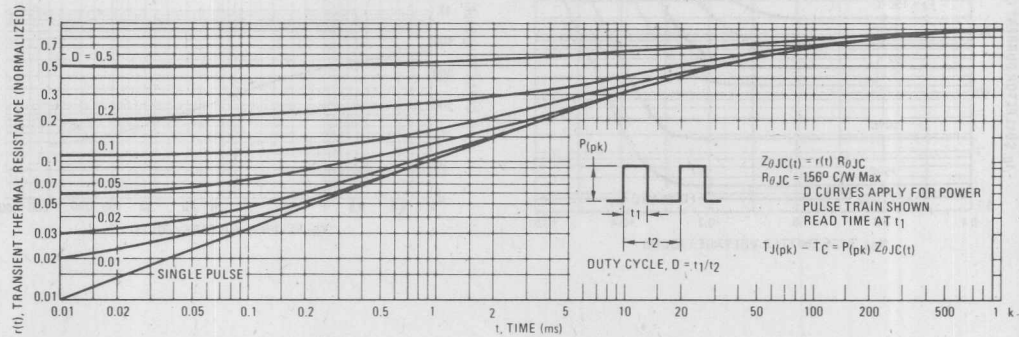


FIGURE 5 — DC CURRENT GAIN

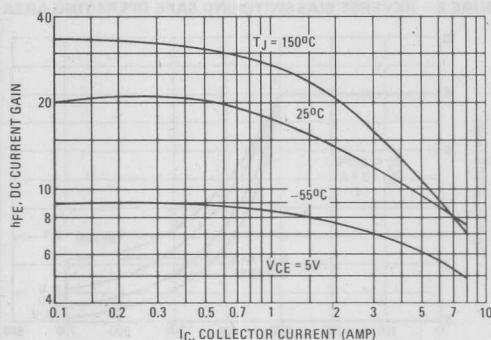


FIGURE 6 — COLLECTOR SATURATION REGION

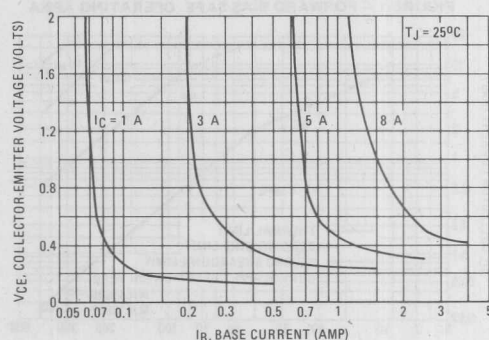


FIGURE 7 — BASE-EMITTER SATURATION VOLTAGE

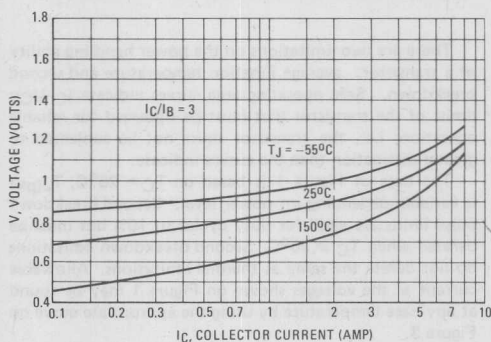


FIGURE 8 — COLLECTOR-EMITTER SATURATION VOLTAGE

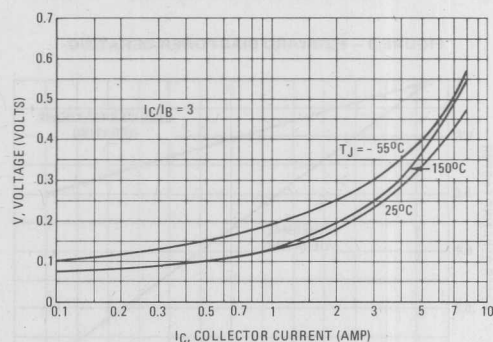


FIGURE 9 — COLLECTOR CUTOFF REGION

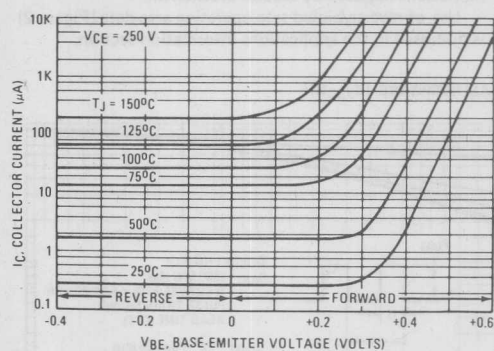


FIGURE 10 — CAPACITANCE

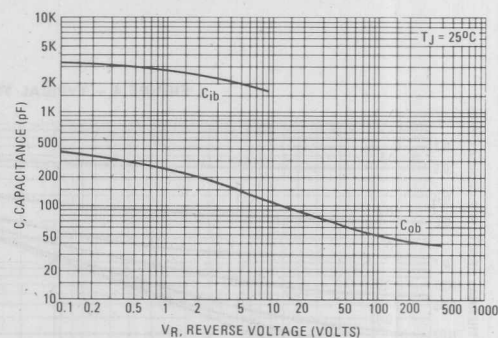


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
TEST CIRCUITS	<div><p>Duty Cycle $\leq 10\%$ $t_r, t_f \leq 10$ ns</p><p>NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}</p></div>	<div><p>+125 V R_C TUT R_B D1 Scope -4.0 V</p></div>
CIRCUIT VALUES	<div>Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16</div> <div>GAP for 200 μH/20A $L_{coil} = 200$ μH</div> <div>$V_{CC} = 20$ V $V_{clamp} = 300$ Vdc</div>	<div>$V_{CC} = 125$ V $R_C = 24.7$ Ω D1 = 1N5820 or Equiv. $R_B = 10$ Ω</div>
TEST WAVEFORMS	<div>OUTPUT WAVEFORMS</div> <div><p>t_1 Adjusted to Obtain I_C</p>$t_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$$t_2 \approx \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$<p>Test Equipment Scope — Tektronix 475 or Equivalent</p></div>	<div><p>25 μs</p><p>+10 V 0 -9.2 V</p><p>$t_r, t_f < 10$ ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C</p></div>

APPLICATIONS INFORMATION FOR SWITCHMODE[▲] SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use

condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737, AN-767, AN-752 and Engineering Bulletins EB-39, EB-65.

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

- (1) The device thermal limitations are not exceeded.
- (2) The turn-on time does not exceed 10 μ s (see standard pulsed forward SOA curves in Figure 1).
- (3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy

handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 — TURN-ON TIME

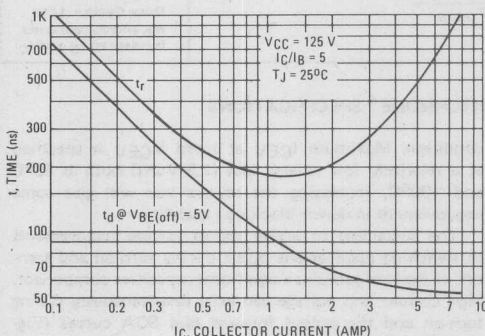


FIGURE 12 — TURN-OFF TIME

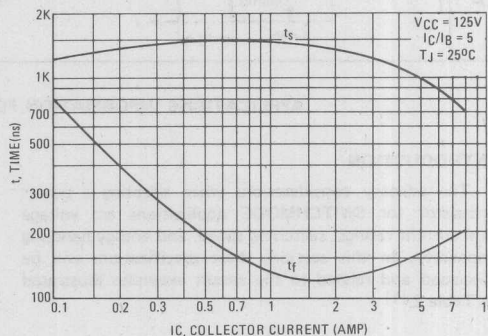


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

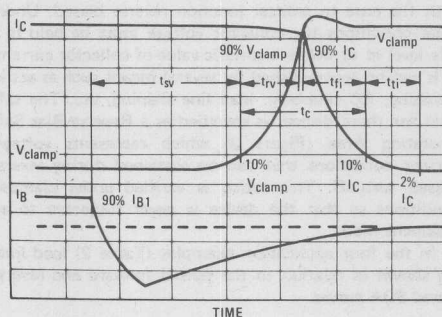


FIGURE 14 — TYPICAL INDUCTIVE SWITCHING WAVEFORMS (at 300 V and 8A with $I_{B1} = 1.6A$ and $V_{BE(off)} = 5V$)

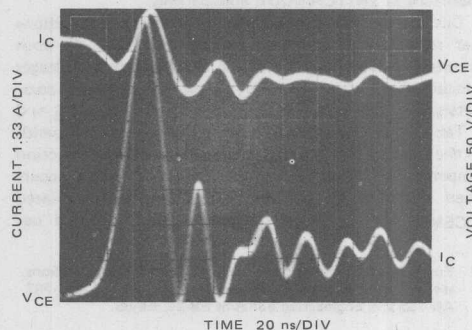


TABLE 2 — APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

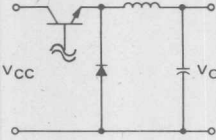
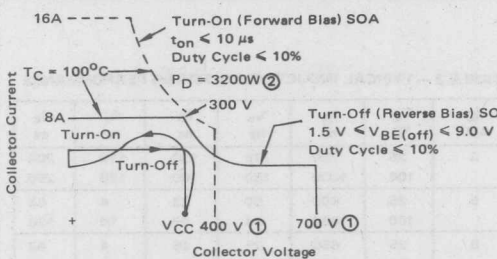
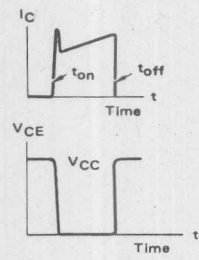
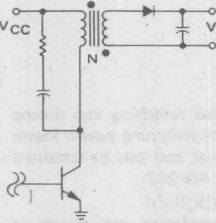
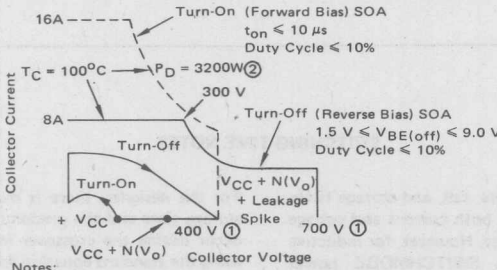
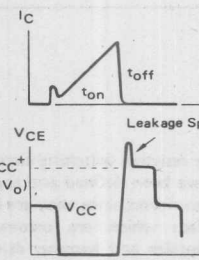
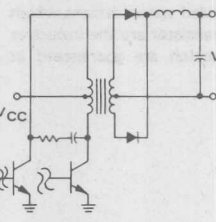
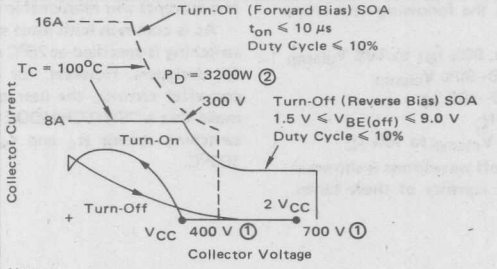
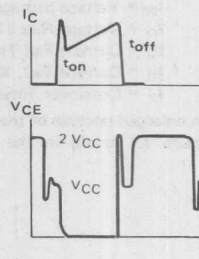
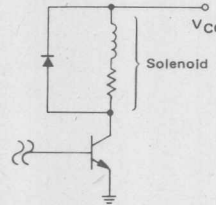
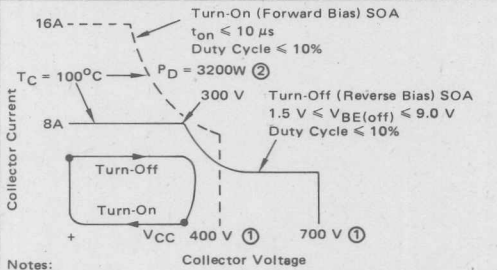
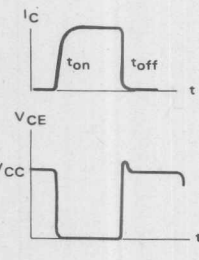
CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
SERIES SWITCHING REGULATOR 	 <p>Notes:</p> <ol style="list-style-type: none"> ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13006 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure. 	
RINGING CHOKE INVERTER 	 <p>Notes:</p> <ol style="list-style-type: none"> ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13006 Ratings are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure 	
PUSH-PULL INVERTER/CONVERTER 	 <p>Notes:</p> <ol style="list-style-type: none"> ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13006 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure. 	
SOLENOID DRIVER 	 <p>Notes:</p> <ol style="list-style-type: none"> ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13006 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure. 	

TABLE 3 — TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{SV} ns	t_{RV} ns	t_{FI} ns	t_{TI} ns	t_C ns
3	25	730	115	100	110	200
	100	1000	150	100	150	250
5	25	600	60	23	4	85
	100	860	84	50	10	136
8	25	650	25	26	4	42
	100	880	52	80	20	160

NOTE: All Data recorded in the Inductive Switching Circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CLAMP}

t_{RV} = Voltage Rise Time, 10–90% V_{CLAMP}

t_{FI} = Current Fall Time, 90–10% I_C

t_{TI} = Current Tail, 10–2% I_C

t_C = Crossover Time, 10% V_{CLAMP} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_C) f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{RV} + t_{FI} \approx t_C$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_C and t_{SV}) which are guaranteed at 100°C.

**MOTOROLA****MJE13008
MJE13009****Designers' Data Sheet****SWITCHMODE^Δ SERIES
NPN SILICON POWER TRANSISTORS**

The MJE13008 and MJE13009 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CE(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 3 to 12 Amp, 25 and 100°C
... t_c @ 8 A, 100°C is 120 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

MAXIMUM RATINGS

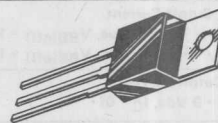
Rating	Symbol	MJE13008	MJE13009	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous	I_C	12		Adc
— Peak (1)	I_{CM}	24		
Base Current — Continuous	I_B	6		Adc
— Peak (1)	I_{BM}	12		
Emitter Current — Continuous	I_E	18		Adc
— Peak (1)	I_{EM}	36		
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2		Watts mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	100	800	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

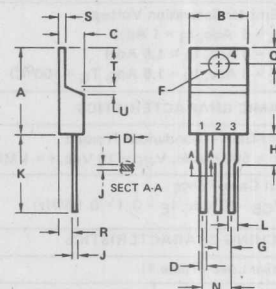
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

**12 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
100 WATTS**

**Designer's Data for
"Worst Case" Conditions**

The Designers' Δ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	300 400	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	— —	— —	1 5	mAdc
Emitter Cutoff Current ($V_{EB} = 9\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 1
Clamped Inductive SOA with Base Reverse Biased	—	See Figure 2

*ON CHARACTERISTICS

DC Current Gain ($I_C = 5\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 8\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	8 6	— —	40 30	—
Collector-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$) ($I_C = 12\text{ Adc}$, $I_B = 3\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — — —	— — — —	1 1.5 3 2	Vdc
Base-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— — —	— — —	1.2 1.6 1.5	Vdc

DYNAMIC CHARACTERISTICS

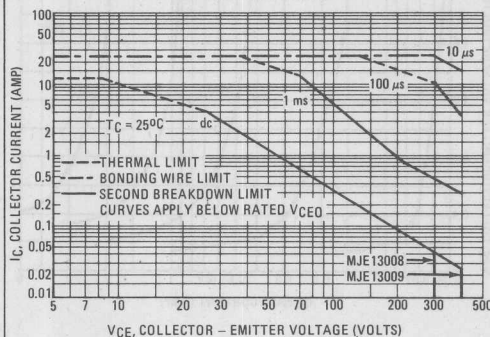
Current-Gain — Bandwidth Product ($I_C = 500\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ MHz}$)	f_T	4	—	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	—	180	—	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)					
Delay Time	$(V_{CC} = 125\text{ Vdc}$, $I_C = 8\text{ A}$,	t_d	—	0.06	0.1 μs
Rise Time	$I_{B1} = I_{B2} = 1.6\text{ A}$, $t_P = 25\text{ }\mu\text{s}$,	t_r	—	0.45	1 μs
Storage Time	Duty Cycle $\leq 1\%$	t_s	—	1.3	3 μs
Fall Time		t_f	—	0.2	0.7 μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time	$(I_C = 8\text{ A}$, $V_{clamp} = 300\text{ Vdc}$,	t_{sv}	—	0.92	2.3 μs
Crossover Time	$I_{B1} = 1.6\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_c	—	0.12	0.7 μs

*Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 2 — REVERSE BIAS SWITCHING SAFE OPERATING AREA

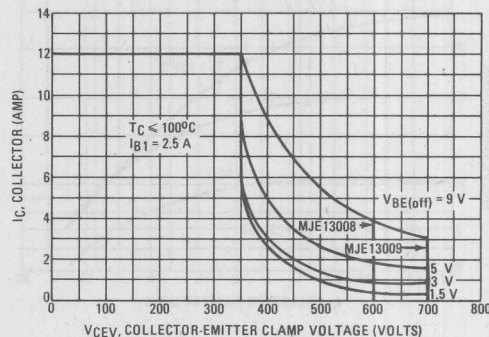
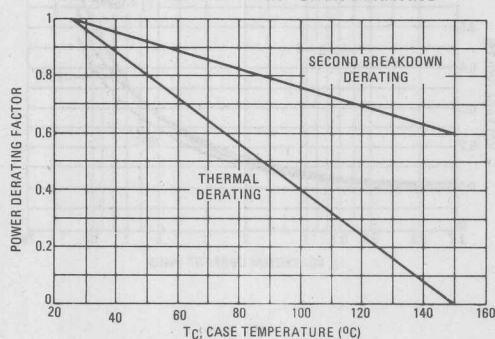


FIGURE 3 — FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_J(\text{pk})$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 — TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

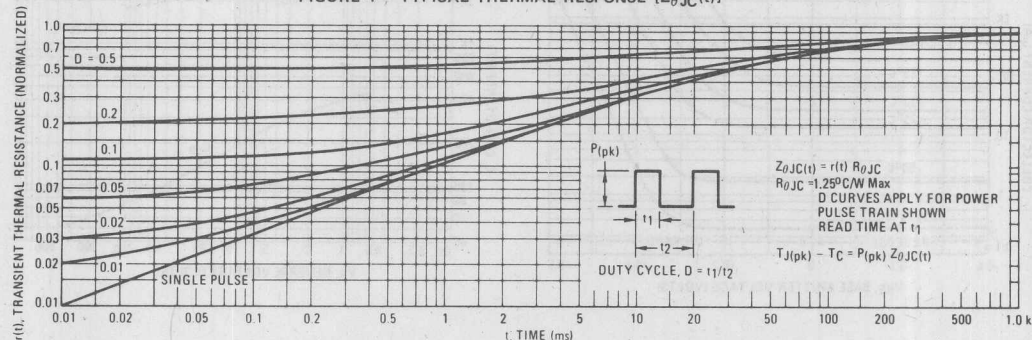


FIGURE 5 — DC CURRENT GAIN

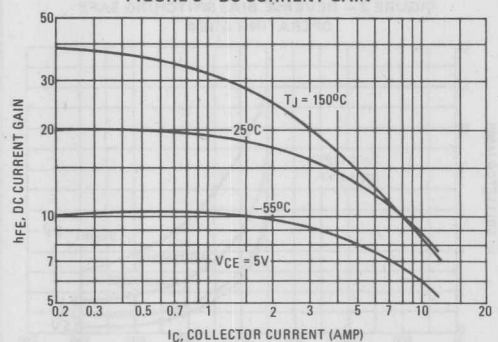


FIGURE 6 — COLLECTOR SATURATION REGION

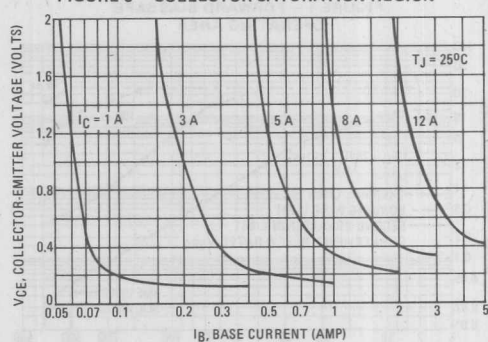


FIGURE 7 — BASE-EMITTER SATURATION VOLTAGE

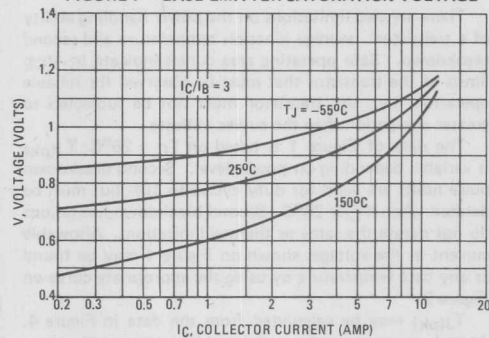


FIGURE 8 — COLLECTOR-EMITTER SATURATION VOLTAGE

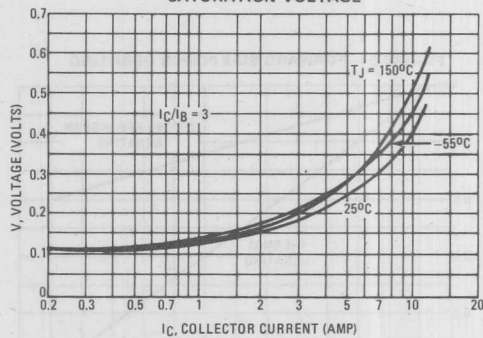


FIGURE 9 — COLLECTOR CUTOFF REGION

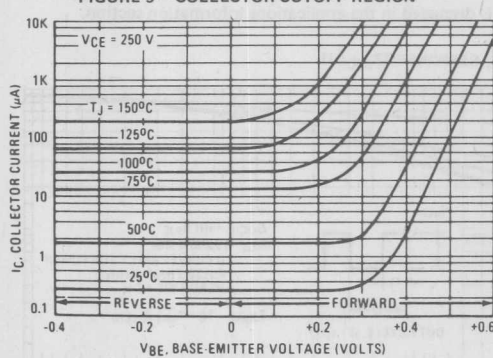
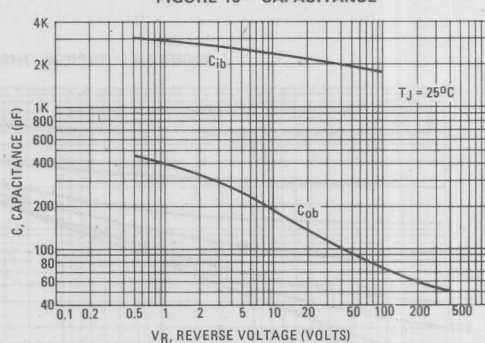


FIGURE 10 — CAPACITANCE



VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

- (1) The device thermal limitations are not exceeded.
- (2) The turn-on time does not exceed $10 \mu\text{s}$ (see standard pulsed forward SOA curves in Figure 1).
- (3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy

handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 — TURN-ON TIME

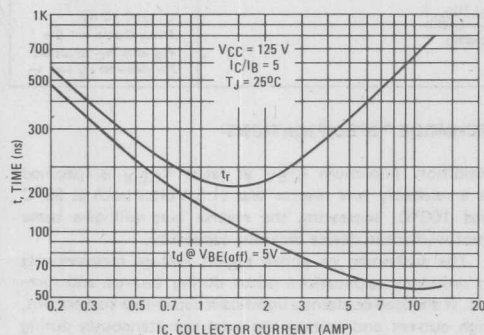


FIGURE 12 — TURN-OFF TIME

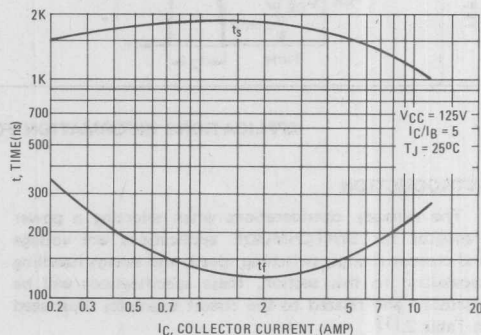


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

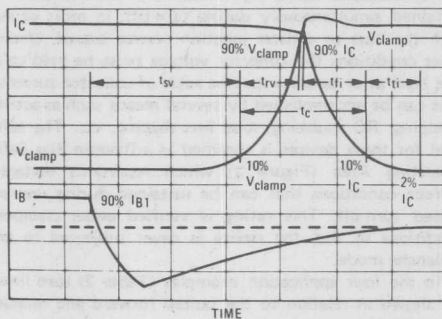
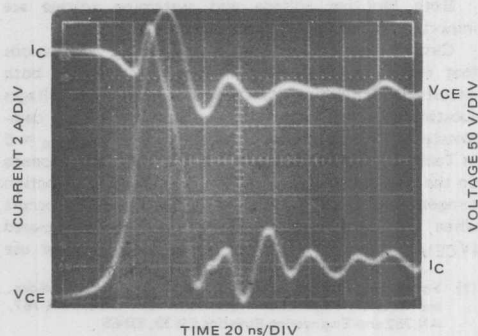
FIGURE 14 — TYPICAL INDUCTIVE SWITCHING WAVEFORMS (at 300 V and 12 A with $I_{B1} = 2.4 \text{ A}$ and $V_{BE(off)} = 5 \text{ V}$)

TABLE 2 — APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

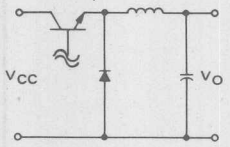
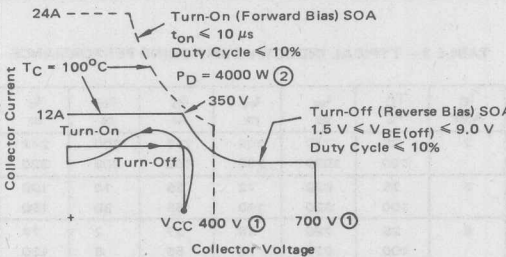
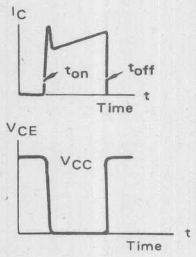
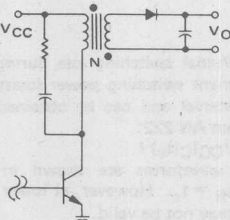
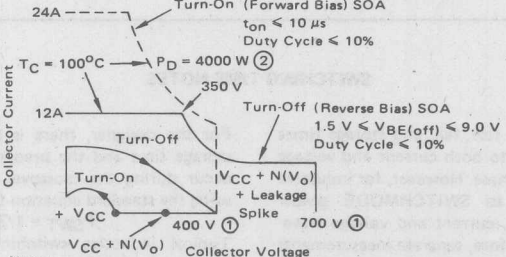
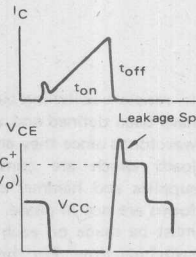
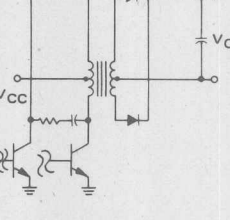
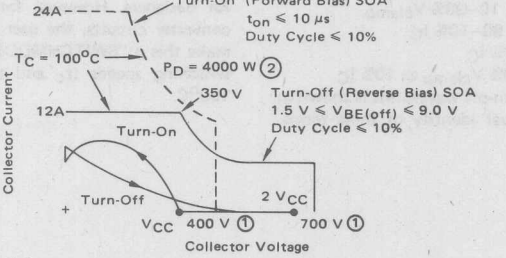
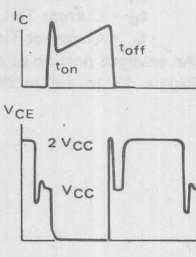
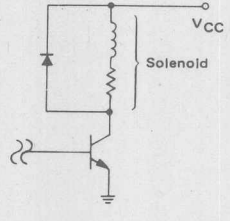
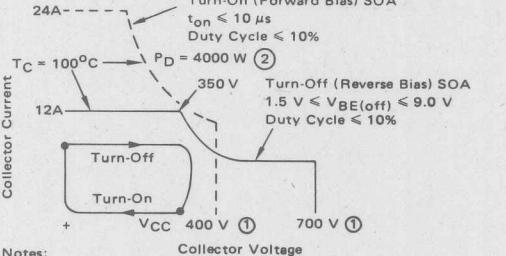
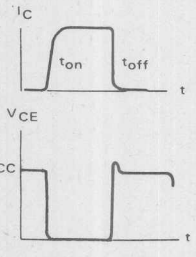
CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
SERIES SWITCHING REGULATOR 	 <p>Notes:</p> <p>① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.</p> <p>② See AN-569 for Pulse Power Derating Procedure.</p>	
RINGING CHOKE INVERTER 	 <p>Notes:</p> <p>① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.</p> <p>② See AN-569 For Pulse Power Derating Procedure</p>	
PUSH-PULL INVERTER/CONVERTER 	 <p>Notes:</p> <p>① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.</p> <p>② See AN-569 for Pulse Power Derating Procedure.</p>	
SOLENOID DRIVER 	 <p>Notes:</p> <p>① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.</p> <p>② See AN-569 for Pulse Power Derating Procedure.</p>	

TABLE 3 — TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I _C AMP	T _C °C	t _{sv} ns	t _{rv} ns	t _{fi} ns	t _{ti} ns	t _c ns
3	25	770	100	150	200	240
	100	1000	230	160	200	320
5	25	630	72	26	10	100
	100	820	100	55	30	180
8	25	720	55	27	2	77
	100	920	70	50	8	120
12	25	640	20	17	2	41
	100	800	32	24	4	54

NOTE: All Data recorded in the inductive Switching Circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

Typical inductive switching waveforms are shown in Figure 14. In general, t_{rv} + t_{fi} ≈ t_c. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

**MOTOROLA**

NPN PNP
MJE15028 MJE15029
MJE15030 MJE15031

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

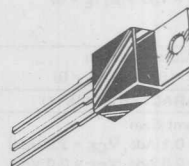
... designed for use as high-frequency drivers in audio amplifiers.

- DC Current Gain Specified to 4.0 Amperes
 $h_{FE} = 40(\text{Min}) @ I_C = 3.0 \text{ Adc}$
 $= 20(\text{Min}) @ I_C = 4.0 \text{ Adc}$
- Collector-Emitter Sustaining Voltage —
 $V_{CE(sus)} = 120 \text{ Vdc (Min)} - \text{MJE15028, MJE15029}$
 $= 150 \text{ Vdc (Min)} - \text{MJE15030, MJE15031}$
- High Current Gain — Bandwidth Product
 $f_T = 30 \text{ MHz (Min)} @ I_C = 500 \text{ mAdc}$
- TO-220AB Compact Package
- TO-66 Leadform Also Available

8 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

120-150 VOLTS
50 WATTS



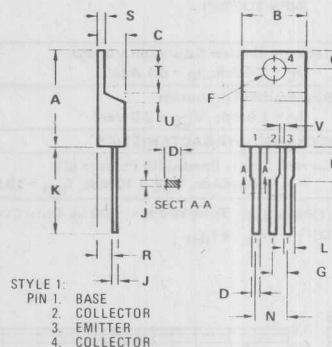
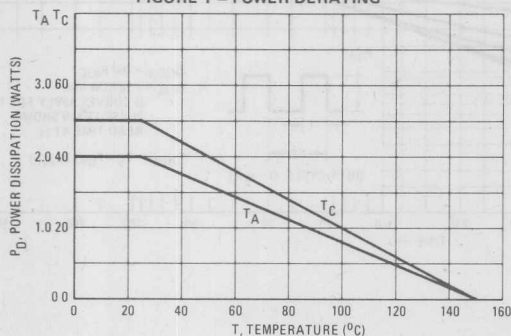
MAXIMUM RATINGS

Rating	Symbol	MJE15028 MJE15029	MJE15030 MJE15031	Unit
Collector-Emitter Voltage	V_{CEO}	120	150	Vdc
Collector-Base Voltage	V_{CB}	120	150	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	8.0		Adc
Collector Current — Peak		16		
Base Current	I_B	2.0		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	50		Watts
Derate above 25°C		0.40		W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.0		Watts
Derate above 25°C		0.016		W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

FIGURE 1 — POWER DERATING



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	120 150	— —	Vdc
Collector Cutoff Current ($V_{CE} = 120\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 150\text{ Vdc}$, $I_B = 0$)	I_{CEO}	— —	0.1 0.1	mA
Collector Cutoff Current ($V_{CB} = 120\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 150\text{ Vdc}$, $I_E = 0$)	I_{CBO}	— —	10 10	μA
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	10	μA
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 0.1\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$) ($I_C = 2.0\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$) ($I_C = 3.0\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$) ($I_C = 4.0\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$)	h_{FE}	40 40 40 20	— — — —	—
DC Current Gain Linearity (V_{CE} From 2.0V to 20V, I_C From 0.1A to 3A) (NPN TO PNP)	h_{FE}	Typ 2 3		—
Collector-Emitter Saturation Voltage ($I_C = 1.0\text{ A}$, $I_B = 0.1\text{ A}$)	$V_{CE(sat)}$	—	0.5	Vdc
Base-Emitter On Voltage ($I_C = 1.0\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) ($I_C = 500\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 10\text{ MHz}$)	f_T	30	—	MHz

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 — THERMAL RESPONSE

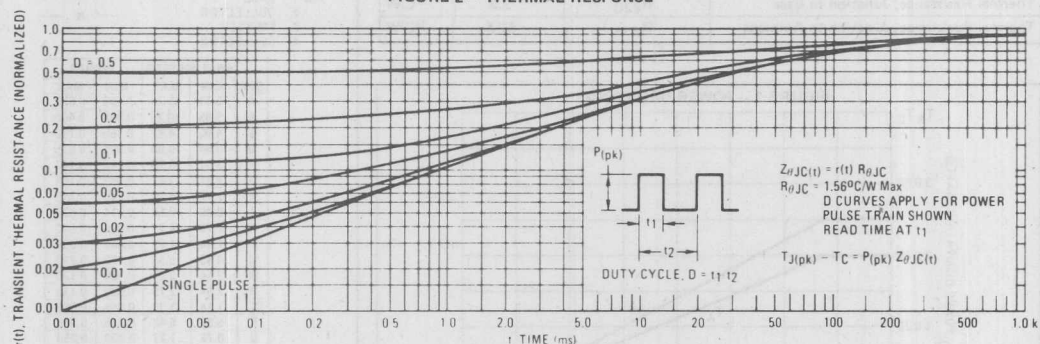
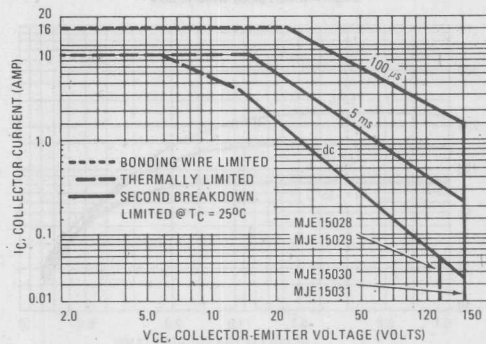


FIGURE 3 – FORWARD BIAS
SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – REVERSE-BIAS SWITCHING
SAFE OPERATING AREA

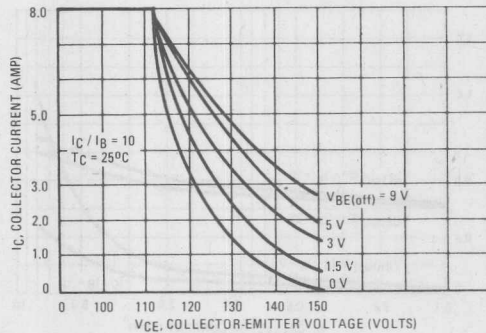


FIGURE 5 – CAPACITANCES

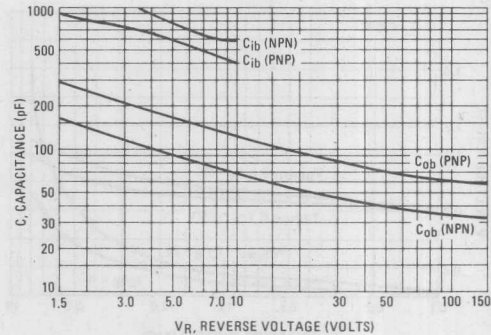


FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

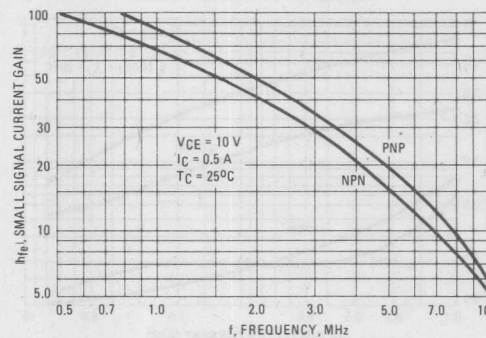
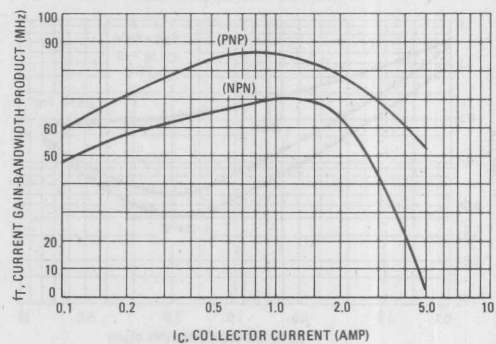


FIGURE 7 – CURRENT GAIN-BANDWIDTH PRODUCT



NPN MJE15028 • MJE15030
PNP MJE15029 • MJE15031

FIGURE 8 – DC CURRENT GAIN

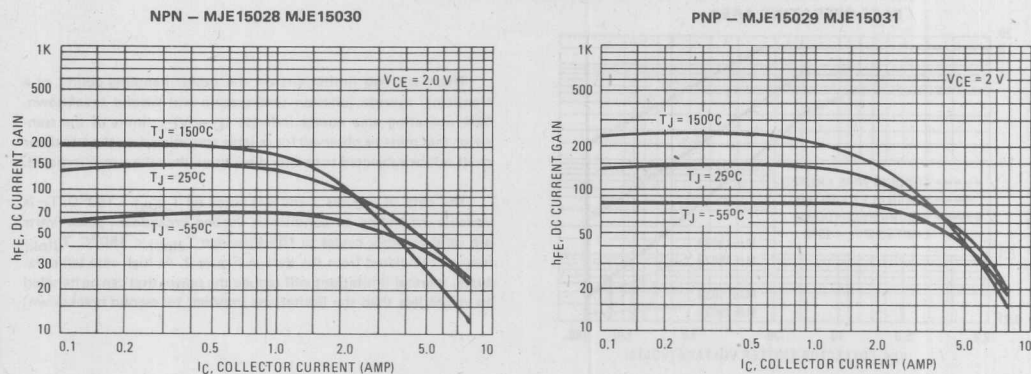


FIGURE 9 – "ON" VOLTAGE

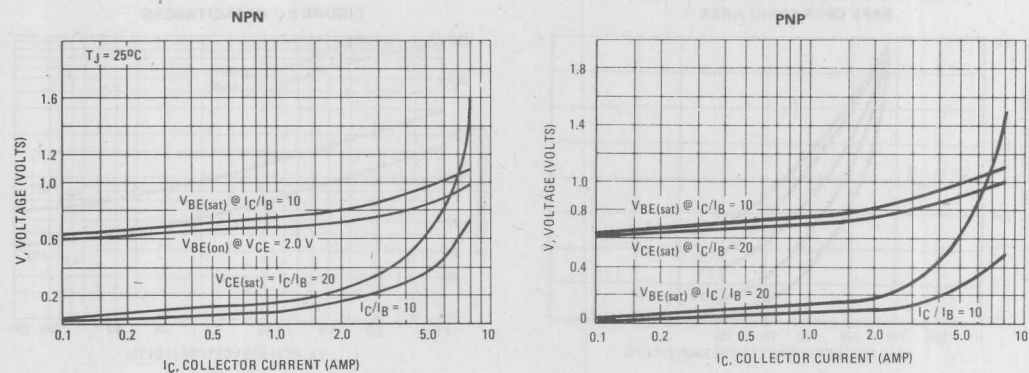


FIGURE 10 – TURN-ON TIMES

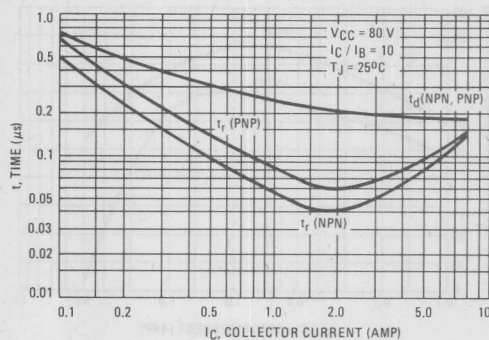
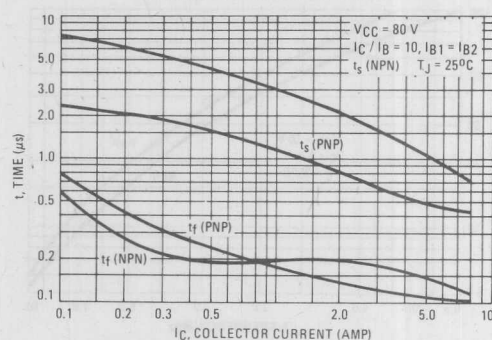


FIGURE 11 – TURN-OFF TIMES



**MOTOROLA****MJE16002
MJE16004****Designer's Data Sheet****SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS**

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJE16004 is a selected high-gain version of the MJE16002 for applications where drive current is limited.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 50 ns Inductive Fall Time — 75°C (Typ)
 - 70 ns Inductive Crossover Time — 75°C (Typ)
 - 500 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range —65 to +150°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

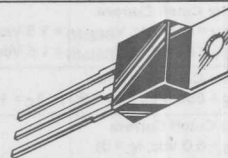
MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
— Peak (1)	I_{CM}	10	
Base Current — Continuous	I_B	4.0	Adc
— Peak (1)	I_{BM}	8.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	80	Watts
— @ $T_C = 100^\circ\text{C}$		32	
Derate above 25°C		0.64	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

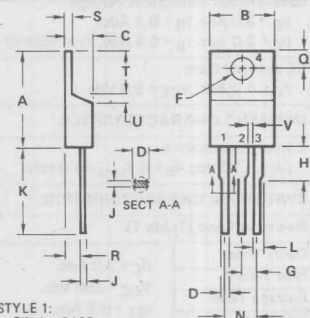
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

5 AMPERE**NPN SILICON
POWER TRANSISTORS****450 VOLTS
80 WATTS****Designer's Data for
"Worst Case" Conditions**

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTORNOTE:
1. DIM. L & H APPLIES
TO ALL LEADS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

**CASE 221A-02
TO-220AB**

MJE16002

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.0 2.5 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	5.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	200	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$(I_C = 3.0\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 0.4\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	$(I_{B2} = 0.8\text{ Adc}$, $R_{B2} = 8.0\ \Omega)$	t_d	—	30	100	ns
Rise Time			t_r	—	100	300	
Storage Time			t_s	—	1000	3000	
Fall Time			t_f	—	60	300	
Storage Time		$(V_{BE(off)} = 5.0\text{ Vdc})$	t_s	—	400	—	
Fall Time			t_f	—	130	—	

Inductive Load (Table 2)

Storage Time	$(I_C = 3.0\text{ Adc}$, $I_{B1} = 0.4\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	$(T_J = 100^\circ\text{C})$	t_{sv}	—	500	1600	ns
Fall Time			t_{fi}	—	100	200	
Crossover Time			t_c	—	120	250	
Storage Time		$(T_J = 150^\circ\text{C})$	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

$$*\beta_{ef} = \frac{I_C}{I_{B1}}$$

MJE16004

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mA _{dc}
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mA _{dc}
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mA _{dc}

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 0.15\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.0 2.5 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	200	pF
--	----------	---	---	-----	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$I_C = 3.0\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 0.3\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$	$I_{B2} = 0.6\text{ Adc}$, $R_{B2} = 8.0\ \Omega$) ($V_{BE(off)} = 5.0\text{ Vdc}$)	t_d	—	30	100	ns
Rise Time			t_r	—	130	300	
Storage Time			t_s	—	800	2700	
Fall Time			t_f	—	80	350	
Storage Time			t_{sv}	—	250	—	
Fall Time			t_{fv}	—	60	—	

Inductive Load (Table 2)

Storage Time	$I_C = 3.0\text{ Adc}$, $I_{B1} = 0.3\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$	$(T_J = 100^\circ\text{C})$	t_{sv}	—	400	1300	ns
Fall Time			t_{fv}	—	80	150	
Crossover Time			t_c	—	90	200	
Storage Time		$(T_J = 150^\circ\text{C})$	t_{sv}	—	450	—	
Fall Time			t_{fv}	—	100	—	
Crossover Time			t_c	—	110	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

$$\beta_{eff} = \frac{I_C}{I_{B1}}$$

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

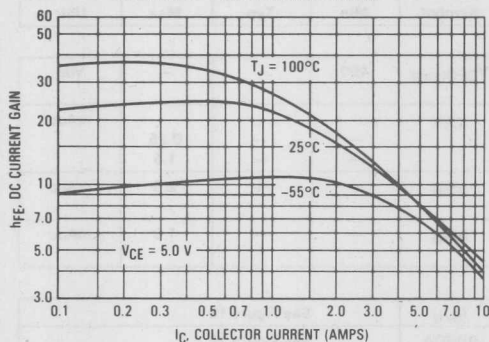


FIGURE 2 — COLLECTOR SATURATION REGION

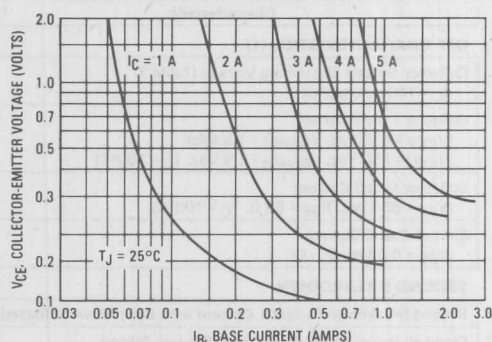


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

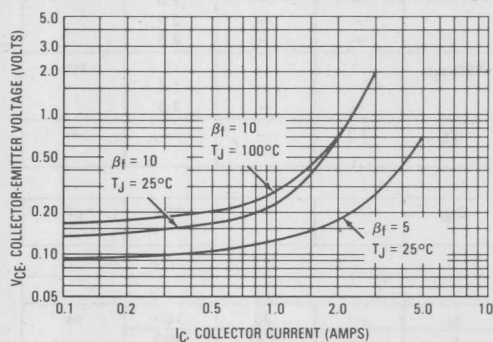


FIGURE 4 — BASE-EMITTER VOLTAGE

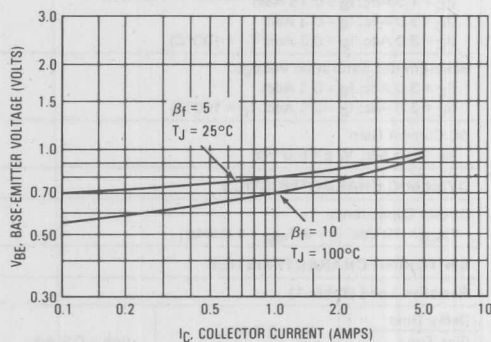


FIGURE 5 — COLLECTOR CUTOFF REGION

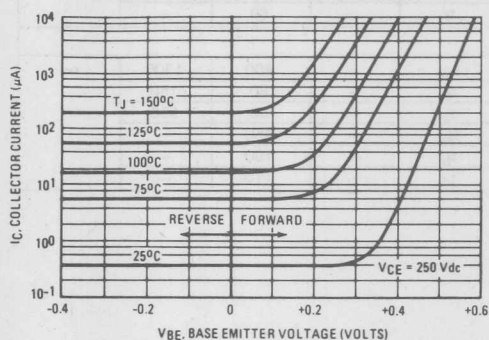
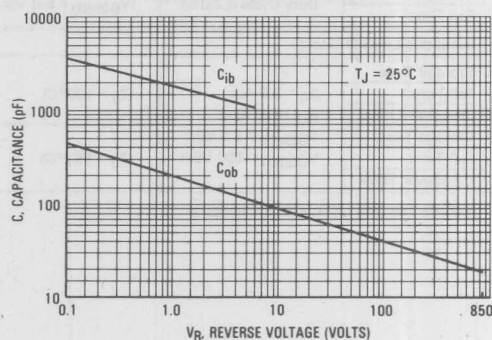


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

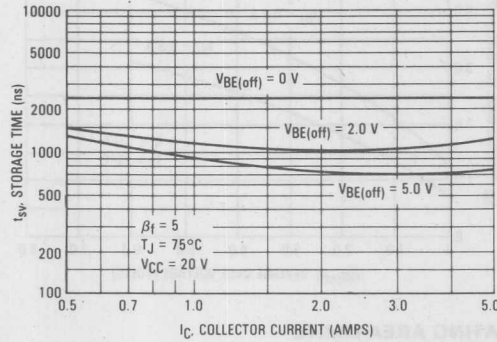


FIGURE 8 — STORAGE TIME

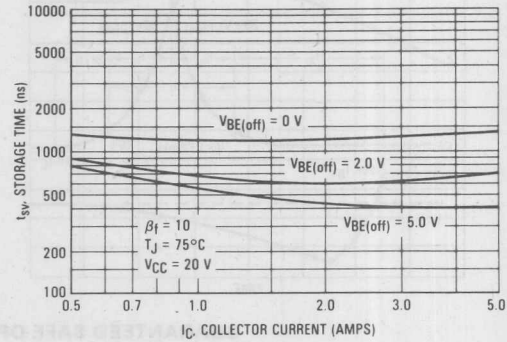


FIGURE 9 — COLLECTOR CURRENT FALL TIME

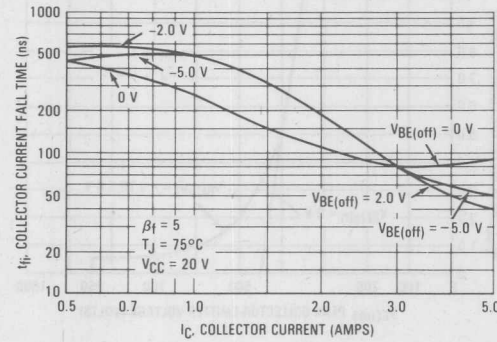


FIGURE 10 — COLLECTOR CURRENT FALL TIME

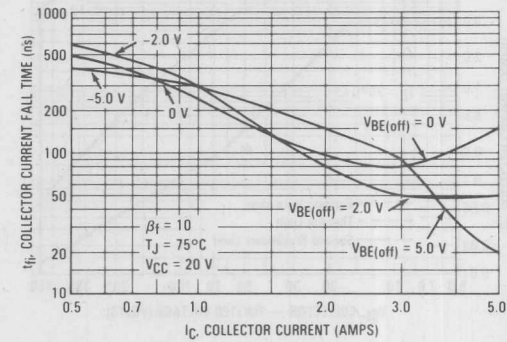


FIGURE 11 — Crossover TIME

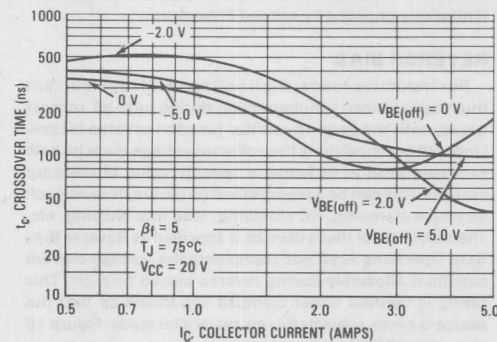


FIGURE 12 — Crossover TIME

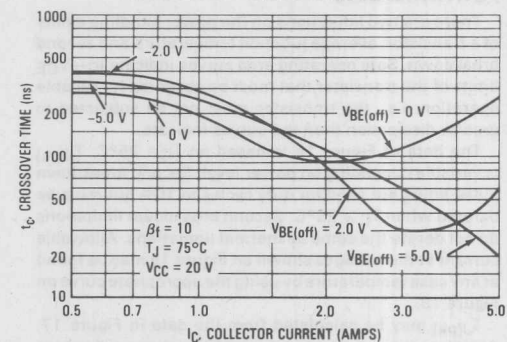


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

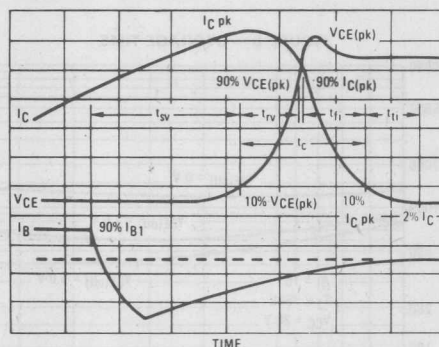
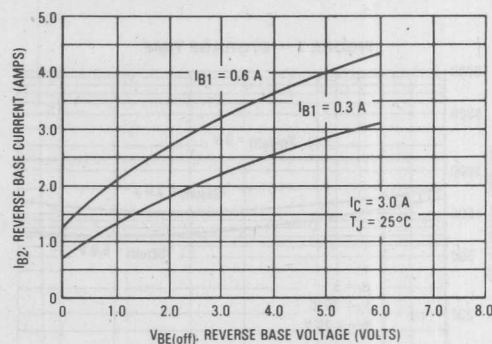


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

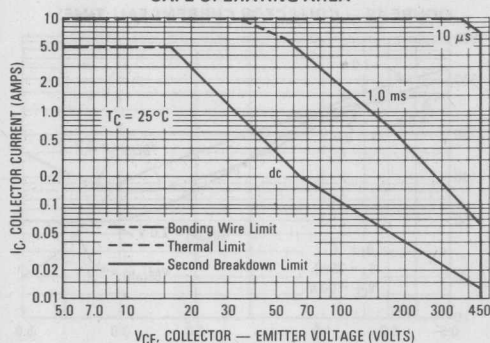
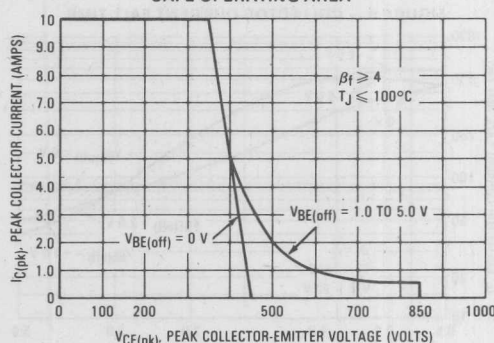


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_J(pk)$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce

the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

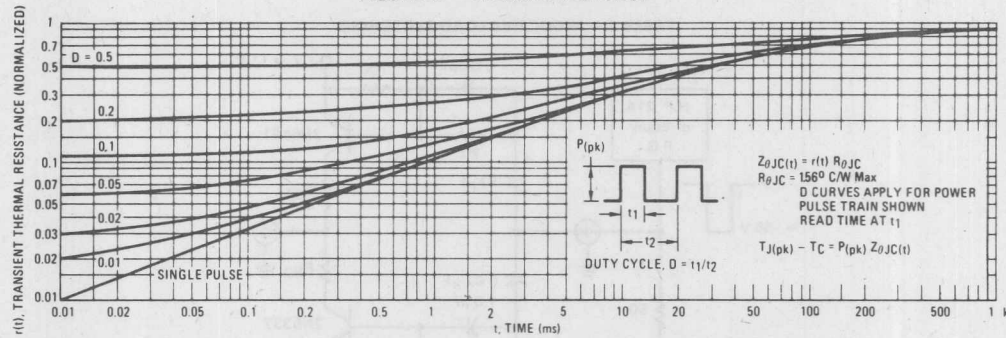


FIGURE 18 — POWER DERATING

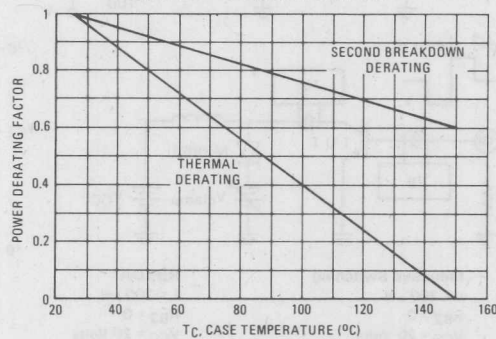
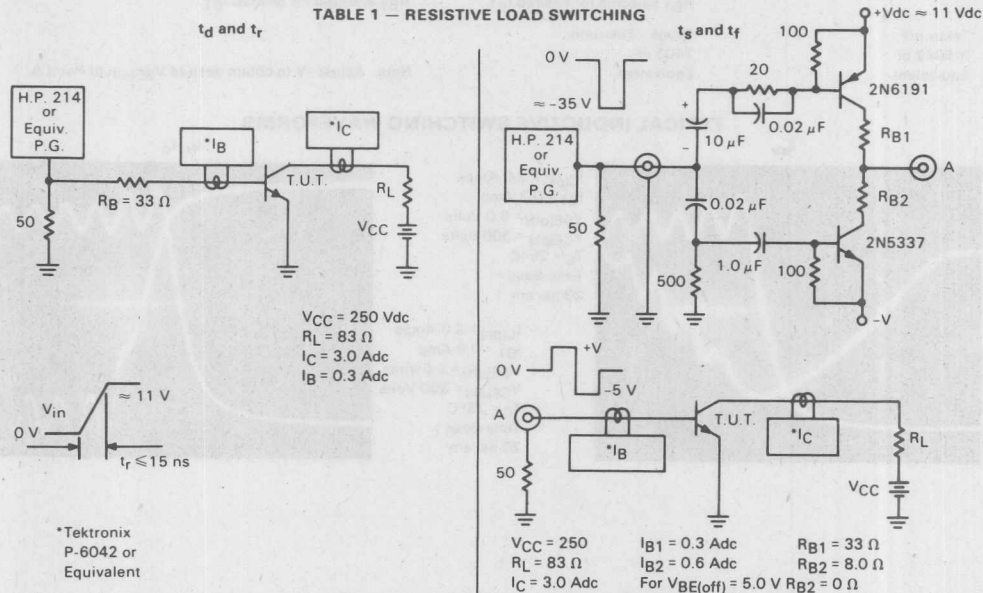
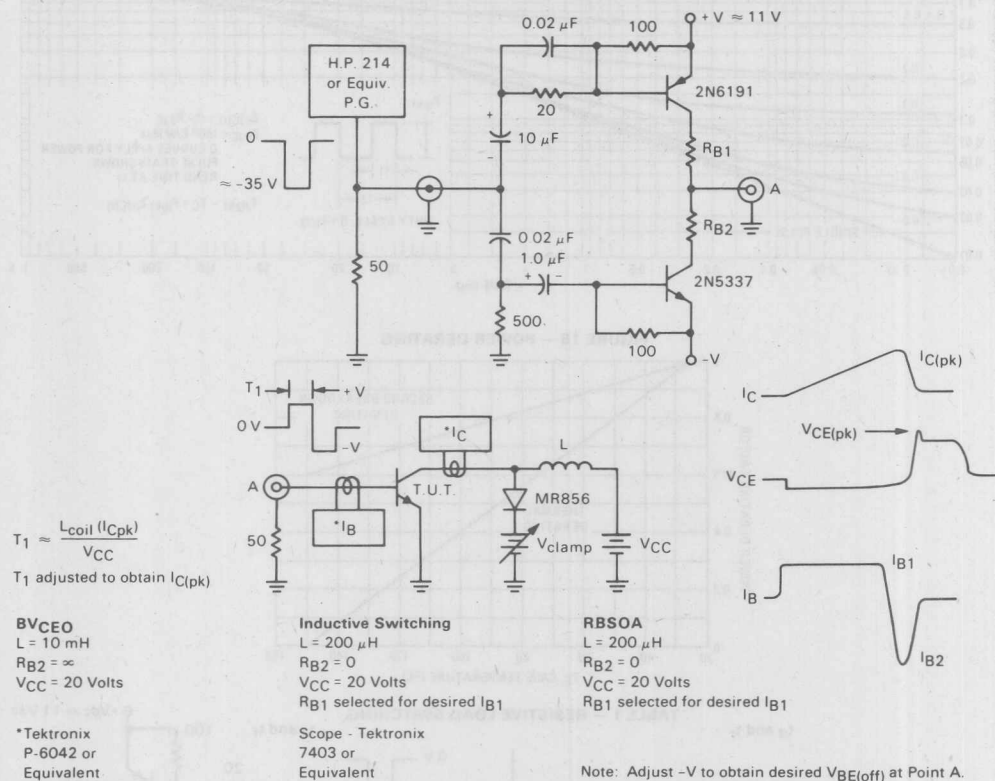


TABLE 1 — RESISTIVE LOAD SWITCHING

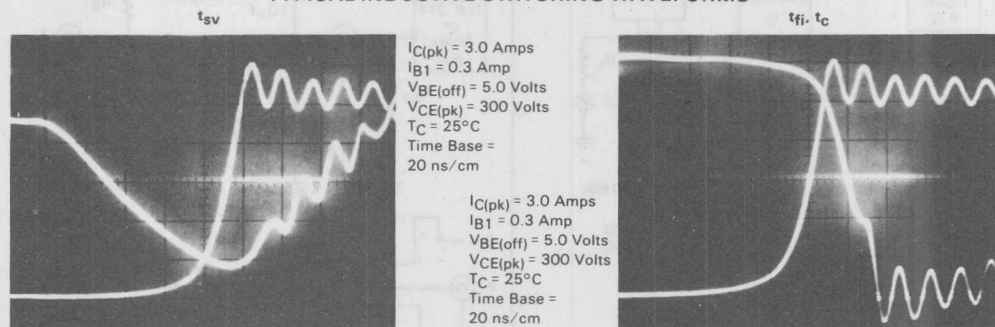


*Note: Adjust $-V$ to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



TYPICAL INDUCTIVE SWITCHING WAVEFORMS



**MOTOROLA****MPS-U01
MPS-U01A****NPN SILICON ANNULAR TRANSISTORS**

... designed for complementary symmetry audio circuits to 5 Watts output.

- Excellent Current Gain Linearity – 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.5 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Adc}$
- Complements to PNP MPS-U51 and MPS-U51A
- Uniwatt Package for Excellent Thermal Properties –
1.0 Watt @ $T_A = 25^\circ\text{C}$

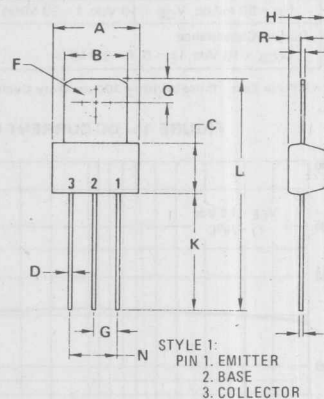
**NPN SILICON
AUDIO TRANSISTORS****MAXIMUM RATINGS**

Rating	Symbol	MPS-U01	MPS-U01A	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Base Voltage	V_{CB}	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	2.0		Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0		Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80		Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^\circ\text{C/W}$

Uniwatt packages can be To-5 lead formed by adding -5 to the device title and tab formed for flush mounting by adding -1 to the device title.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 10\text{ mAdc}$, $I_B = 0$)	BV_{CEO}	30 40	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100\text{ }\mu\text{Adc}$, $I_E = 0$)	BV_{CBO}	40 50	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100\text{ }\mu\text{Adc}$, $I_C = 0$)	BV_{EBO}	5.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 30\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 40\text{ Vdc}$, $I_E = 0$)	I_{CBO}	— —	0.1 0.1	μAdc
Emitter Cutoff Current ($V_{BE} = 3.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS(1)				
DC Current Gain ($I_C = 10\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 100\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 1.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	55 60 50	— — —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.1\text{ Adc}$)	$V_{CE(sat)}$	—	0.5	Vdc
Base-Emitter On Voltage ($I_C = 1.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain-Bandwidth Product ($I_C = 50\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 20\text{ MHz}$)	f_T	50	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	C_{ob}	—	20	pF

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 1 — DC CURRENT GAIN

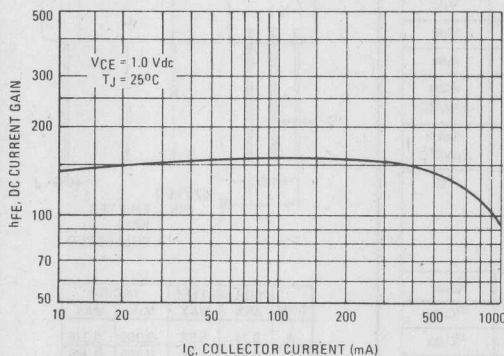


FIGURE 2 — "ON" VOLTAGES

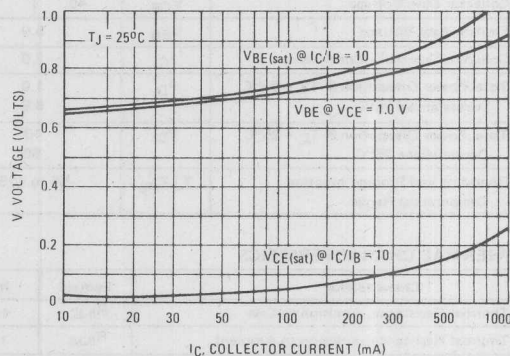
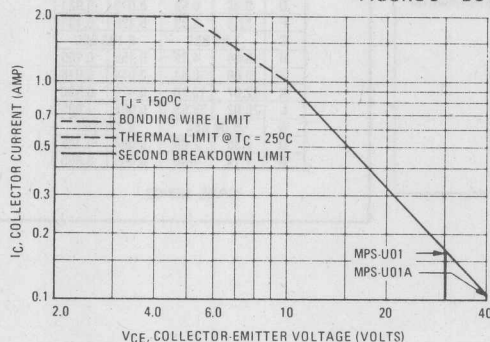


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

**MOTOROLA****MPS-U05****MPS-U06****NPN SILICON ANNULAR
AMPLIFIER TRANSISTORS**

... designed for general-purpose, high-voltage amplifier and driver applications.

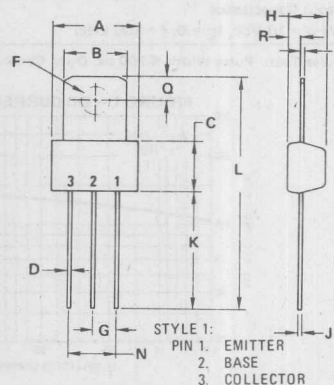
- High Collector-Emitter Breakdown Voltage –
BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mA_{dc} – MPS-U05
80 Vdc (Min) @ I_C = 1.0 mA_{dc} – MPS-U06
- High Power Dissipation – P_D = 10 W @ T_C = 25°C
- Complements to PNP MPS-U55 and MPS-U56

**NPN SILICON
AMPLIFIER TRANSISTORS****MAXIMUM RATINGS**

Rating	Symbol	MPS-U05	MPS-U06	Unit
Collector-Emitter Voltage	V _{CEO}	60	80	Vdc
Collector-Base Voltage	V _{CB}	60	80	Vdc
Emitter-Base Voltage	V _{EB}		4.0	Vdc
Collector Current – Continuous	I _C		2.0	Adc
Total Power Dissipation @ T _A = 25°C Derate above 25°C	P _D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	R _{θJA}	125	°C/W

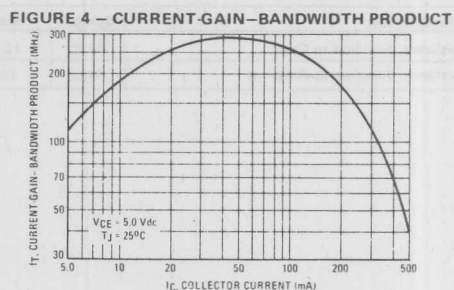
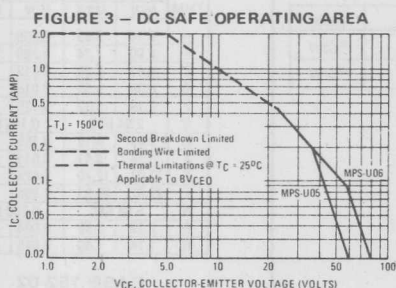
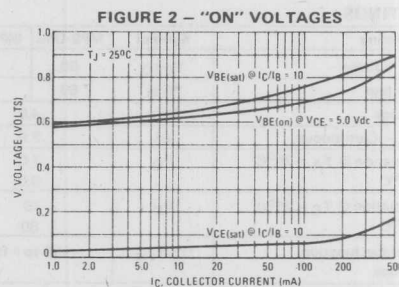
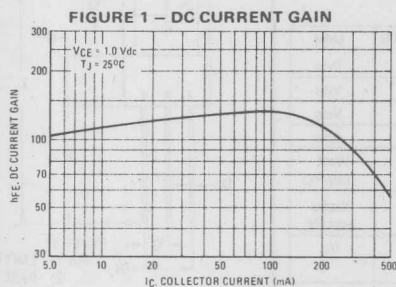


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = 1.0\text{ mAdc}$, $I_B = 0$)	BV_{CEO}	60 80	— —	— —	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100\text{ }\mu\text{Adc}$, $I_C = 0$)	BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 40\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 60\text{ Vdc}$, $I_E = 0$)	I_{CBO}	— —	— —	100 100	nAdc
ON CHARACTERISTICS					
DC Current Gain (1) ($I_C = 50\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 250\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 500\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	80 60 —	125 100 55	— — —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 250\text{ mAdc}$, $I_B = 10\text{ mAdc}$) ($I_C = 250\text{ mAdc}$, $I_B = 25\text{ mAdc}$)	$V_{CE(sat)}$	— —	0.18 0.1	0.4 —	Vdc
Base-Emitter On Voltage (1) ($I_C = 250\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$)	$V_{BE(on)}$	—	0.74	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain-Bandwidth Product (1) ($I_C = 250\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$, $f = 100\text{ MHz}$)	f_T	50	150	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 100\text{ kHz}$)	C_{ob}	—	6.0	12	pF

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**NPN SILICON ANNULAR
AMPLIFIER TRANSISTOR**

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
 $BV_{CEO} = 100 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc}$
- High Power Dissipation — $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complement to PNP MPS-U57

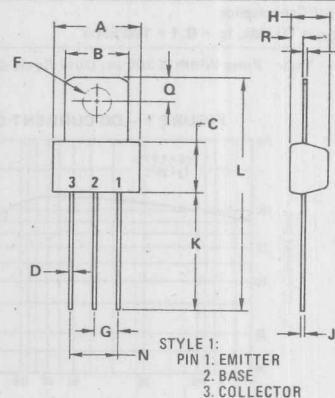
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^\circ\text{C/W}$

**NPN SILICON
AMPLIFIER TRANSISTOR**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0\text{ mA}$, $I_B = 0$)	BV_{CEO}	100	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100\text{ }\mu\text{A}$, $I_C = 0$)	BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 80\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	—	100	nAdc

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 50\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 250\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 500\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}				
		60	110	—	—
		30	65	—	—
		—	33	—	—
Collector-Emitter Saturation Voltage (1) ($I_C = 250\text{ mA}$, $I_B = 10\text{ mA}$) ($I_C = 250\text{ mA}$, $I_B = 25\text{ mA}$)	$V_{CE(sat)}$	—	0.18	0.4	Vdc
		—	0.1	—	—
Base-Emitter On Voltage (1) ($I_C = 250\text{ mA}$, $V_{CE} = 5.0\text{ Vdc}$)	$V_{BE(on)}$	—	0.76	1.2	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product (1) ($I_C = 250\text{ mA}$, $V_{CE} = 5.0\text{ Vdc}$, $f = 100\text{ MHz}$)	f_T	50	150	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 100\text{ kHz}$)	C_{ob}	—	6.0	12	pF

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 1 — DC CURRENT GAIN

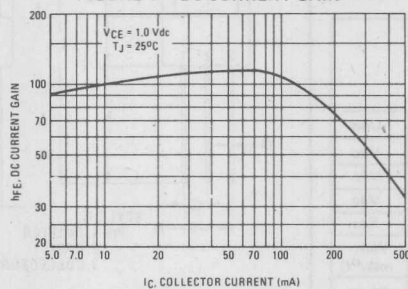


FIGURE 2 — "ON" VOLTAGES

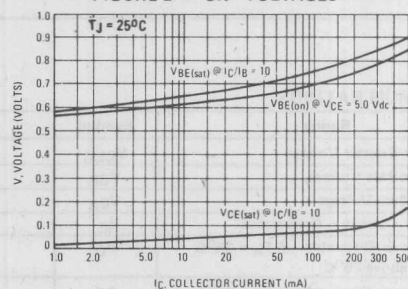


FIGURE 3 — DC SAFE OPERATING AREA

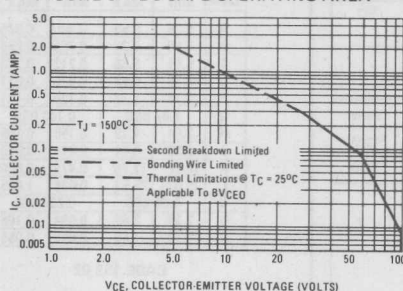
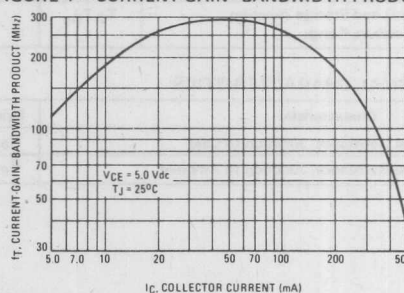


FIGURE 4 — CURRENT-GAIN-BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



NPN SILICON DARLINGTON AMPLIFIER TRANSISTOR

... designed for amplifier and driver applications.

- High DC Current Gain —
 $h_{FE} = 25,000$ (Min) @ $I_C = 200$ mA
 $15,000$ (Min) @ $I_C = 500$ mA
- Collector-Emitter Breakdown Voltage —
 $BV_{CES} = 40$ Vdc (Min) @ $I_C = 100$ μ A
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 1.5$ Vdc @ $I_C = 1.0$ A
- Monolithic Construction for High Reliability
- Complement to PNP MPS-U95

MAXIMUM RATINGS

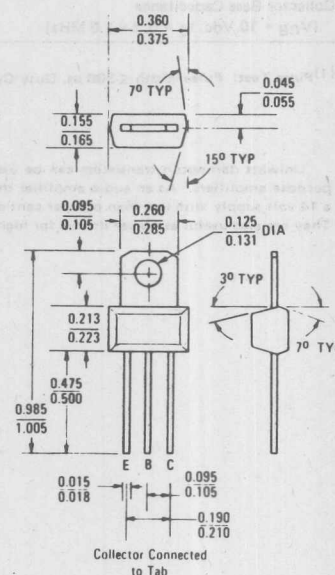
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(1)}$	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	12	Vdc
Collector Current	I_C	2.0	A
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	125	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	θ_{JC}	12.5	$^\circ\text{C/W}$

(1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical. BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by noise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.

NPN SILICON DARLINGTON TRANSISTOR



CASE 152

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = 100\ \mu\text{Adc}$, $V_{BE} = 0$)	BV_{CES}	40	—	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100\ \mu\text{Adc}$, $I_E = 0$)	BV_{CBO}	50	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\ \mu\text{Adc}$, $I_C = 0$)	BV_{EBO}	12	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 30\ \text{Vdc}$, $I_E = 0$)	I_{CBO}	—	—	100	nAdc
Emitter Cutoff Current ($V_{EB} = 10\ \text{Vdc}$, $I_C = 0$)	I_{EBO}	—	—	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain ($I_C = 200\ \text{mAdc}$, $V_{CE} = 5.0\ \text{Vdc}$) ($I_C = 500\ \text{mAdc}$, $V_{CE} = 5.0\ \text{Vdc}$) ($I_C = 1.0\ \text{Adc}$, $V_{CE} = 5.0\ \text{Vdc}$)	h_{FE}	25,000 15,000 4,000	65,000 35,000 12,000	150,000 — —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0\ \text{Adc}$, $I_B = 2.0\ \text{mAdc}$)	$V_{CE(sat)}$	—	1.2	1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0\ \text{Adc}$, $I_B = 2.0\ \text{mAdc}$)	$V_{BE(sat)}$	—	1.85	2.0	Vdc
Base-Emitter On Voltage ($I_C = 1.0\ \text{Adc}$, $V_{CE} = 5.0\ \text{Vdc}$)	$V_{BE(on)}$	—	1.7	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 200\ \text{mAdc}$, $V_{CE} = 5.0\ \text{Vdc}$, $f = 100\ \text{MHz}$)	$ h_{fe} $	1.0	3.2	—	—
Collector Base Capacitance ($V_{CB} = 10\ \text{Vdc}$, $I_E = 0$, $f = 1.0\ \text{MHz}$)	C_{cb}	—	2.5	6.0	pF

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Uniwart darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one per cent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also useful as power drivers for high current application such as voltage regulators.

FIGURE 1 - DC CURRENT GAIN

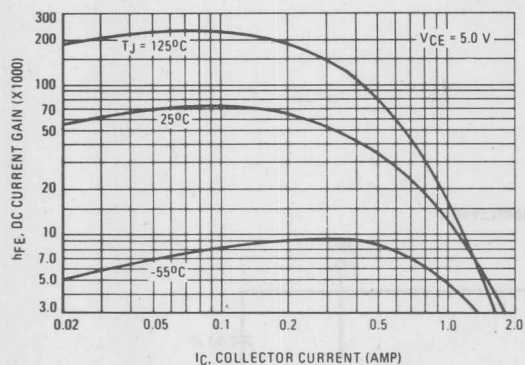


FIGURE 2 - SMALL-SIGNAL CURRENT GAIN

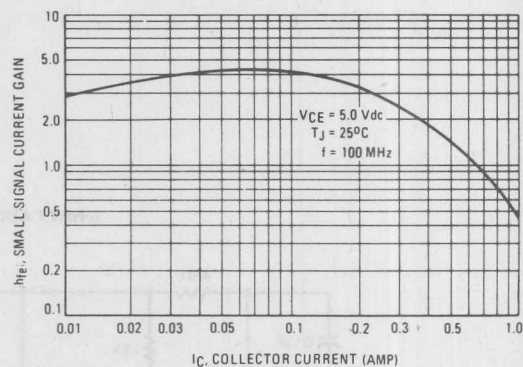


FIGURE 3 - "ON" VOLTAGES

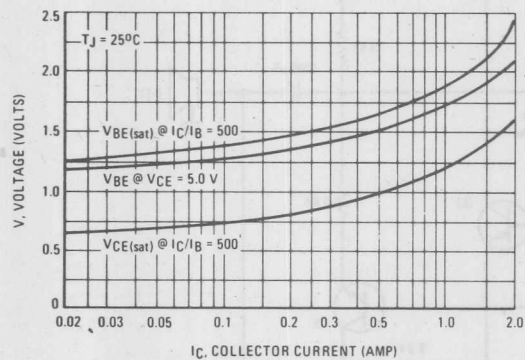


FIGURE 4 - TEMPERATURE COEFFICIENT

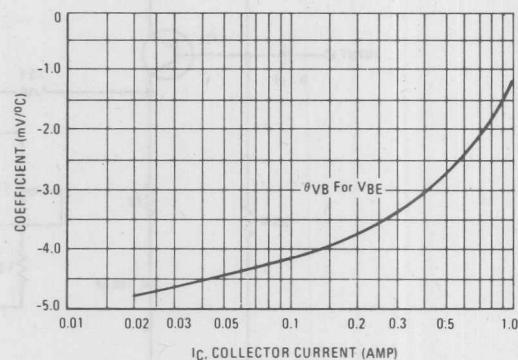
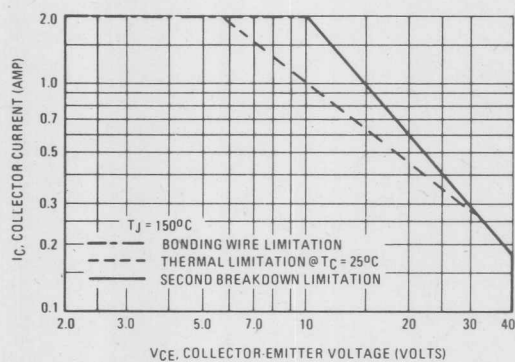


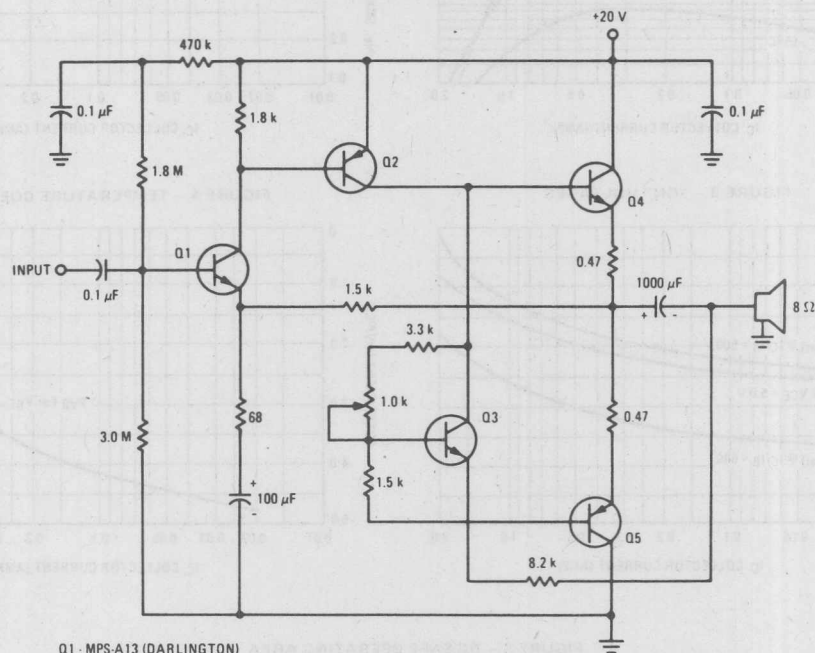
FIGURE 5 - DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

5-WATT AUDIO AMPLIFIER



- Q1 - MPS-A13 (DARLINGTON)
 Q2 - MPS-A70
 Q3 - MPS-A20
 Q4 - MPS-U45
 Q5 - MPS-U95
- { COMPLEMENTARY
 { DARLINGTONS



MOTOROLA

MPS - U51 MPS - U51A

PNP SILICON ANNULAR TRANSISTORS

... designed for complementary symmetry audio circuits to 5 Watts output.

- Excellent Current Gain Linearity – 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.7 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Adc}$
- Complements to NPN MPS-U01 and MPS-U01A
- Uniwatt Package for Excellent Thermal Properties –
1.0 Watt @ $T_A = 25^\circ\text{C}$

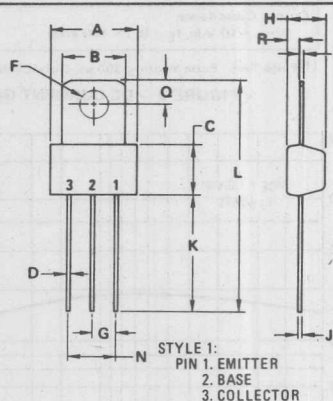
MAXIMUM RATINGS

Rating	Symbol	MPS-U51	MPS-U51A	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Base Voltage	V_{CB}	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	2.0		Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0	8.0	Watt mW/°C
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10	80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

PNP SILICON AUDIO TRANSISTORS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MPS-U51,MPS-U51A

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 1.0\text{ mA}$, $I_B = 0$)	BV_{CEO}	30 40	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100\text{ }\mu\text{A}$, $I_E = 0$)	BV_{CBO}	40 50	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100\text{ }\mu\text{A}$, $I_C = 0$)	BV_{EBO}	5.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 30\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 40\text{ Vdc}$, $I_E = 0$)	I_{CBO}	— —	0.1 0.1	μA
Emitter Cutoff Current ($V_{BE} = 3.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	0.1	μA
ON CHARACTERISTICS(1)				
DC Current Gain ($I_C = 10\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 100\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 1.0\text{ A}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	55 60 50	—	—
Collector-Emitter Saturation Voltage ($I_C = 1.0\text{ A}$, $I_B = 0.1\text{ A}$)	$V_{CE(sat)}$	—	0.7	Vdc
Base-Emitter On Voltage ($I_C = 1.0\text{ A}$, $V_{CE} = 1.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product ($I_C = 50\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f = 20\text{ MHz}$)	f_T	50	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 100\text{ kHz}$)	C_{ob}	—	30	pF

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 1 — DC CURRENT GAIN

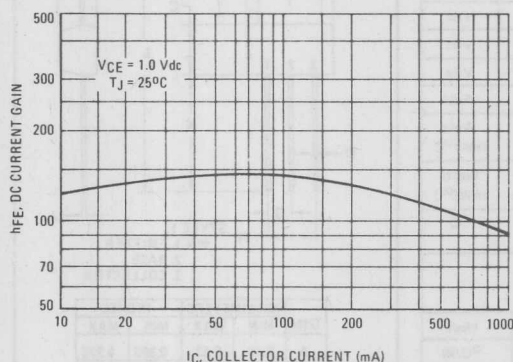


FIGURE 2 — "ON" VOLTAGES

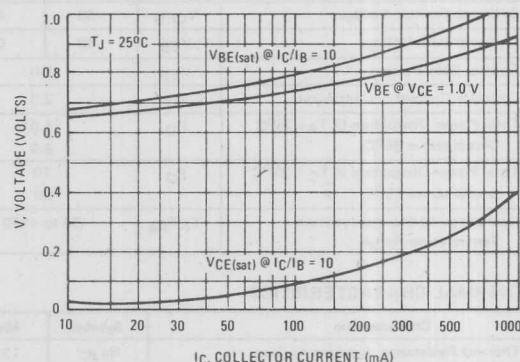
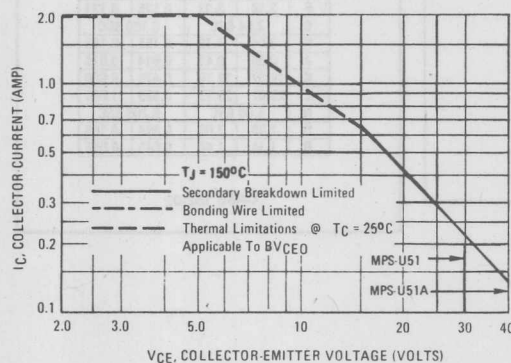


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



MOTOROLA

MPS - U55

MPS - U56

PNP SILICON ANNULAR AMPLIFIER TRANSISTORS

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage –
 $V_{CE0} = 60 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc} - \text{MPS-U55}$
 $80 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc} - \text{MPS-U56}$
- High Power Dissipation – $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complements to NPN MPS-U05 and MPS-U06

PNP SILICON AMPLIFIER TRANSISTORS

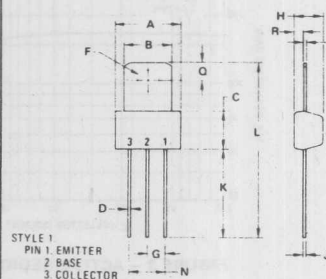


MAXIMUM RATINGS

Rating	Symbol	MPS-U55	MPS-U56	Unit
Collector-Emitter Voltage	V_{CE0}	80	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	2.0		A dc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.0	8.0	Watt mW/°C
Derate above 25°C		8.0		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	10	80	Watts mW/°C
Derate above 25°C				
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.19	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
M	5.08 BSC		0.200 BSC	
Q	2.29	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

Collector Connected
to Tab
CASE 152-02

MPS-U55, MPS-U56

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0\text{ mAdc}$, $I_B = 0$)	BV_{CEO}	60 80	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100\text{ }\mu\text{Adc}$, $I_C = 0$)	BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 40\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 60\text{ Vdc}$, $I_E = 0$)	I_{CBO}	— —	— —	100 100	nAdc
ON CHARACTERISTICS					
DC Current Gain (1) ($I_C = 50\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 250\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 500\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	80 50 —	160 130 80	— — —	—
Collector-Emitter Saturation Voltage(1) ($I_C = 250\text{ mAdc}$, $I_B = 10\text{ mAdc}$) ($I_C = 250\text{ mAdc}$, $I_B = 25\text{ mAdc}$)	$V_{CE(sat)}$	— —	0.22 0.15	0.5 —	Vdc
Base-Emitter On Voltage (1) ($I_C = 250\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$)	$V_{BE(on)}$	—	0.78	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain-Bandwidth Product (1) ($I_C = 250\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$, $f = 100\text{ MHz}$)	f_T	50	100	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 100\text{ kHz}$)	C_{ob}	—	10	15	pF

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 1 — DC CURRENT GAIN

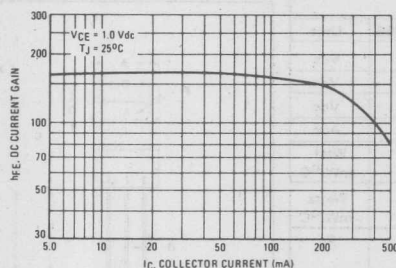


FIGURE 2 — "ON" VOLTAGES

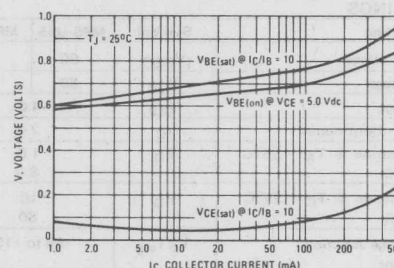


FIGURE 3 — ACTIVE-REGION SAFE OPERATING AREA

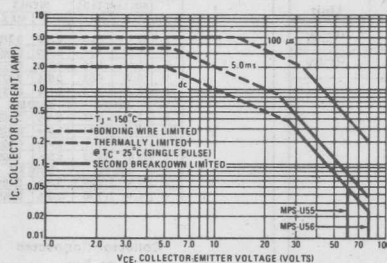
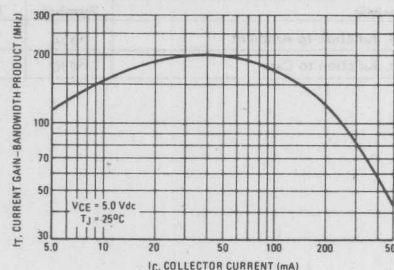


FIGURE 4 — CURRENT-GAIN-BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**PNP SILICON ANNULAR
AMPLIFIER TRANSISTOR**

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
 $V_{CEO} = 100 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc}$
- High Power Dissipation — $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complement to NPN MPS-U07

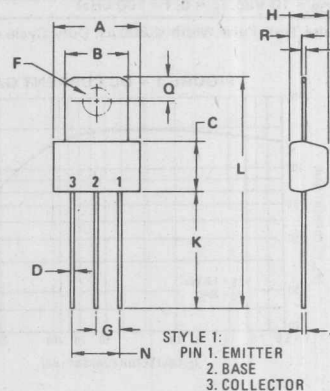
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^\circ\text{C/W}$

**AMPLIFIER TRANSISTOR
PNP SILICON**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0\text{ mAdc}$, $I_B = 0$)	BV_{CEO}	100	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_C = 100\text{ }\mu\text{Adc}$, $I_E = 0$)	BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 40\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	—	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 50\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 250\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 500\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	60 30 —	140 65 30	— — —	—
Collector-Emitter Saturation Voltage ($I_C = 250\text{ mAdc}$, $I_B = 10\text{ mAdc}$) ($I_C = 250\text{ mAdc}$, $I_B = 25\text{ mAdc}$)	$V_{CE(sat)}$	— —	0.24 0.15	0.5 —	Vdc
Base-Emitter On Voltage ($I_C = 250\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$)	$V_{BE(on)}$	—	0.78	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain-Bandwidth Product (1) ($I_C = 250\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$, $f = 100\text{ MHz}$)	f_T	50	100	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 100\text{ kHz}$)	C_{ob}	—	10	15	pF

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 1 — DC CURRENT GAIN

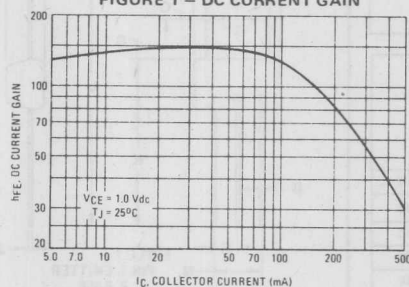


FIGURE 2 — "ON" VOLTAGES

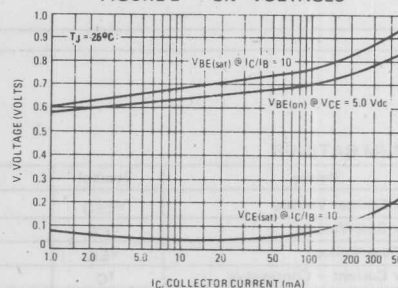


FIGURE 3 — DC SAFE OPERATING AREA

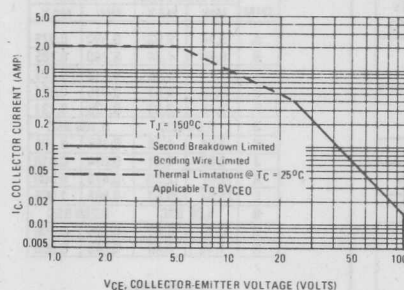
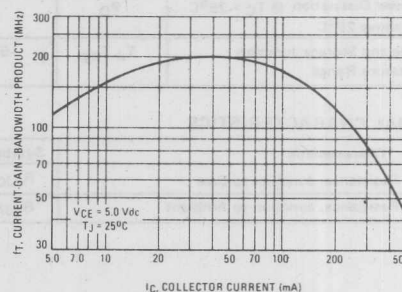


FIGURE 4 — CURRENT-GAIN-BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**PNP SILICON DARLINGTON
AMPLIFIER TRANSISTOR**

... designed for amplifier and driver applications.

- High DC Current Gain –
 $h_{FE} = 25,000$ (Min) @ $I_C = 200$ mAdc
 $15,000$ (Min) @ $I_C = 500$ mAdc
- Collector-Emitter Breakdown Voltage –
 $BV_{CES} = 40$ Vdc (Min) @ $I_C = 100$ μ Adc
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.5$ Vdc @ $I_C = 1.0$ Adc
- Monolithic Construction for High Reliability
- Complement to NPN MPS-U45

**PNP SILICON
DARLINGTON
TRANSISTOR**



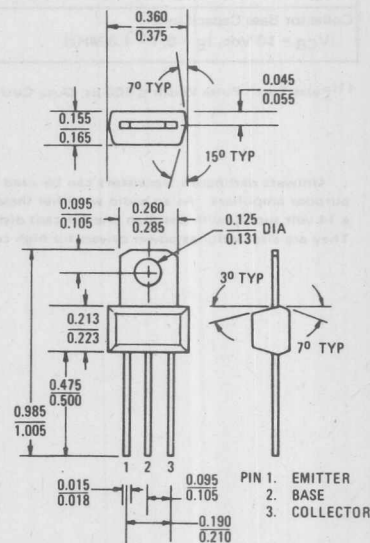
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(1)}$	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	12	Vdc
Collector Current	I_C	2.0	Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	125	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	θ_{JC}	12.5	$^\circ\text{C/W}$

(1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical. BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by noise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.



Collector connected to tab
To convert inches to millimeters multiply by 25.4

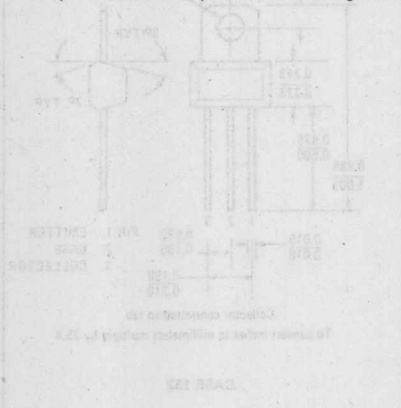
CASE 152

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = 100\ \mu\text{Adc}$, $V_{BE} = 0$)	BV_{CES}	40	—	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100\ \mu\text{Adc}$, $I_E = 0$)	BV_{CBO}	50	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\ \mu\text{Adc}$, $I_C = 0$)	BV_{EBO}	10	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 30\ \text{Vdc}$, $I_E = 0$)	I_{CBO}	—	—	100	nAdc
Emitter Cutoff Current ($V_{EB} = 8.0\ \text{Vdc}$, $I_C = 0$)	I_{EBO}	—	—	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain ($I_C = 200\ \text{mAdc}$, $V_{CE} = 5.0\ \text{Vdc}$) ($I_C = 500\ \text{mAdc}$, $V_{CE} = 5.0\ \text{Vdc}$) ($I_C = 1.0\ \text{Adc}$, $V_{CE} = 5.0\ \text{Vdc}$)	h_{FE}	25,000 15,000 4,000	65,000 35,000 12,000	150,000 — —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0\ \text{Adc}$, $I_B = 2.0\ \text{mAdc}$)	$V_{CE(sat)}$	—	1.2	1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0\ \text{Adc}$, $I_B = 2.0\ \text{mAdc}$)	$V_{BE(sat)}$	—	1.85	2.0	Vdc
Base-Emitter On Voltage ($I_C = 1.0\ \text{Adc}$, $V_{CE} = 5.0\ \text{Vdc}$)	$V_{BE(on)}$	—	1.7	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 200\ \text{mAdc}$, $V_{CE} = 5.0\ \text{Vdc}$, $f = 100\ \text{MHz}$)	$ h_{fe} $	0.5	3.2	—	—
Collector Base Capacitance ($V_{CB} = 10\ \text{Vdc}$, $I_E = 0$, $f = 1.0\ \text{MHz}$)	C_{cb}	—	2.5	12	pF

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Uniwatt darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one per cent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also useful as power drivers for high current application such as voltage regulators.



Characteristic	Symbol	Min	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	—	—	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	—	$^\circ\text{C/W}$

FIGURE 1 - DC CURRENT GAIN

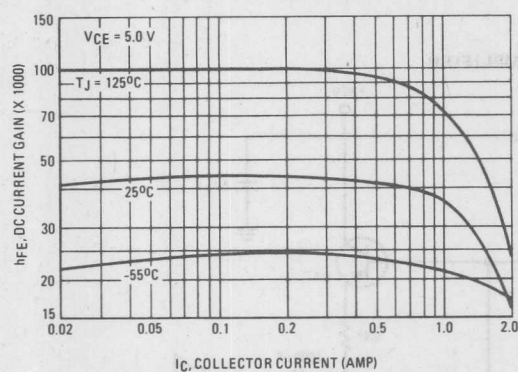


FIGURE 2 - SMALL-SIGNAL CURRENT GAIN

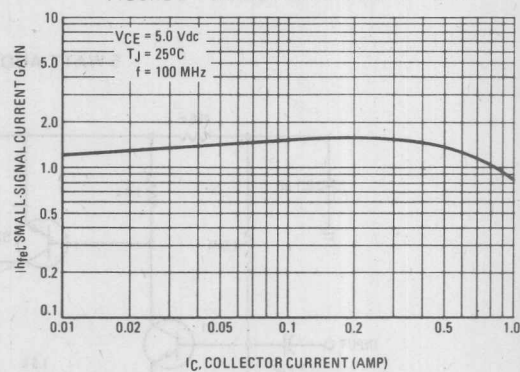


FIGURE 3 - "ON" VOLTAGES

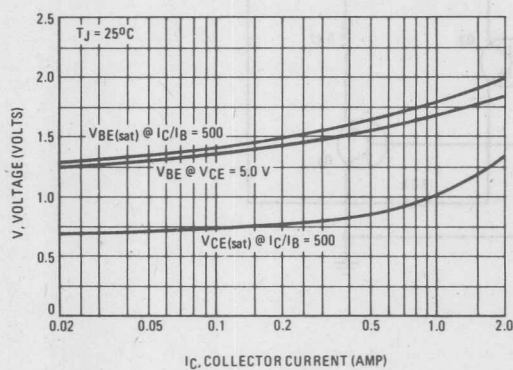


FIGURE 4 - TEMPERATURE COEFFICIENT

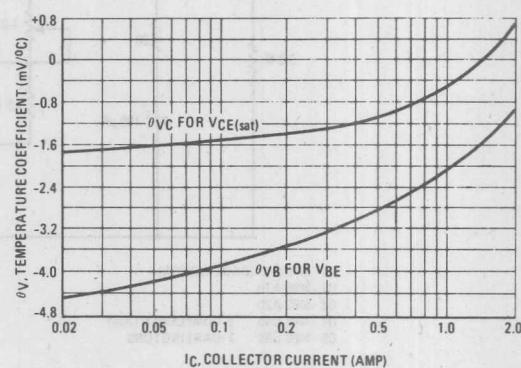
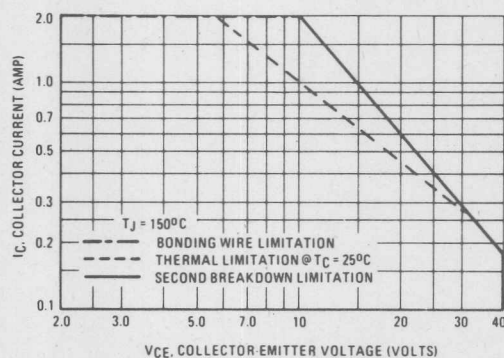


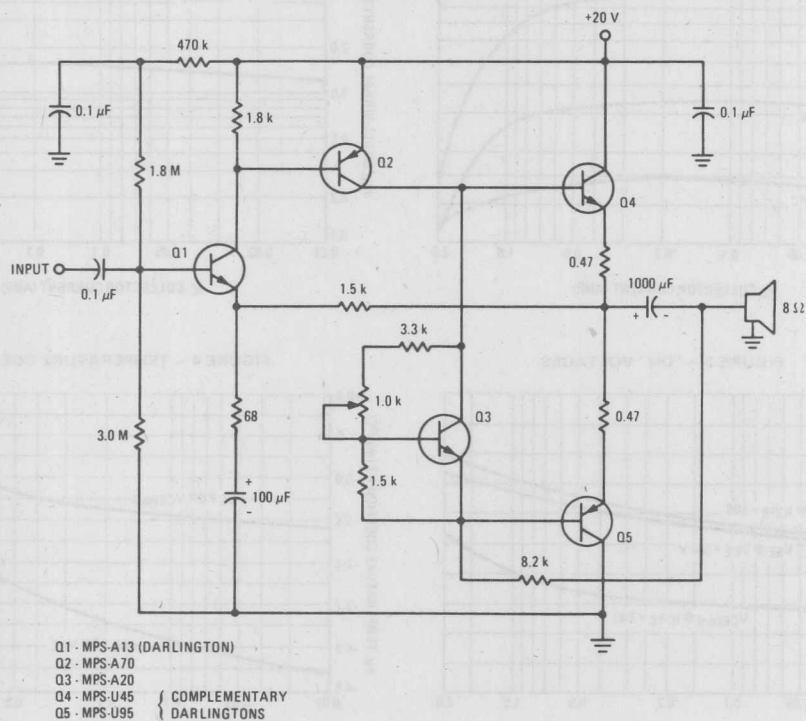
FIGURE 5 - DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

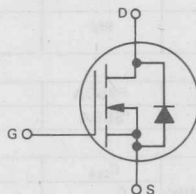
5-WATT AUDIO AMPLIFIER



**MOTOROLA****MTM1N95, MTM1N100
MTP1N95, MTP1N100****Designer's Data Sheet****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, and converters or high voltage linear applications such as high voltage power supplies.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)

**MAXIMUM RATINGS**

Rating	Symbol	MTM1N95 MTP1N95	MTM1N100 MTP1N100	Unit
Drain — Source Voltage	V_{DSS}	950	1000	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0$ m Ω)	V_{DGR}	950	1000	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	1.0		Adc
Pulsed	I_{DM}	6.0		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6		Watts W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

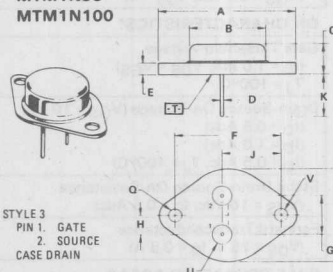
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

1 AMPERE**N-CHANNEL TMOS
POWER FET**

$r_{DS(on)} = 10$ OHMS
950 and 1000 VOLTS

**MTM1N95
MTM1N100**

STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

**CASE 1-05
TO-3 TYPE**

DIM	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.45 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	26.81	—	1.050
N	4.83	5.33	0.190	0.210
P	3.81	4.19	0.150	0.165

NOTES:

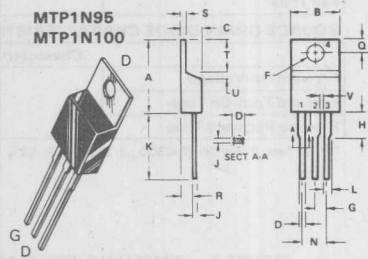
- DIMENSIONS Q AND V ARE DATUMS.
- IS SEATING PLANE AND DATUM.
- POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.

± 0.13 (0.005) T V ± 0.13 (0.005) T V ± 0.13 (0.005) T V

FOR LEADS:

± 0.13 (0.005) T V ± 0.13 (0.005) T V ± 0.13 (0.005) T V

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

**MTP1N95
MTP1N100**

STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.85	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
E	3.61	3.73	0.142	0.147
F	2.41	2.87	0.095	0.105
G	2.79	3.30	0.110	0.130
H	0.36	0.56	0.014	0.022
J	12.70	14.27	0.500	0.562
K	1.14	1.27	0.045	0.050
L	4.83	5.33	0.190	0.210
M	2.54	3.04	0.100	0.120
N	2.04	2.79	0.080	0.110
O	1.14	1.39	0.045	0.055
P	5.97	6.48	0.235	0.255
Q	0.76	1.27	0.030	0.050
R	1.14	—	0.045	—

**CASE 221A-02
TO-220AB**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	950 1000	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 0.5$ Adc) ($I_D = 1.0$ Adc) ($I_D = 0.5$ Adc, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	5.0 12 10	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 0.5$ Adc)	$r_{DS(on)}$	—	10	Ohms
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 0.5$ A)	g_{fs}	0.5	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	$(V_{DS} = 125$ V, $I_D = 0.5$ A, $R_{gen} = 50$ ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage	V_{SD}	1.0	Vdc
Forward Turn-On Time	t_{on}	250	ns
Reverse Recovery Time	t_{rr}	420	ns

*Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle $\leq 2\%$.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

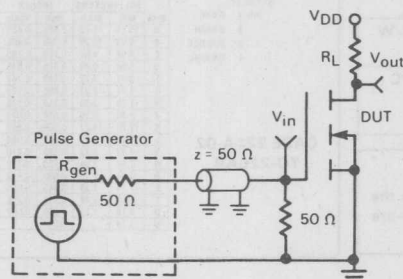


FIGURE 2 — SWITCHING WAVEFORMS

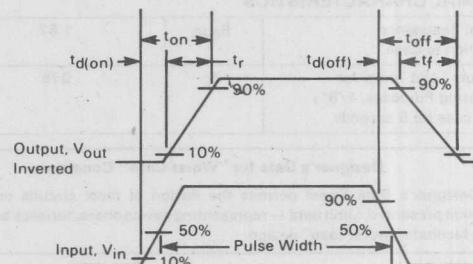


FIGURE 3 — OUTPUT CHARACTERISTICS

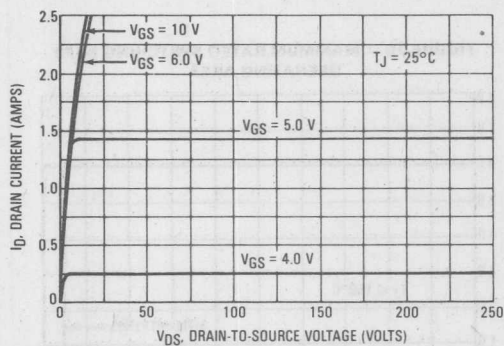


FIGURE 4 — ON-REGION CHARACTERISTICS

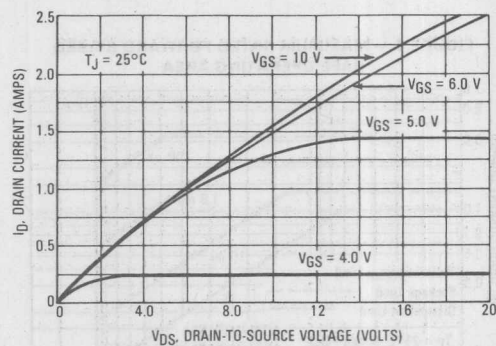


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

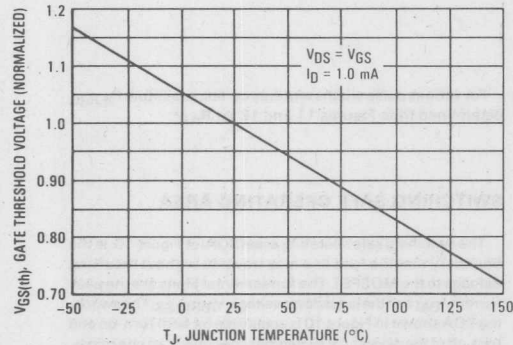


FIGURE 6 — TRANSFER CHARACTERISTICS

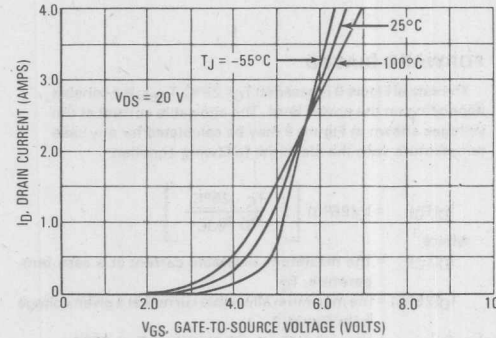


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

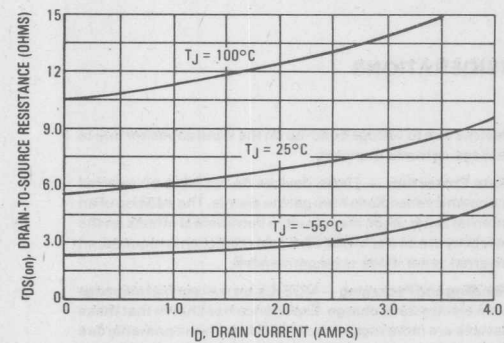
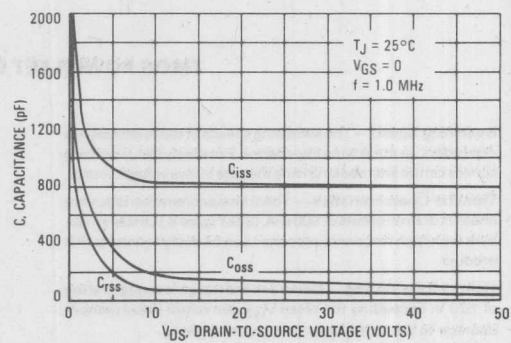
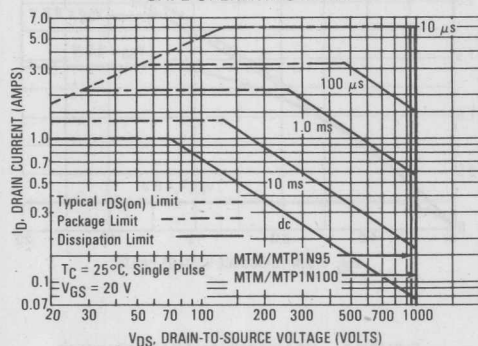


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

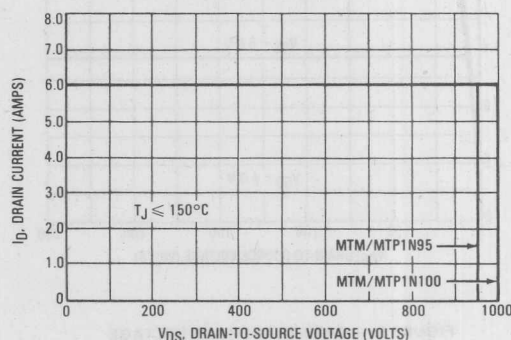
$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



For various pulse widths and duty cycles, substitute $R_{\theta JC}(t)$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{BR}DSS$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

THERMAL RESPONSE

FIGURE 11 — MTM1N95/MTM1N100

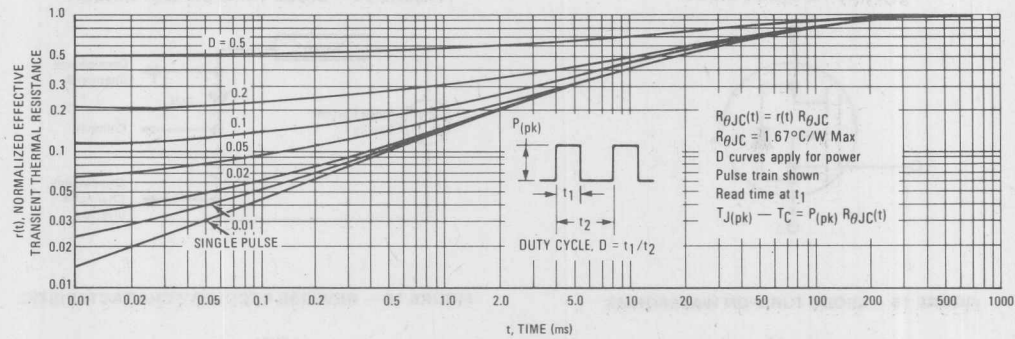
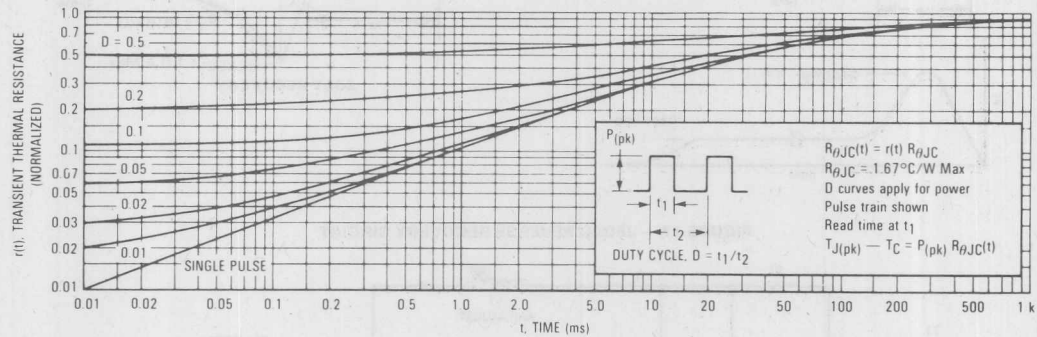


FIGURE 12 — MTP1N95/MTP1N100



TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This

diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 13 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

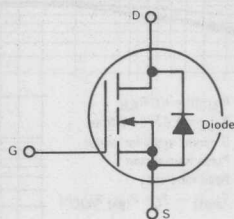


FIGURE 14 — DIODE TURN-ON TEST CIRCUIT

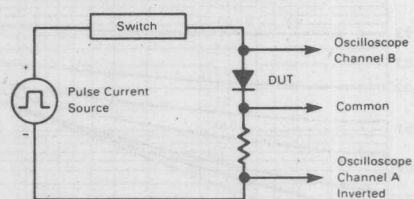


FIGURE 15 — DIODE TURN-ON WAVEFORMS

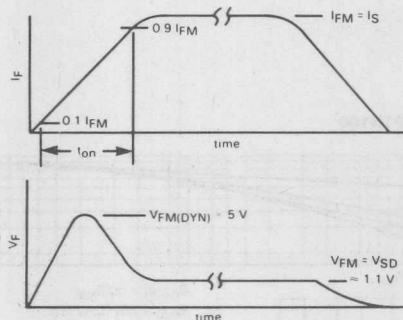


FIGURE 16 — REVERSE RECOVERY CHARACTERISTIC

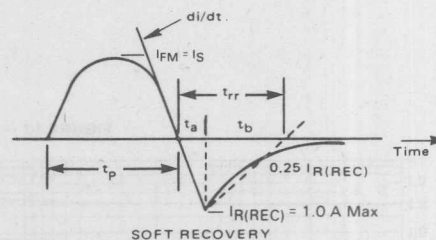
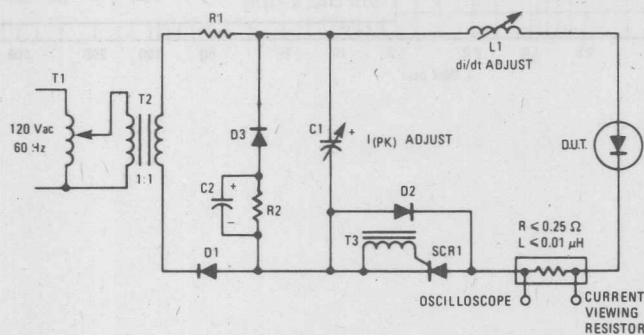


FIGURE 17 — JEDEC REVERSE RECOVERY CIRCUIT



- R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μ F
C2 \approx 4000 μ F
L1 = 1.0 - 27 μ H
T1 = Variac Adjusts (pK) and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)



MOTOROLA

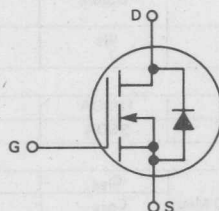
MTM2N45, MTM2N50 MTP2N45, MTP2N50

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)



MAXIMUM RATINGS

Rating	Symbol	MTM2N45 MTP2N45	MTM2N50 MTP2N50	Unit
Drain — Source Voltage	V_{DSS}	450	500	Vdc
Drain — Gate Voltage $R_{GS} = 1\text{ M}\Omega$	V_{DGR}	450	500	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	2.0		Adc
Pulsed	I_{DM}	7.0		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

2 AMPERE

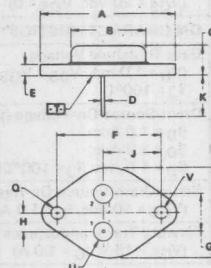
N-CHANNEL TMOS POWER FET

$r_{DS(on)} = 4.0\text{ OHMS}$
450 and 500 VOLTS

MTM2N45 MTM2N50



STYLE 3
PIN 1 GATE
2 SOURCE
CASE DRAIN



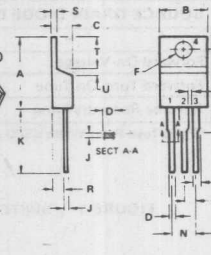
CASE 1-05 TO-3 TYPE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	0.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	26.67	—	1.050	—
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

MTP2N45 MTP2N50



STYLE 5
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN



CASE 221A-02 TO-220AB

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.54	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	7.79	8.30	0.307	0.327
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.38	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	450 500	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 1.0$ Adc) ($I_D = 2.0$ Adc) ($I_D = 1.0$ Adc, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	4.0 10 8.0	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 1.0$ Adc)	$r_{DS(on)}$	—	4.0	Ohms
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 1.0$ A)	g_{fs}	1.0	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	100	pF
Reverse Transfer Capacitance		C_{rss}	—	50	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DS} = 125$ V, $I_D = 1.0$ A, $R_{gen} = 50$ ohms)	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	60	ns
Turn-Off Delay Time		$t_{d(off)}$	—	60	ns
Fall Time		t_f	—	30	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage	V_{SD}	1.0	Vdc
Forward Turn-On Time	t_{on}	150	ns
Reverse Recovery Time	t_{rr}	200	ns

*Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 SWITCHING TEST CIRCUIT

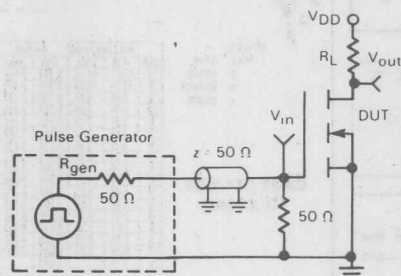
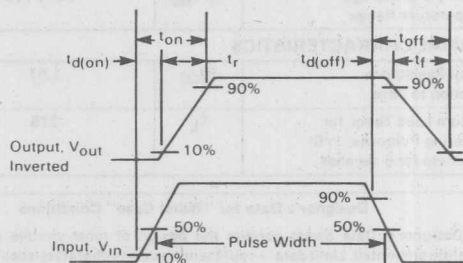


FIGURE 2 - SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 OUTPUT CHARACTERISTICS

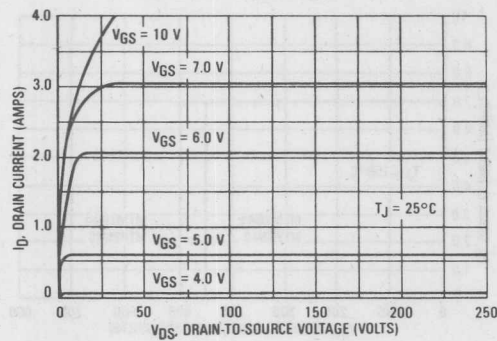


FIGURE 4 — ON-CHARACTERISTICS

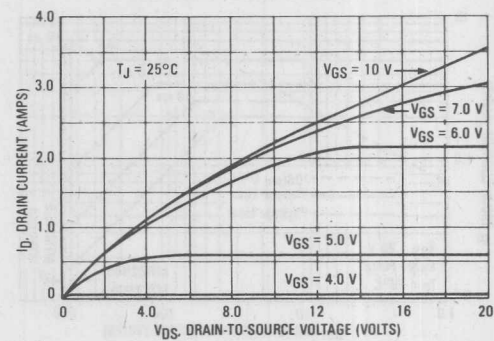


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

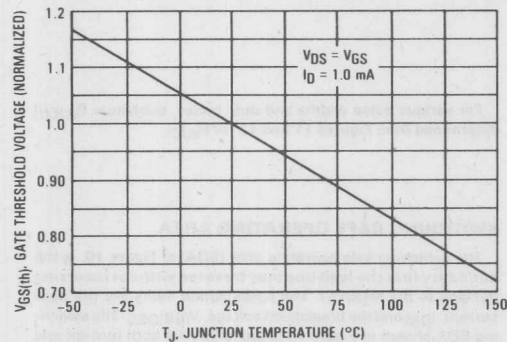


FIGURE 6 — TRANSFER CHARACTERISTICS

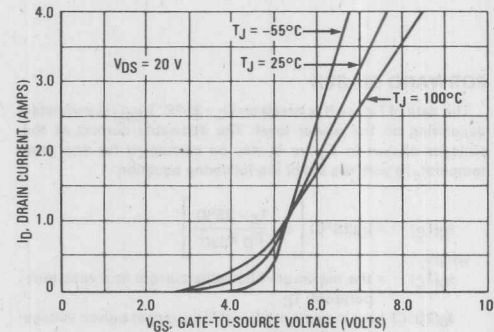


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

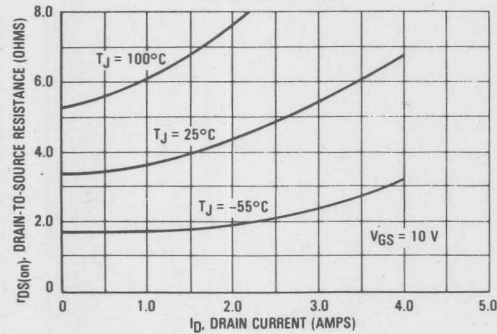
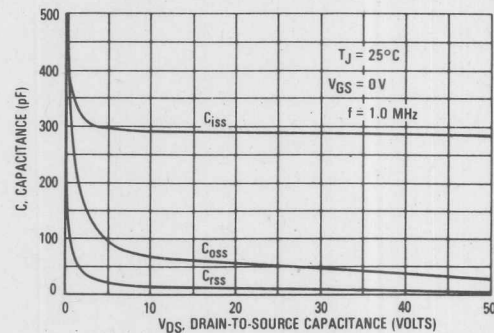


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

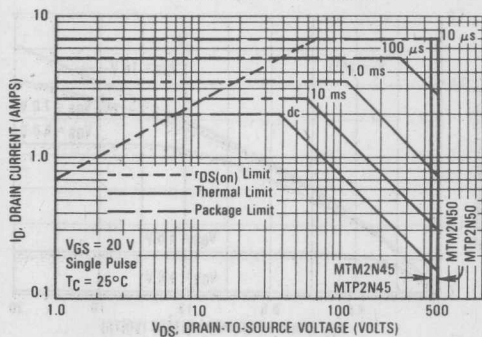
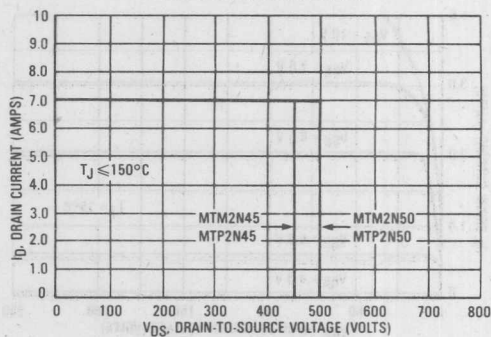


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance.

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

FIGURE 11 — MTM2N45/MTM2N50

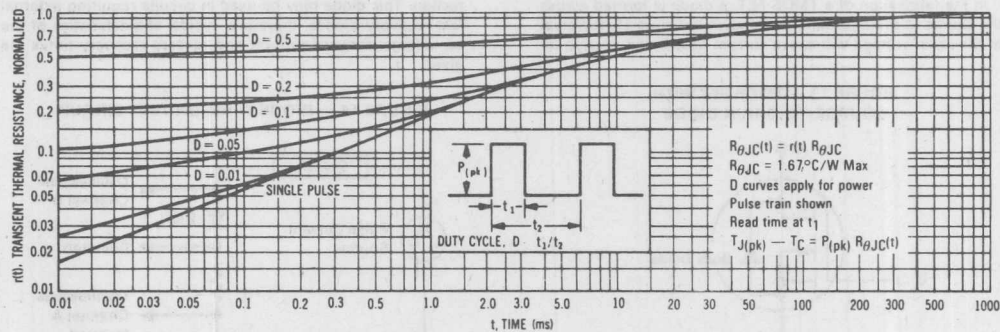
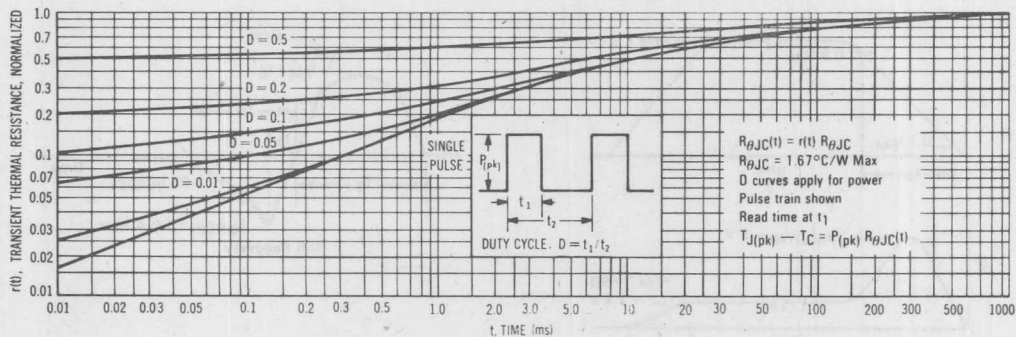


FIGURE 12 — MTP2N45/MTP2N50



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse di-

FIGURE 13 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

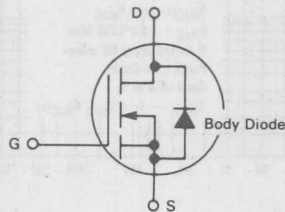
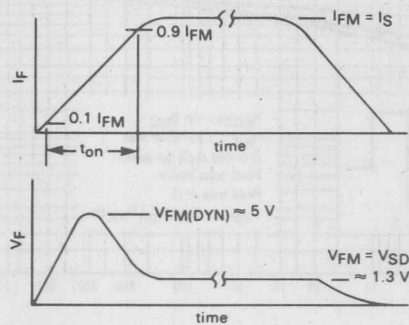


FIGURE 15 — DIODE TURN-ON WAVEFORMS



rection. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 14 — DIODE TURN-ON TEST CIRCUIT

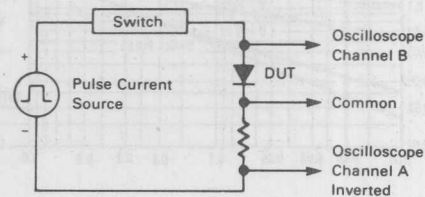


FIGURE 16 — REVERSE RECOVERY CHARACTERISTIC

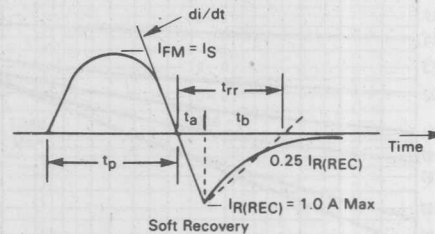
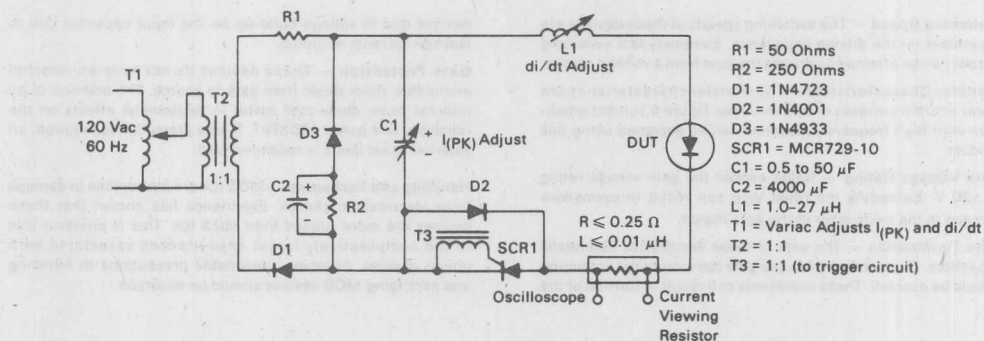


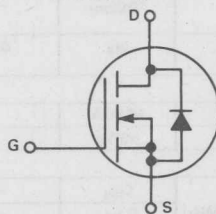
FIGURE 17 — JEDEC REVERSE RECOVERY CIRCUIT



**MOTOROLA****MTM2N85, MTM2N90
MTP2N85, MTP2N90****Designer's Data Sheet****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, high voltage power supplies and grid drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)

**MAXIMUM RATINGS**

Rating	Symbol	MTM2N85 MTP2N85	MTM2N90 MTP2N90	Unit
Drain — Source Voltage	V_{DSS}	850	900	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0$ mΩ)	V_{DGR}	850	900	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	2.0		Adc
Pulsed	I_{DM}	7.0		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

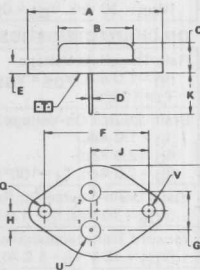
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

2.0 AMPERE**N-CHANNEL TMOS
POWER FET**

$r_{DS(on)} = 8.0$ OHMS
850 and 900 VOLTS

**MTM2N85
MTM2N90**

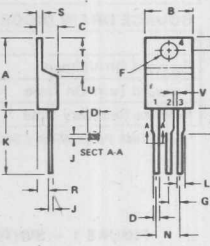
STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

**CASE 1-05
TO-3 TYPE**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.68	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.48 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	28.67	—	1.090
N	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

**MTP2N85
MTP2N90**

STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

**CASE 221A-02
TO-220AB**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	8.85	10.29	0.380	0.405
C	4.86	4.82	0.190	0.190
D	0.64	0.89	0.025	0.035
E	3.51	3.73	0.142	0.147
F	2.41	2.67	0.095	0.105
G	2.79	3.30	0.110	0.130
H	0.36	0.56	0.014	0.022
J	12.70	14.27	0.500	0.562
K	1.14	1.27	0.045	0.050
L	4.83	5.33	0.190	0.210
M	2.54	3.04	0.100	0.120
N	2.04	2.79	0.080	0.110
O	1.14	1.39	0.045	0.055
P	5.97	6.48	0.235	0.255
Q	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	850 900	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 1.0$ Adc) ($I_D = 2.0$ Adc) ($I_D = 1.0$ Adc, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	8.0 20 16	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 1.0$ Adc)	$r_{DS(on)}$	—	8.0	Ohms
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 1.0$ A)	g_{fs}	0.5	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DS} = 125$ V, $I_D = 1.0$ A, $R_{gen} = 50$ ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage $I_S = 2.0$ A	V_{SD}	1.0	Vdc
Forward Turn-On Time $V_{GS} = 0$	t_{on}	250	ns
Reverse Recovery Time See Figures 15 and 16	t_{rr}	420	ns

*Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

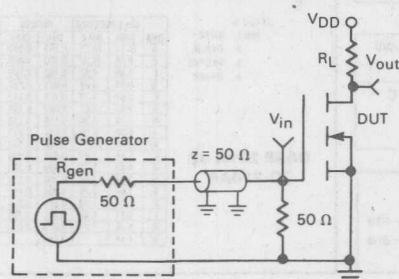
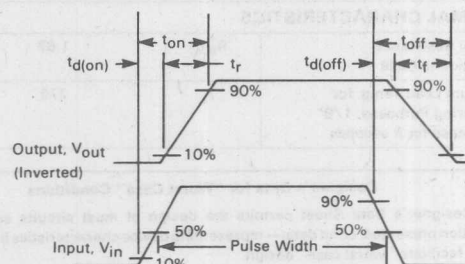


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

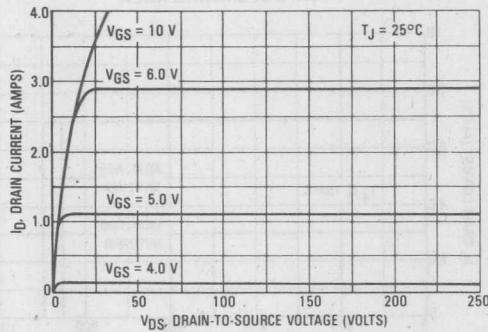


FIGURE 4 — ON-REGION CHARACTERISTICS

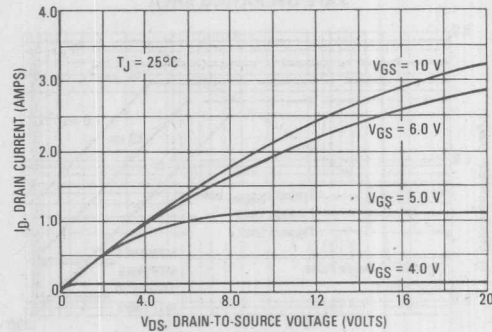


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

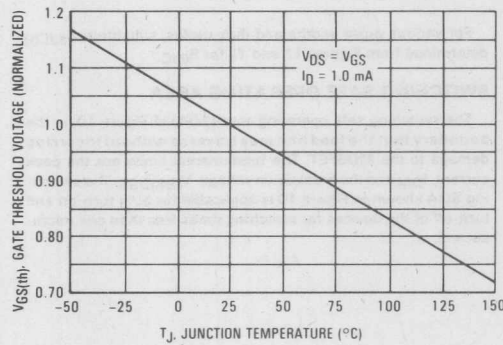


FIGURE 6 — TRANSFER CHARACTERISTICS

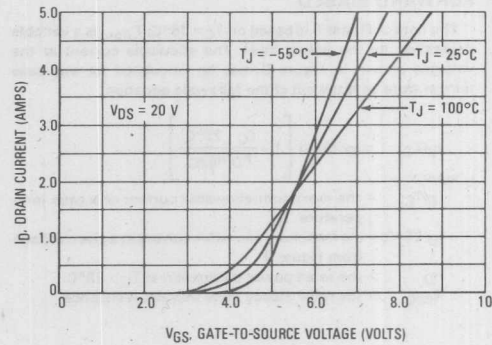


FIGURE 7 — ON RESISTANCE versus DRAIN CURRENT

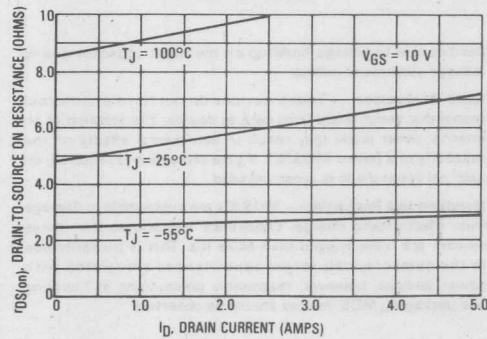
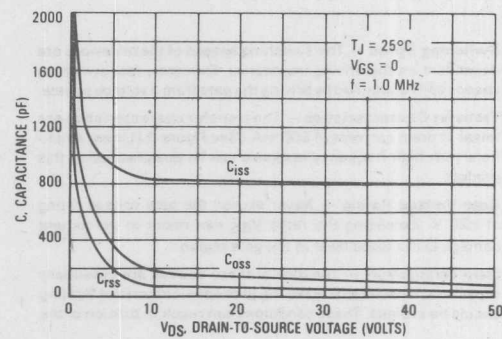
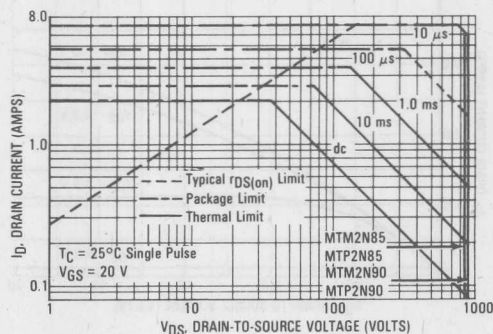


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

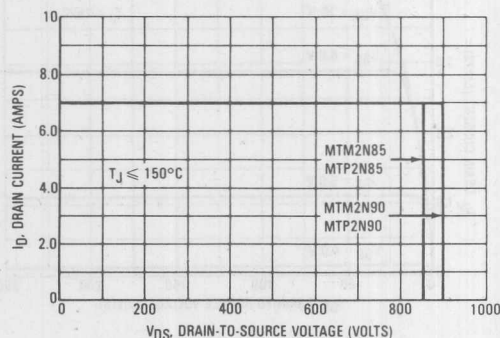
$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



For various pulse widths and duty cycles, substitute $R_{\theta JC}(t)$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

THERMAL RESPONSE

FIGURE 11 — MTM2N85/MTM2N90

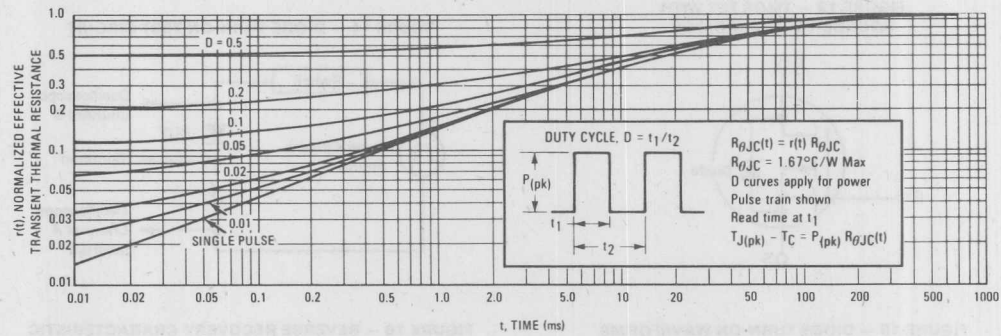
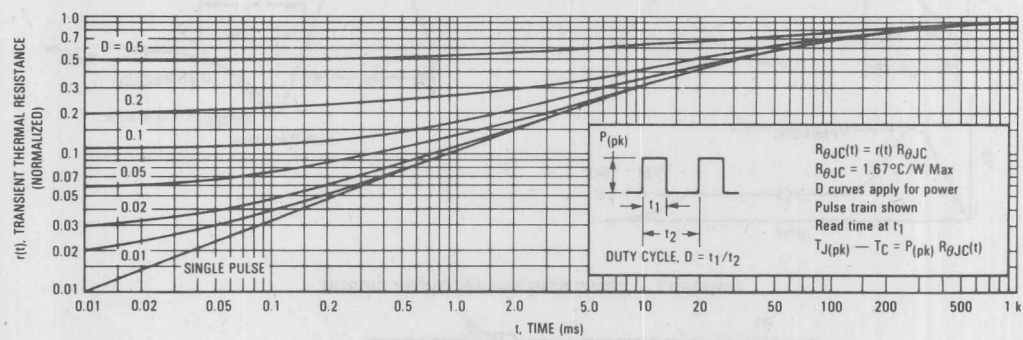


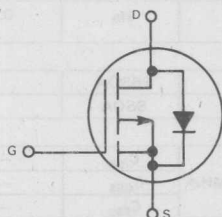
FIGURE 12 — MTP2N85/MTP2N90



**MOTOROLA****MTM2P45, MTM2P50
MTP2P45, MTP2P50****Designer's Data Sheet****P-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.0$ Volts (max)

**MAXIMUM RATINGS**

Rating	Symbol	MTM2P45 MTP2P45	MTM2P50 MTP2P50	Unit
Drain — Source Voltage	V_{DSS}	450	500	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0$ M Ω)	V_{DGR}	450	500	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	2.0		Adc
Pulsed	I_{DM}	8.0		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75		Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

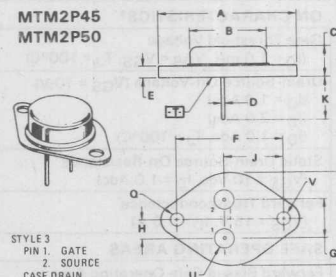
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C/W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

2 AMPERE**P-CHANNEL TMOS
POWER FET**

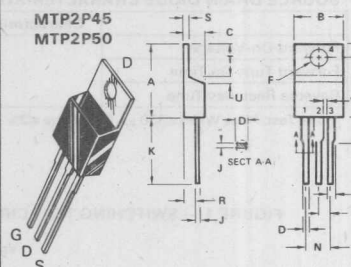
$r_{DS(on)} = 6.0$ OHMS
450 and 500 VOLTS

**MTM2P45
MTM2P50**

STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

**CASE 1-05
TO-3 TYPE**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

**MTP2P45
MTP2P50**

STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

**CASE 221A-02
TO-220AB**

DIM	MILLIMETERS			INCHES		
	MIN	MAX		MIN	MAX	
A	15.11	15.75		0.595	0.620	
B	9.65	10.29		0.380	0.405	
C	4.06	4.82		0.160	0.190	
D	0.64	0.89		0.025	0.035	
F	3.61	3.73		0.142	0.147	
G	2.41	2.67		0.095	0.105	
H	2.79	3.30		0.110	0.130	
J	0.38	0.56		0.014	0.022	
K	12.70	14.27		0.500	0.562	
L	1.14	1.27		0.045	0.050	
N	4.83	5.33		0.190	0.210	
Q	2.54	3.04		0.100	0.120	
R	2.04	2.79		0.080	0.110	
S	1.14	1.39		0.045	0.055	
T	5.97	6.48		0.235	0.255	
U	0.76	1.27		0.030	0.050	
V	1.14			0.045		

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0\text{ mA}$)	$V_{(BR)DSS}$	450 500	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85\text{ BV}_{DSS}$, $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0\text{ mA}$, $V_{DS} = V_{GS}$, $T_J = 100^\circ\text{C}$)	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 1.0\text{ Adc}$) ($I_D = 2.0\text{ Adc}$) ($I_D = 1.0\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	—	6.0 12.5 12.0	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.0\text{ Adc}$)	$r_{DS(on)}$	—	6.0	Ohms
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 1.0\text{ A}$)	g_{fs}	0.5	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	(VDS = 25 V, VGS = 0, f = 1.0 MHz)	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	200	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	(VDS = 125 V, $I_D = 1.0\text{ A}$, $R_{gen} = 50\text{ ohms}$)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	100	ns
Turn-Off Delay Time		$t_{d(off)}$	—	150	ns
Fall Time		t_f	—	50	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage ($I_S = 2.0\text{ A}$)	V_{SD}	1.8	Vdc
Forward Turn-On Time ($V_{GS} = 0$)	t_{on}	50	ns
Reverse Recovery Time (See Figures 15 and 16)	t_{rr}	120	ns

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

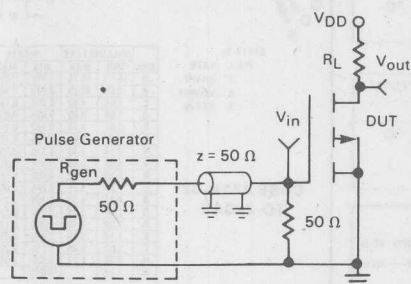
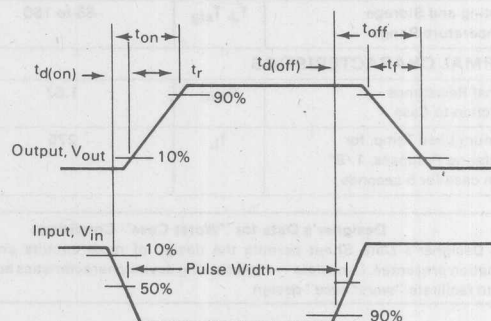
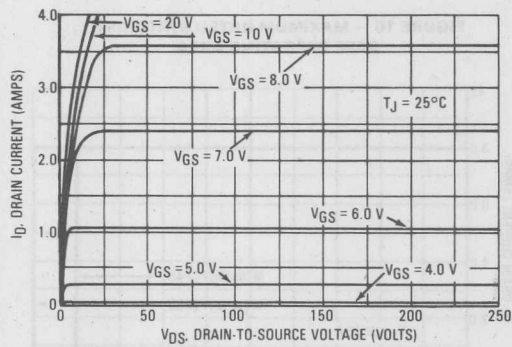
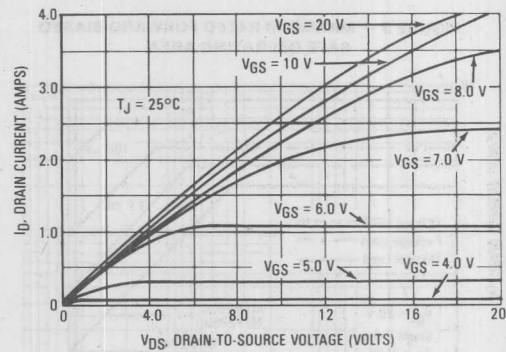
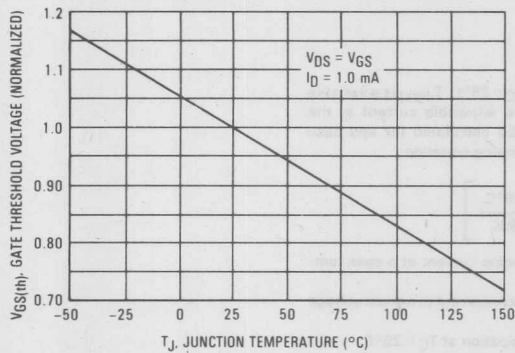
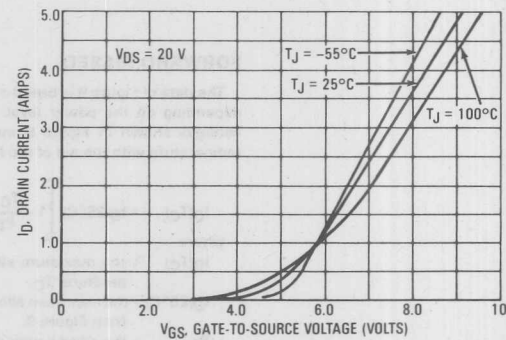
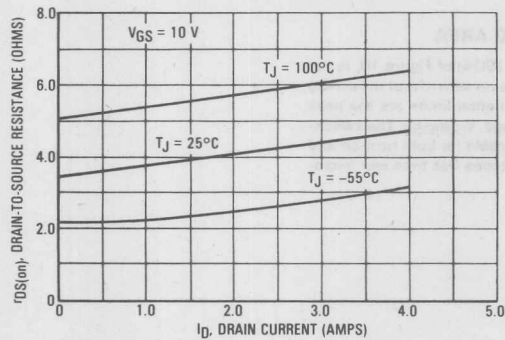
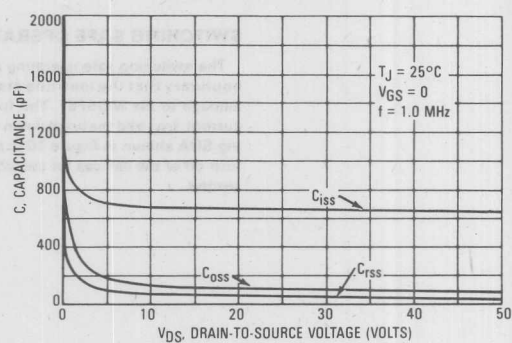


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

FIGURE 4 — ON-CHARACTERISTICS

FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

FIGURE 6 — TRANSFER CHARACTERISTICS

FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

FIGURE 8 — CAPACITANCE VARIATION


SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

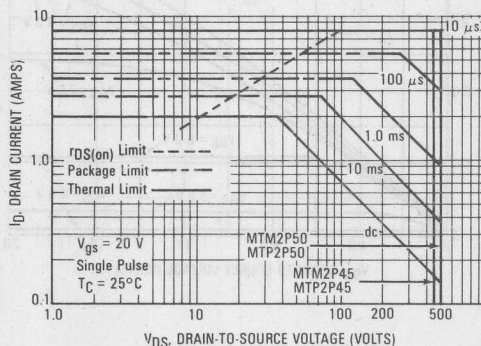
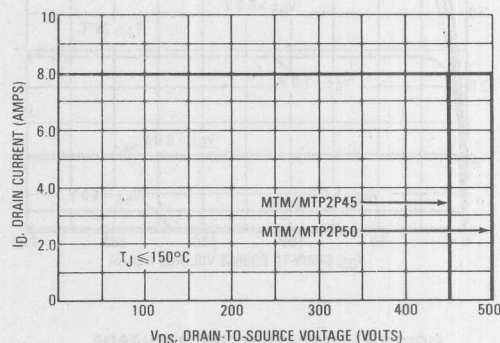


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC}(t)$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

THERMAL RESPONSE

FIGURE 11 — MTM2P45/MTM2P50

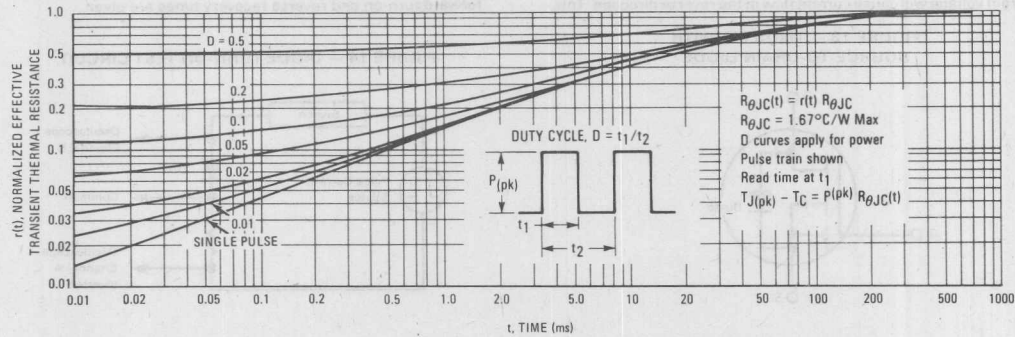
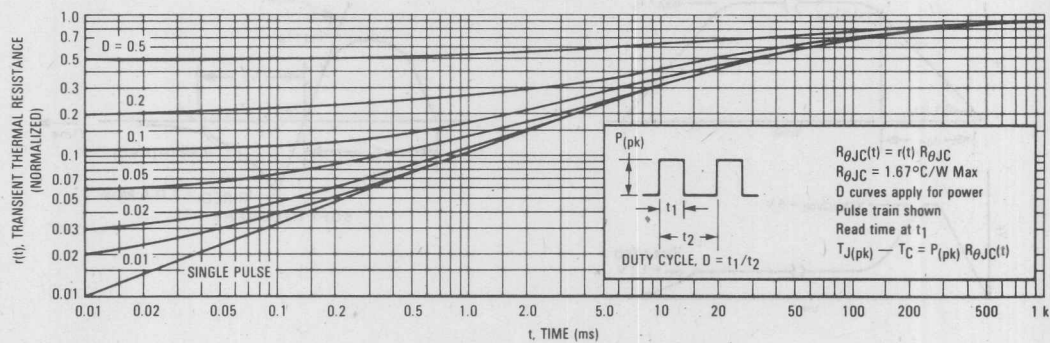


FIGURE 12 — MTP2P45/MTP2P50



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 13. Reversal of the drain voltage will cause current flow in the reverse direction. This

diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 13 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

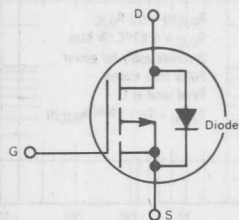


FIGURE 14 — DIODE TURN-ON TEST CIRCUIT

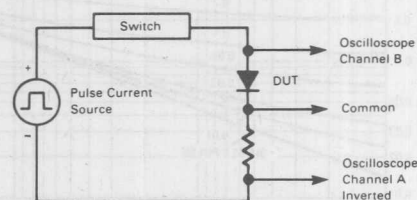


FIGURE 15 — BODY DIODE TURN-ON WAVEFORMS

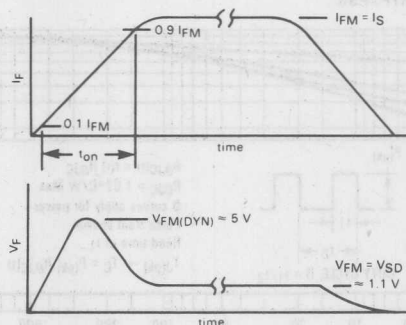


FIGURE 16 — REVERSE RECOVERY CHARACTERISTIC

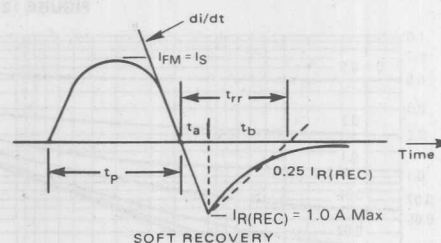
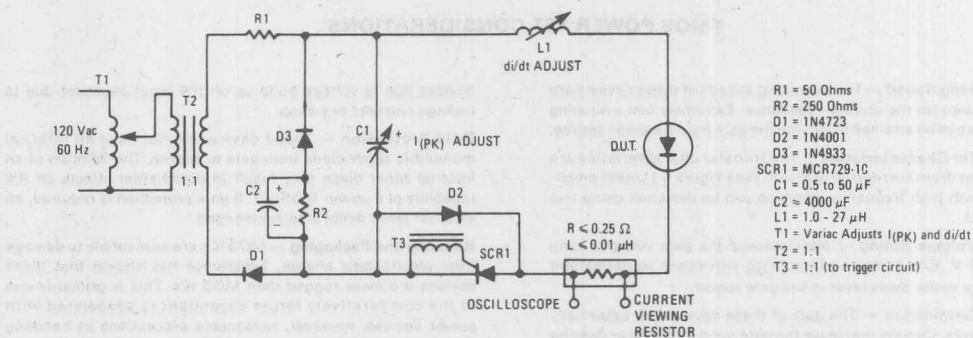


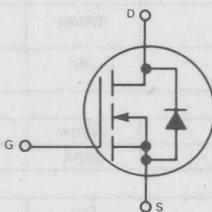
FIGURE 17 — JEDEC REVERSE RECOVERY CIRCUIT



**MOTOROLA****MTM3N35, MTM3N40
MTP3N35, MTP3N40****Designer's Data Sheet****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)

**MAXIMUM RATINGS**

Rating	Symbol	MTM3N3 MTP3N35	MTM3N40 MTP3N40	Unit
Drain — Source Voltage	V_{DSS}	350	400	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0$ M Ω)	V_{DGR}	350	400	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	3.0		Adc
Pulsed	I_{DM}	8.0		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

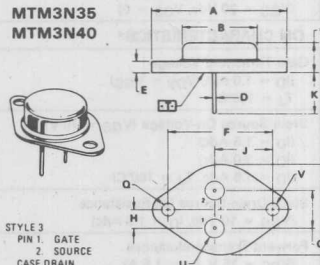
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

3 AMPERE**N-CHANNEL TMOS
POWER FET**

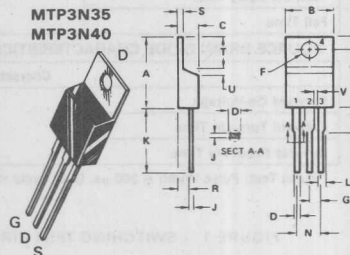
$r_{DS(on)} = 3.3$ OHMS
350 and 400 VOLTS

**MTM3N35
MTM3N40**

STYLE 3
PIN 1 GATE
PIN 2 SOURCE
CASE DRAIN

USE CASE 1-05
TO-3 TYPE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.08	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

**MTP3N35
MTP3N40**

STYLE 5
PIN 1 GATE
PIN 2 DRAIN
PIN 3 SOURCE
PIN 4 DRAIN

CASE 221A-02
TO-220AB

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.83	0.160	0.190
D	0.64	0.89	0.025	0.035
E	3.61	3.73	0.142	0.147
F	2.41	2.67	0.095	0.105
G	7.79	8.30	0.307	0.327
H	3.30	3.56	0.130	0.140
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
M	4.83	5.33	0.190	0.210
N	2.54	3.04	0.100	0.120
P	2.04	2.79	0.080	0.110
Q	1.14	1.39	0.045	0.055
R	5.97	6.48	0.235	0.255
S	0.76	1.27	0.030	0.050
T	1.14	—	0.045	—

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0\text{ mA}$)	$V_{(BR)DSS}$	350 400	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85\text{ Rated } V_{DSS}$, $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0\text{ mA}$, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 1.5\text{ Adc}$) ($I_D = 3.0\text{ Adc}$) ($I_D = 1.5\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	5.0 12 10	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.5\text{ Adc}$)	$r_{DS(on)}$	—	3.3	Ohms
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 1.5\text{ A}$)	g_{fs}	0.75	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	100	pF
Reverse Transfer Capacitance		C_{rss}	—	50	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DS} = 125\text{ V}$, $I_D = 1.5\text{ A}$, $R_{gen} = 50\text{ ohms}$)	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	60	ns
Turn-Off Delay Time		$t_{d(off)}$	—	60	ns
Fall Time		t_f	—	30	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage	V_{SD}	1.0	Vdc
Forward Turn-On Time	t_{on}	190	ns
Reverse Recovery Time	t_{rr}	300	ns

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 - SWITCHING TEST CIRCUIT

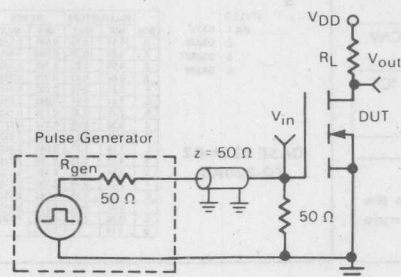
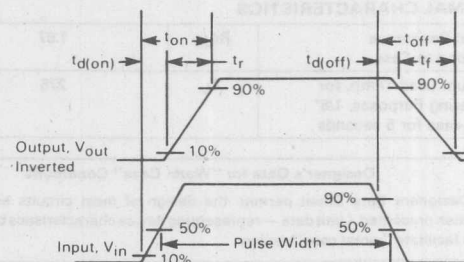


FIGURE 2 - SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

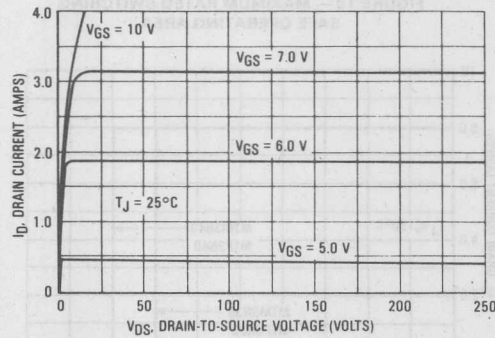


FIGURE 4 — ON-CHARACTERISTICS

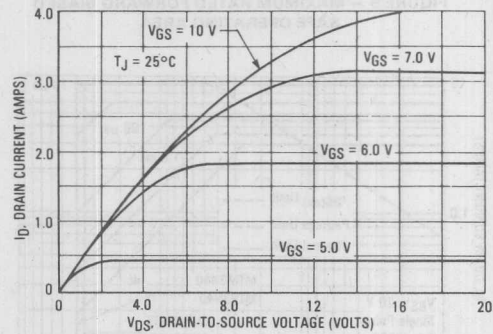


FIGURE 6 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

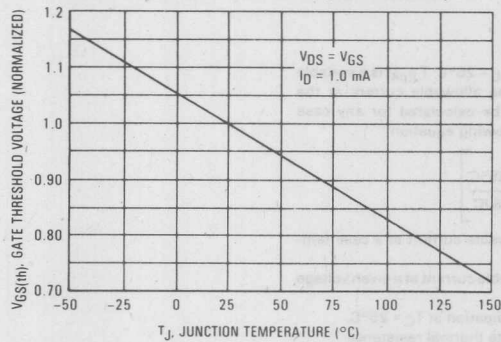


FIGURE 6 — TRANSFER CHARACTERISTICS

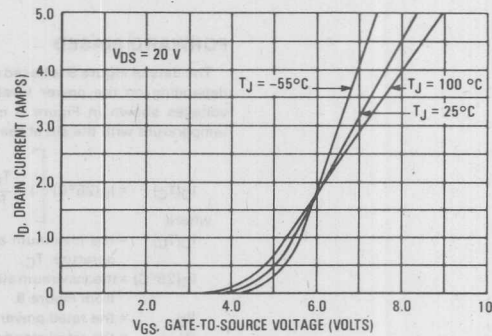


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

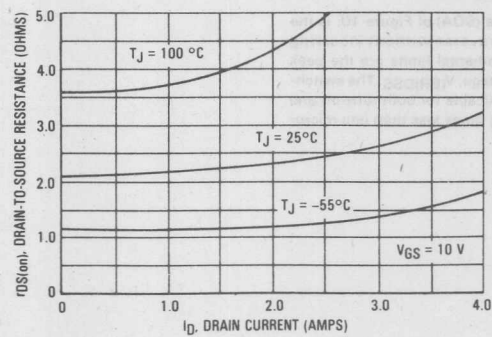
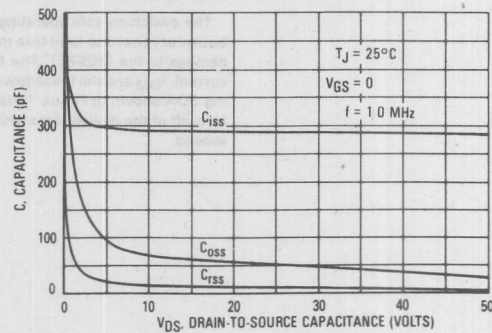


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

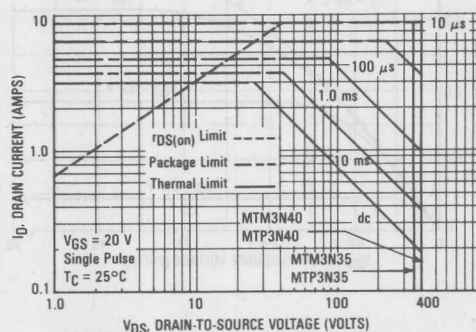
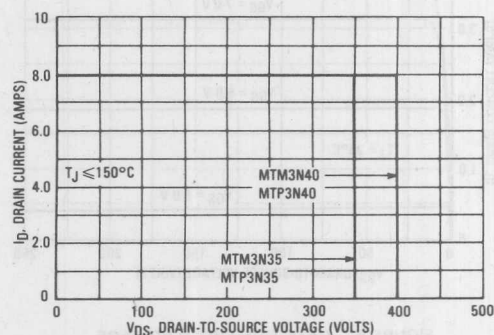


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

THERMAL RESPONSE

FIGURE 11 — MTM3N35/MTM3N40

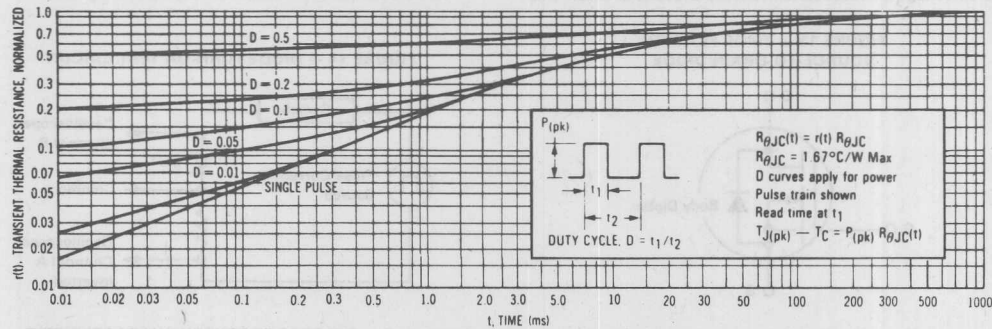
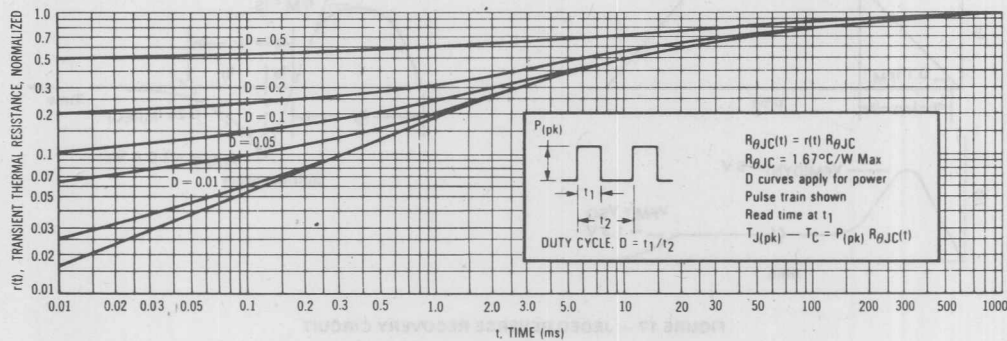


FIGURE 12 — MTP3N35/MTP3N40



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 11. Reversal of the drain voltage will cause current flow in the reverse direction. This

diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 13 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

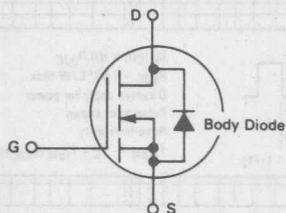


FIGURE 14 — DIODE TURN-ON TEST CIRCUIT

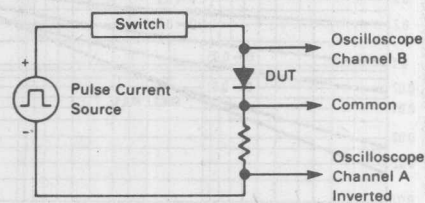


FIGURE 15 — DIODE TURN-ON WAVEFORMS

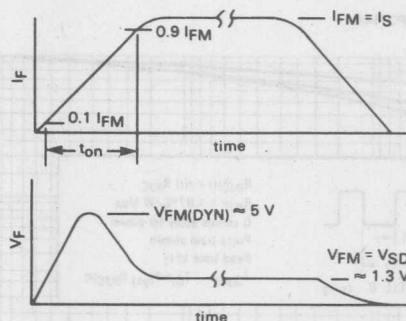


FIGURE 16 — REVERSE RECOVERY CHARACTERISTIC

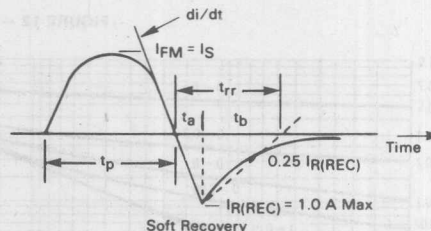
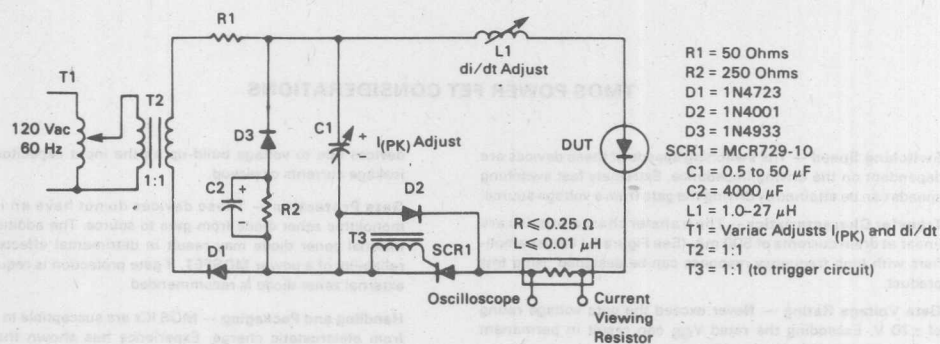


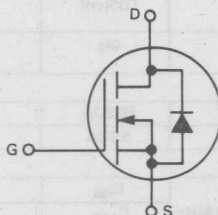
FIGURE 17 — JEDEC REVERSE RECOVERY CIRCUIT



**MOTOROLA****MTM3N55, MTM3N60
MTP3N55, MTP3N60****Designer's Data Sheet****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)

**MAXIMUM RATINGS**

Rating	Symbol	MTM3N55 MTP3N55	MTM3N60 MTP3N60	Unit
Drain — Source Voltage	V_{DSS}	550	600	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0$ m Ω)	V_{DGR}	550	600	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	3.0		Adc
Pulsed	I_{DM}	10		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75	0.6	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

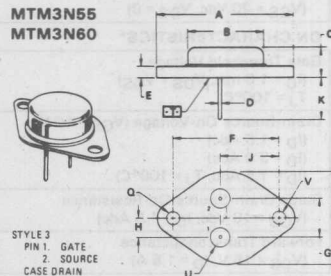
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C/W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

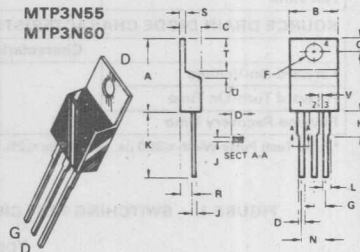
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

3 AMPERE**N-CHANNEL TMOS
POWER FET**

$r_{DS(on)} = 2.5$ OHMS
550 and 600 VOLTS

**MTM3N55
MTM3N60****CASE 1-05
TO-3**

DIM	MIN	MAX	MIN	MAX
A	29.37	—	1.550	—
B	—	21.08	—	0.820
C	6.35	7.62	0.250	0.300
D	0.97	1.05	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.181 BSC	—
G	10.97 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.10	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	26.67	—	1.050
N	4.83	5.33	0.190	0.210
O	3.81	4.19	0.150	0.165

**MTP3N55
MTP3N60****CASE 221A-02
TO-220AB**

DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.85	10.29	0.380	0.405
C	4.06	4.81	0.160	0.190
D	0.64	0.89	0.025	0.035
E	3.61	3.73	0.142	0.147
F	2.41	2.67	0.095	0.105
G	2.79	3.20	0.110	0.130
H	0.35	0.56	0.014	0.022
I	12.10	14.27	0.500	0.562
J	1.14	1.27	0.045	0.050
K	4.83	5.33	0.190	0.210
L	2.54	3.04	0.100	0.120
M	2.04	2.79	0.080	0.110
N	1.14	1.39	0.045	0.055
O	5.97	6.48	0.235	0.255
P	0.76	1.27	0.030	0.050
Q	1.14	—	0.045	—

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0\text{ mA}$)	$V_{(BR)DSS}$	550 600	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0\text{ mA}$, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 1.5\text{ Adc}$) ($I_D = 3.0\text{ Adc}$) ($I_D = 1.5\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	3.75 9.0 7.5	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.5\text{ Adc}$)	$r_{DS(on)}$	—	2.5	Ohms
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 1.5\text{ A}$)	g_{fs}	1.5	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	300	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	(V _{DS} = 125 V, I _D = 1.5 A, R _{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	100	ns
Turn-Off Delay Time		$t_{d(off)}$	—	180	ns
Fall Time		t_f	—	80	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage	V_{SD}	1.1	Vdc
Forward Turn-On Time	t_{on}	70	ns
Reverse Recovery Time	t_{rr}	165	ns

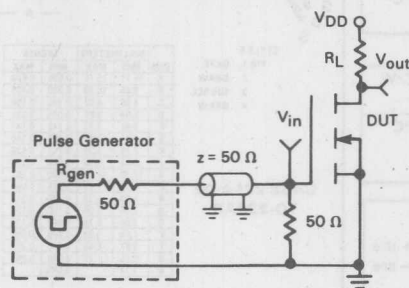
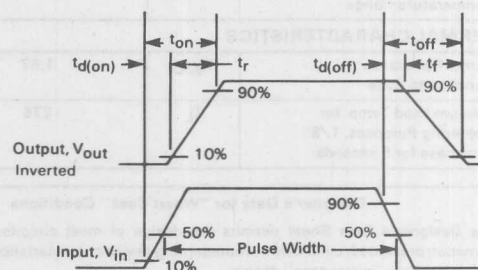
*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING****FIGURE 1 — SWITCHING TEST CIRCUIT****FIGURE 2 — SWITCHING WAVEFORMS**

FIGURE 3 — OUTPUT CHARACTERISTICS

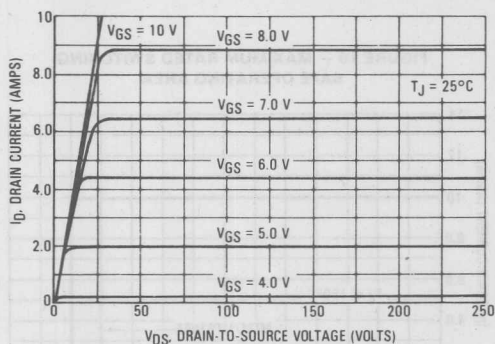


FIGURE 4 — ON-REGION CHARACTERISTICS

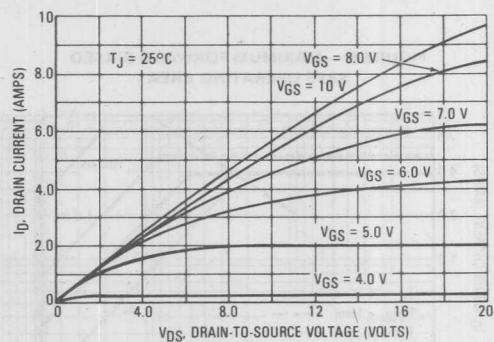


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

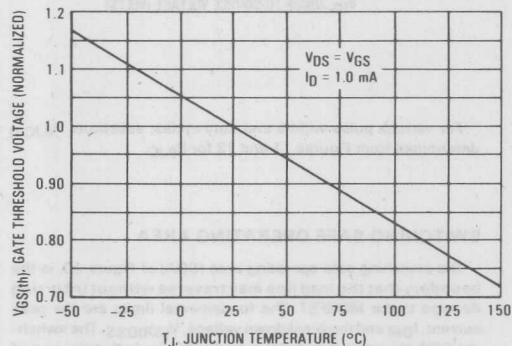


FIGURE 6 — TRANSFER CHARACTERISTICS

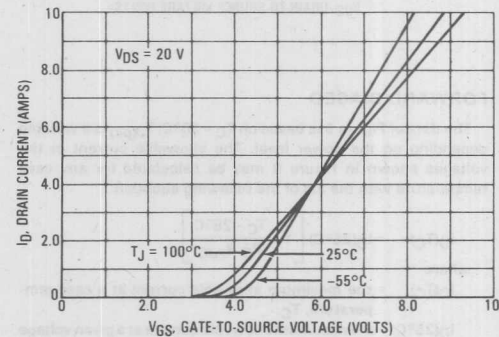


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

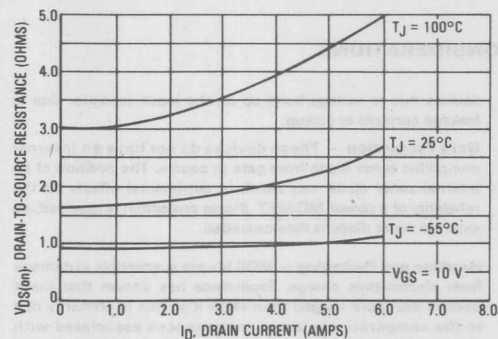
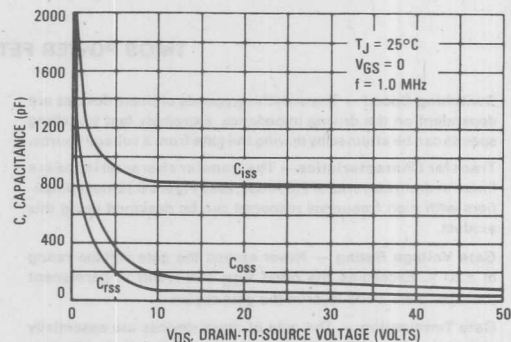
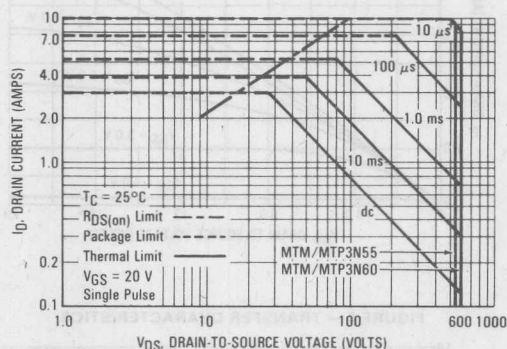


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM FORWARD BIASED SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

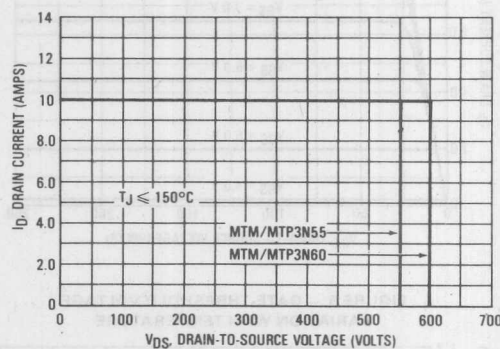
$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



For various pulse widths and duty cycles, substitute $R_{\theta JC}(t)$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 2.0 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

THERMAL RESPONSE

FIGURE 11 — MTM3N55/MTM3N60

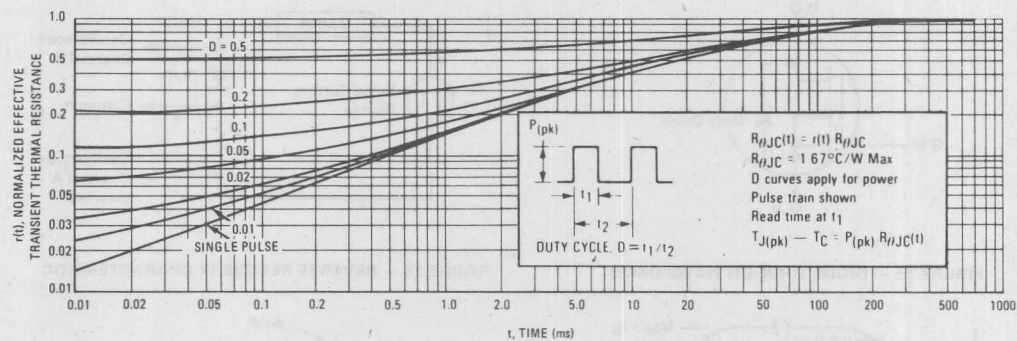
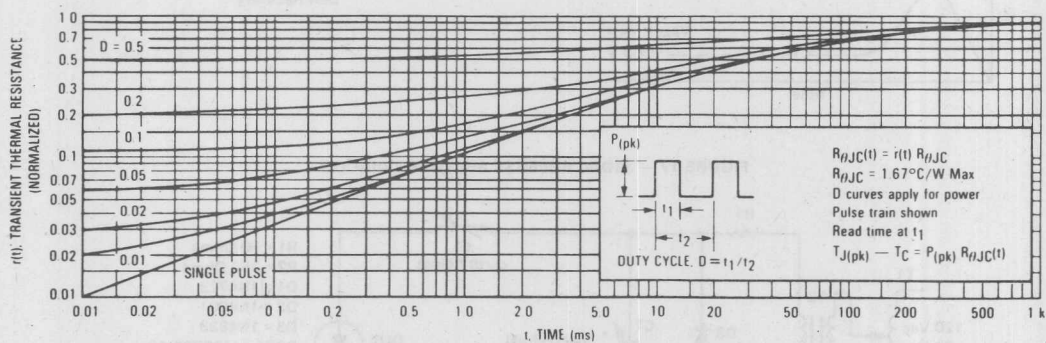


FIGURE 12 — MTP3N55/MTP3N60



TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 11. Reversal of the drain voltage will cause current flow in the reverse direction. This

diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 13 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

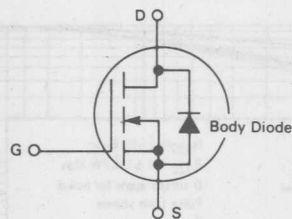


FIGURE 14 — DIODE TURN-ON TEST CIRCUIT

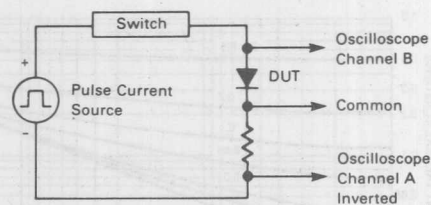


FIGURE 15 — DIODE TURN-ON WAVEFORMS

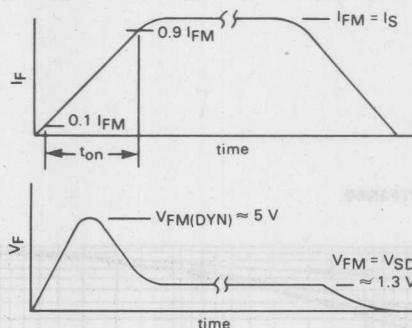


FIGURE 16 — REVERSE RECOVERY CHARACTERISTIC

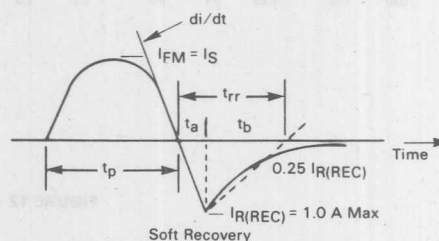
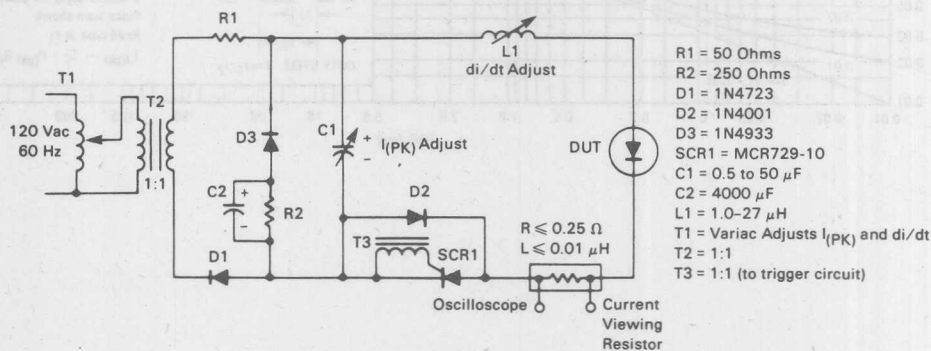


FIGURE 17 — JEDEC REVERSE RECOVERY CIRCUIT



- R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μ F
C2 = 4000 μ F
L1 = 1.0-27 μ H
T1 = Variac Adjusts $I_{(PK)}$ and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)



MOTOROLA

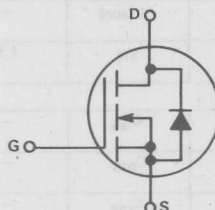
MTM4N45, MTM4N50 MTP4N45, MTP4N50

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

Rating	Symbol	MTM4N45 MTP4N45	MTM4N50 MTP4N50	Unit
Drain — Source Voltage	V_{DSS}	450	500	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	450	500	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current — Continuous	I_D	4.0		Adc
Drain Current — Pulsed	I_{DM}	10		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75		Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

4 AMPERE

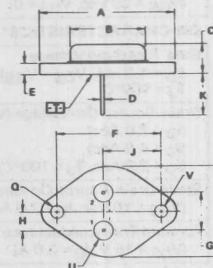
N-CHANNEL TMOS POWER FET

$r_{DS(on)} = 2.0 \text{ OHMS}$
450 and 500 VOLTS

MTM4N45
MTM4N50



STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN



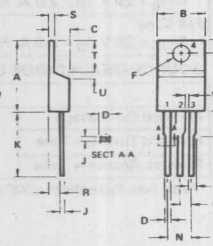
CASE 1-05
TO-3 TYPE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	26.67	—	1.050
N	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

MTP4N45
MTP4N50



STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



CASE 221A-02
TO-220AB

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.26	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
M	4.83	5.33	0.190	0.210
N	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0\text{ mA}$)	$V_{(BR)DSS}$	450 500	— —	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_C = 100^\circ\text{C}$	I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0\text{ mA}$, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 2.0\text{ Adc}$) ($I_D = 4.0\text{ Adc}$) ($I_D = 2.0\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	4.0 9.0 8.0	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 2.0\text{ Adc}$)	$r_{DS(on)}$	—	2.0	Ohms
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 2.0\text{ A}$)	g_{fs}	1.5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{iss}	—	1200	pF
Output Capacitance ($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{oss}	—	300	pF
Reverse Transfer Capacitance ($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	80	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time ($V_{DS} = 25\text{ V}$, $I_D = 2.0\text{ A}$, $R_{gen} = 50\text{ ohms}$)	$t_{d(on)}$	—	50	ns
Rise Time ($V_{DS} = 25\text{ V}$, $I_D = 2.0\text{ A}$, $R_{gen} = 50\text{ ohms}$)	t_r	—	100	ns
Turn-Off Delay Time ($V_{DS} = 25\text{ V}$, $I_D = 2.0\text{ A}$, $R_{gen} = 50\text{ ohms}$)	$t_{d(off)}$	—	200	ns
Fall Time ($V_{DS} = 25\text{ V}$, $I_D = 2.0\text{ A}$, $R_{gen} = 50\text{ ohms}$)	t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage $I_S = 4.0\text{ A}$	V_{SD}	1.1	Vdc
Forward Turn-On Time $V_{GS} = 0$	t_{on}	250	ns
Reverse Recovery Time See Figures 17 and 18	t_{rr}	420	ns

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 – SWITCHING TEST CIRCUIT

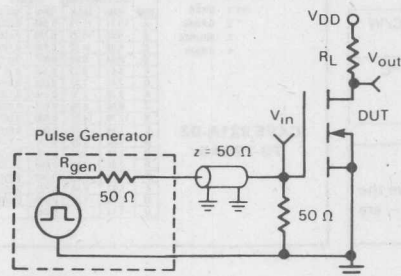
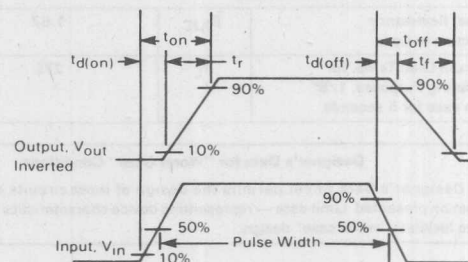


FIGURE 2 – SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 - OUTPUT CHARACTERISTICS

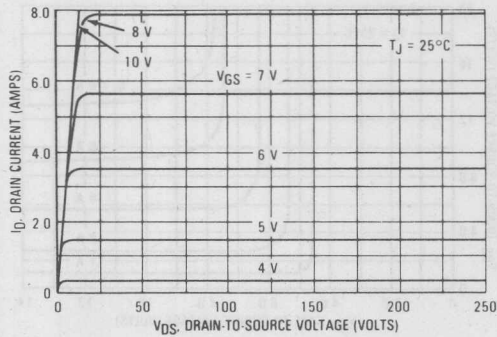


FIGURE 4 - ON-REGION CHARACTERISTICS

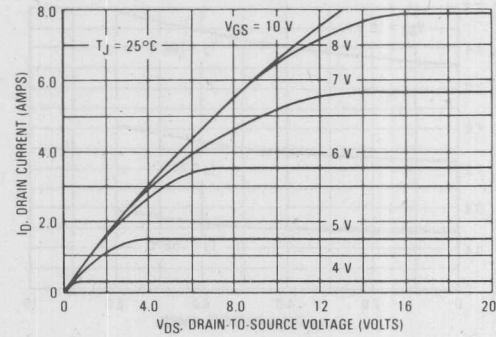


FIGURE 5 - GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

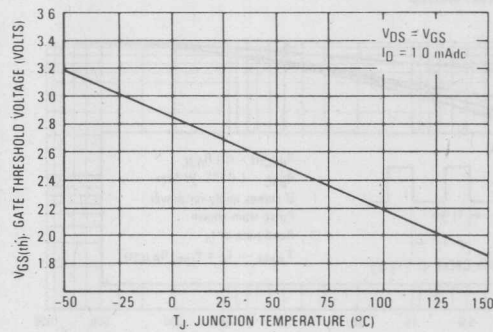


FIGURE 6 - TRANSFER CHARACTERISTICS

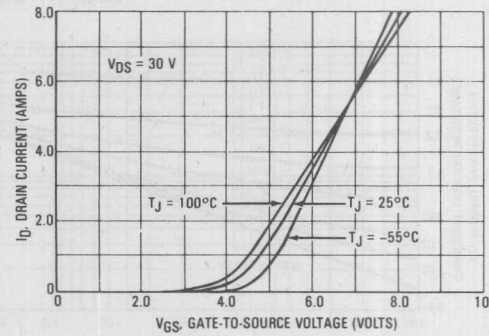


FIGURE 7 - ON-VOLTAGE versus TEMPERATURE

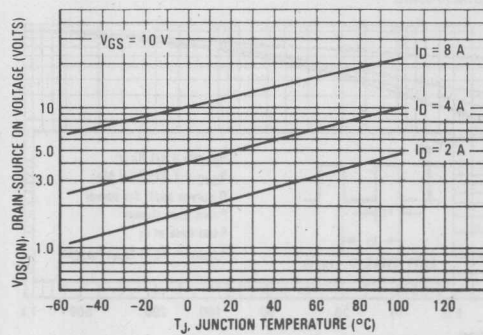
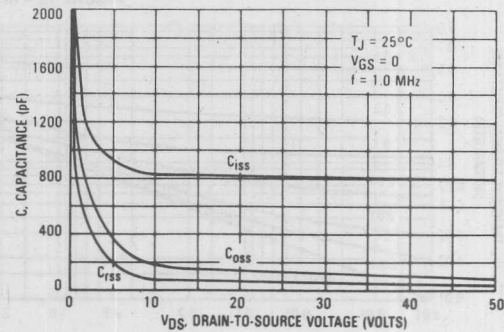


FIGURE 8 - CAPACITANCE VARIATION



TYPICAL CHARACTERISTICS

FIGURE 9 — ON-RESISTANCE versus DRAIN CURRENT

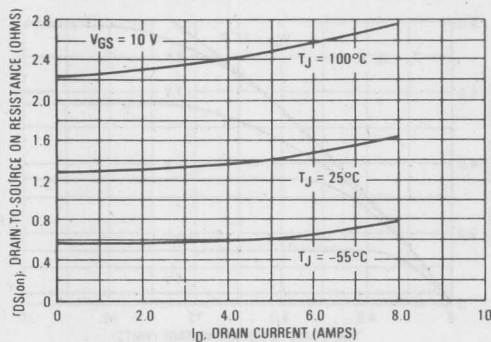
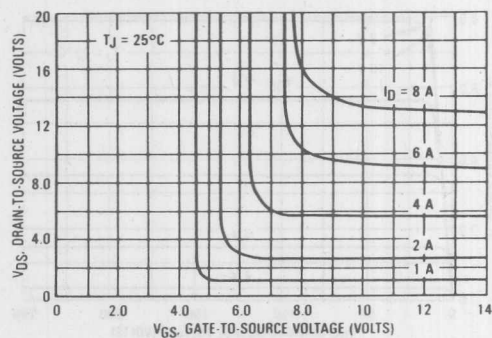


FIGURE 10 — ON-VOLTAGE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM4N45/MTM4N50

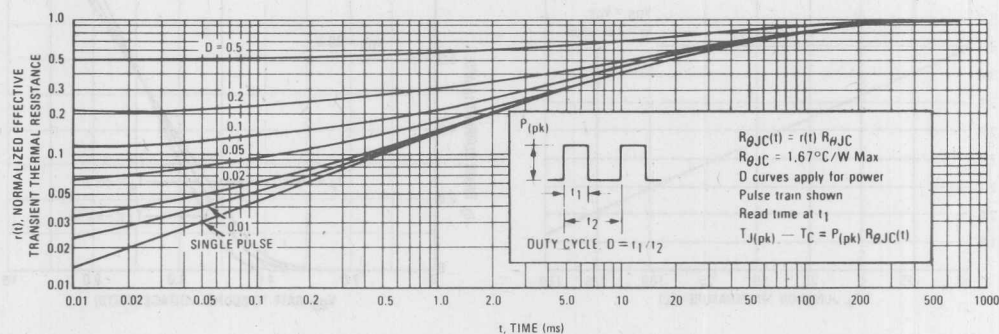
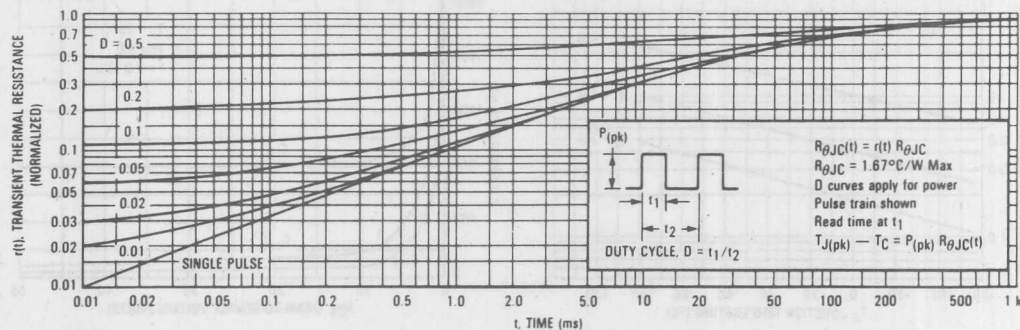


FIGURE 12 — MTP4N45/MTP4N50



SAFE OPERATING AREA INFORMATION

FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

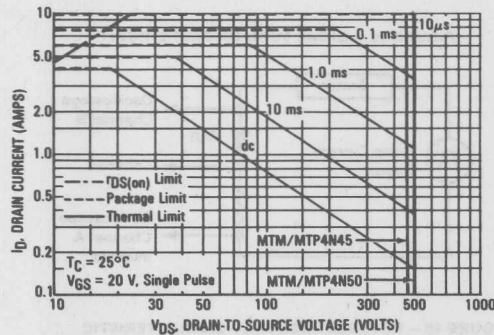
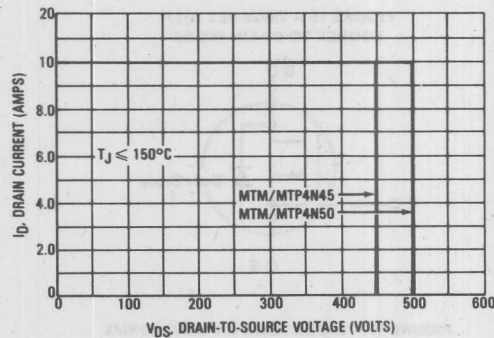


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$. $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 13 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 13.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 11. Reversal of the drain voltage will cause current flow in the reverse direction. This

diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 15 – TMOS FET WITH SOURCE-TO-DRAIN DIODE

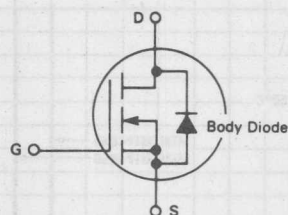


FIGURE 17 – DIODE TURN-ON WAVEFORMS

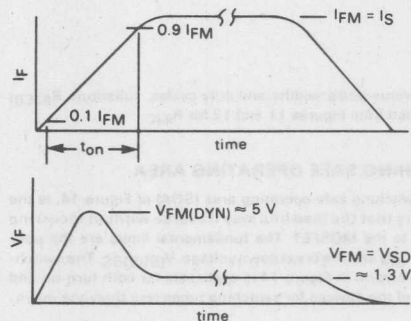


FIGURE 16 – DIODE TURN-ON TEST CIRCUIT

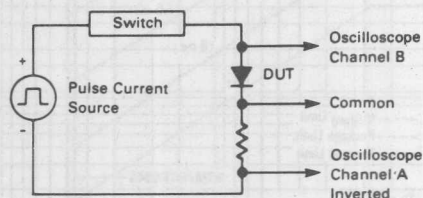


FIGURE 18 – REVERSE RECOVERY CHARACTERISTIC

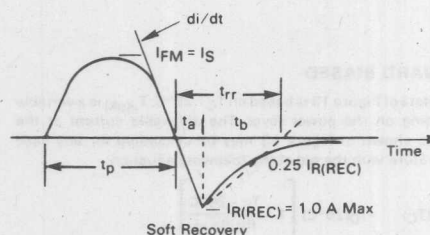
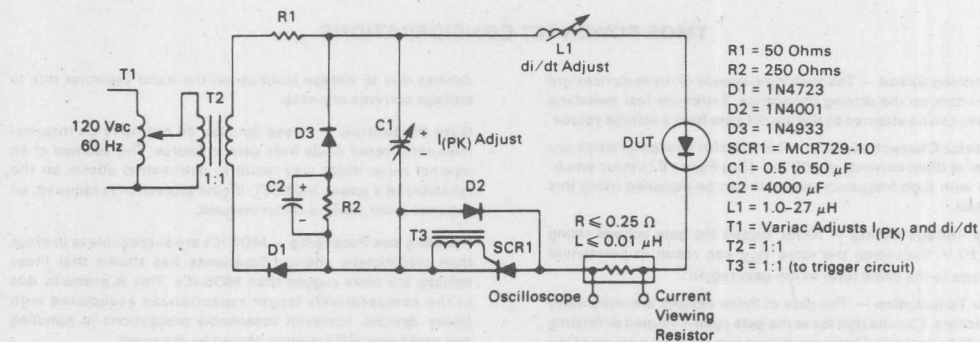


FIGURE 19 – JEDEC REVERSE RECOVERY CIRCUIT




MOTOROLA

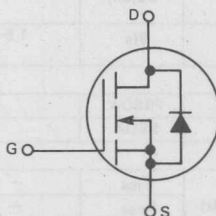
MTM5N18, MTM5N20 MTP5N18, MTP5N20

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

Rating	Symbol	MTM5N18 MTP5N18	MTM5N20 MTP5N20	Unit
Drain — Source Voltage	V_{DSS}	180	200	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	180	200	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	5.0		Adc
Pulsed	I_{DM}	15		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75		Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

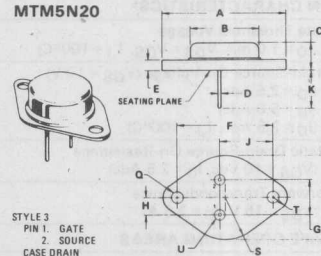
Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

5 AMPERE

N-CHANNEL TMOS POWER FET

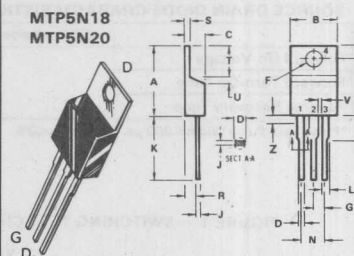
$r_{DS(on)} = 1.0 \text{ OHM}$
180 and 200 VOLTS

**MTM5N18
MTM5N20**


STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

TO-204
CASE 1-04
(TO-3 TYPE)

DIM	MIN	MAX	MIN	MAX
A	38.37	—	1.500	—
B	—	21.08	—	0.830
C	0.35	7.62	0.250	0.300
D	0.87	1.09	0.039	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.53	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	28.67	—	1.090
N	2.54	3.05	0.100	0.120

**MTP5N18
MTP5N20**


STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
E	3.61	3.73	0.142	0.147
F	2.41	2.67	0.095	0.105
G	2.79	3.30	0.110	0.130
H	0.36	0.56	0.014	0.022
J	12.70	14.27	0.500	0.562
K	1.14	1.27	0.045	0.050
L	4.83	5.53	0.190	0.210
M	2.54	3.04	0.100	0.120
N	2.04	2.79	0.080	0.110
O	1.14	1.39	0.045	0.055
P	5.97	6.40	0.235	0.255
Q	0.78	1.27	0.030	0.050
R	1.14	—	0.045	—
S	—	2.60	—	0.090

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	180 200	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$, $T_J = 100^\circ\text{C}$)	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 2.5$ Adc) ($I_D = 5.0$ Adc) ($I_D = 2.5$ Adc, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	2.5 6.0 5.0	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 2.5$ Adc)	$r_{DS(on)}$	—	1.0	Ohms
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 2.5$ A)	g_{fs}	1.5	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 10
Switching Safe Operating Area	SSOA	See Figure 11

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	150	pF
Reverse Transfer Capacitance		C_{rss}	—	30	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	(V _{DS} = 25 V, I _D = 2.5 A, R _{gen} = 50 ohms)	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	60	ns
Turn-Off Delay Time		$t_{d(off)}$	—	40	ns
Fall Time		t_f	—	40	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

	Characteristic	Symbol	Typ	Unit
Forward On-Voltage	$I_S = 5.0$ A	V_{SD}	2.0	Vdc
Forward Turn-On Time	$V_{GS} = 0$	t_{on}	200	ns
Reverse Recovery Time	See Figures 16 and 17	t_{rr}	300	ns

*Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.

FIGURE 1 — SWITCHING TEST CIRCUIT

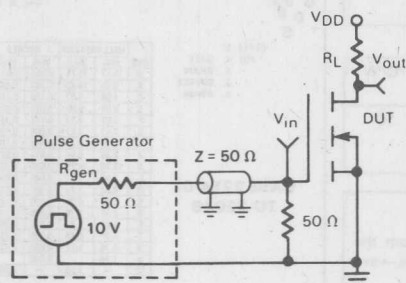
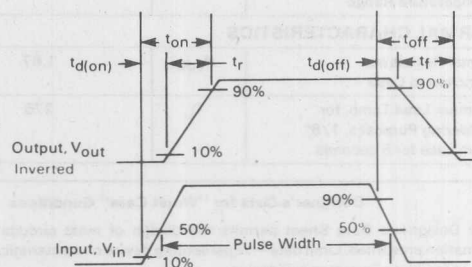


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

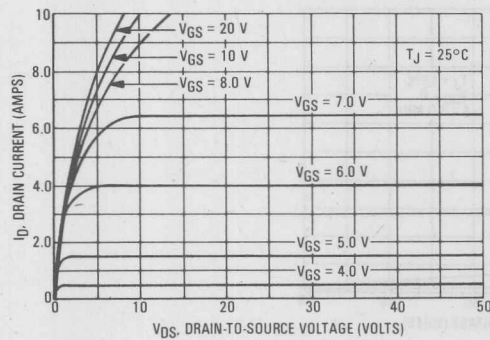


FIGURE 4 — ON-REGION CHARACTERISTICS

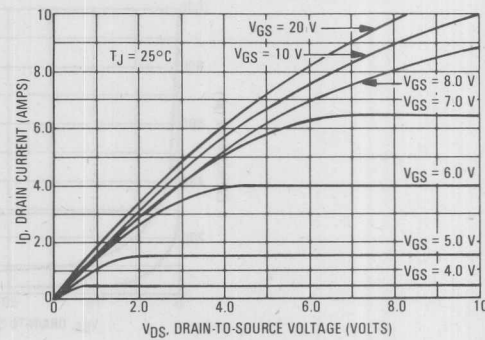


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

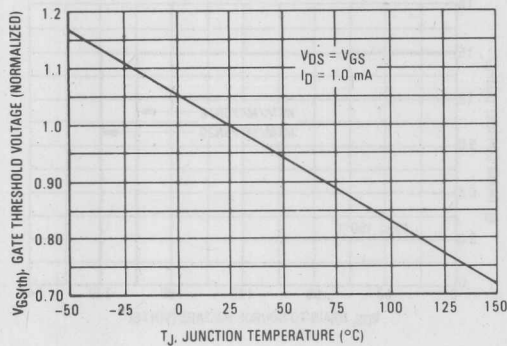


FIGURE 6 — TRANSFER CHARACTERISTICS

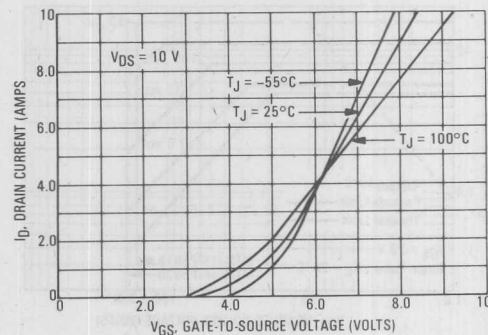


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

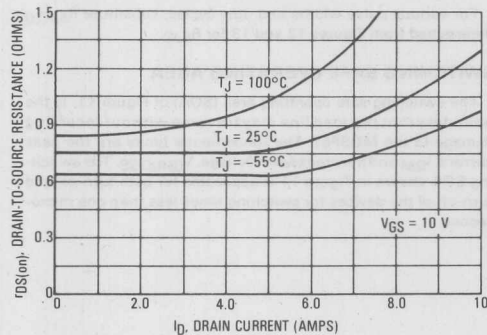
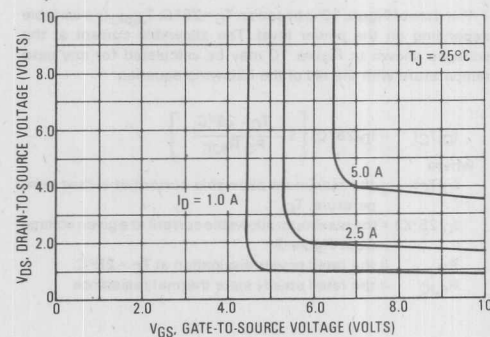


FIGURE 8 — ON-VOLTAGE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — CAPACITANCE VARIATION

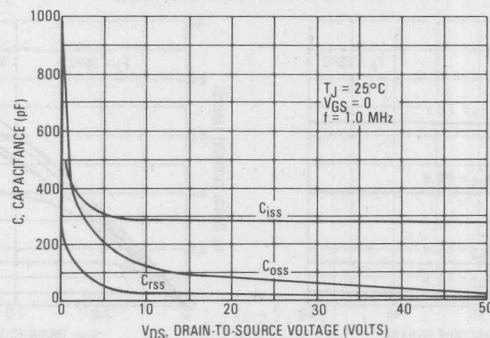


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

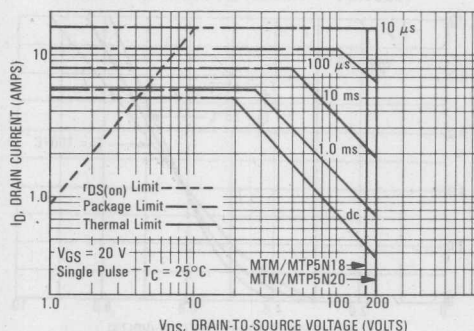
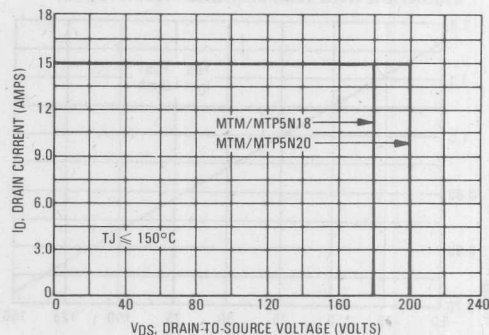


FIGURE 11 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 10 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 10 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 12 and 13 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 11, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 11 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

THERMAL RESPONSE

FIGURE 12 — MTM5N18/MTM5N20

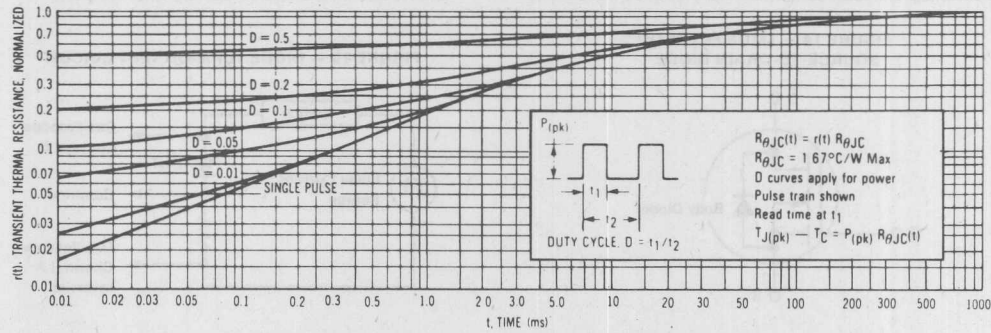
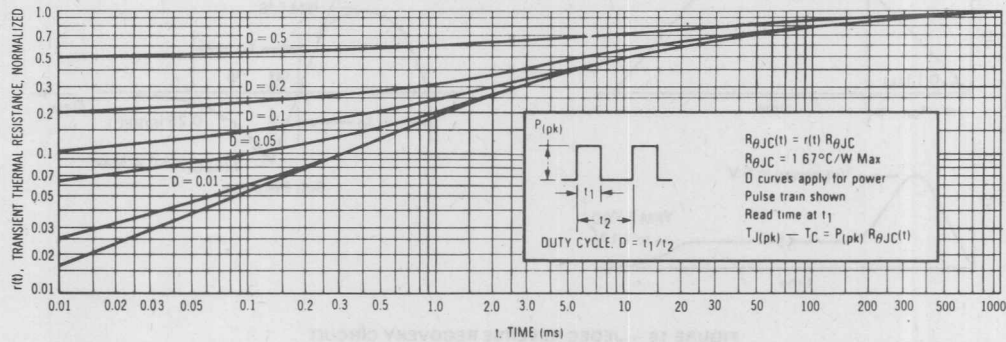


FIGURE 13 — MTP5N18/MTP5N20



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 1.5 A. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 14. Reversal of the drain voltage will cause current flow in the reverse direction. This

diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 14 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

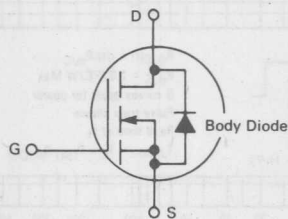


FIGURE 15 — DIODE TURN-ON TEST CIRCUIT

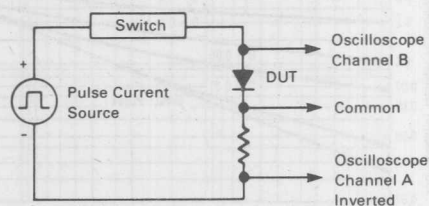


FIGURE 16 — BODY DIODE TURN-ON WAVEFORMS

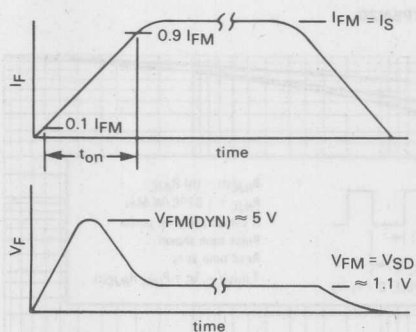


FIGURE 17 — REVERSE RECOVERY CHARACTERISTIC

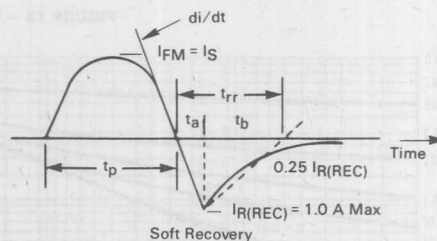
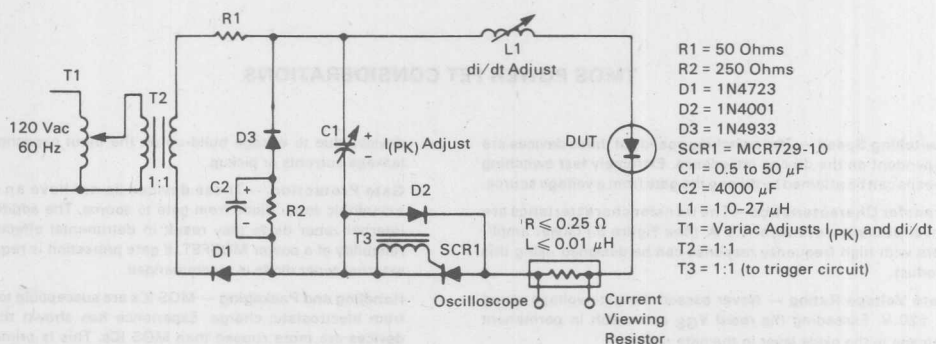


FIGURE 18 — JEDEC REVERSE RECOVERY CIRCUIT





MOTOROLA

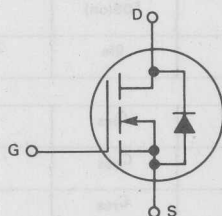
MTM5N35, MTM5N40 MTP5N35, MTP5N40

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

Rating	Symbol	MTM5N35 MTP5N35	MTM5N40 MTP5N40	Unit
Drain — Source Voltage	V_{DSS}	350	400	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ m}\Omega$)	V_{DGR}	350	400	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	5.0		Adc
Pulsed	I_{DM}	12		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75		Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

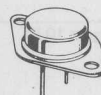
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

5 AMPERE

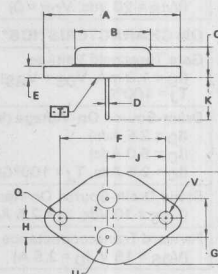
N-CHANNEL TMOS POWER FET

$r_{DS(on)} = 1.5 \text{ OHMS}$
350 and 400 VOLTS

MTM5N35
MTM5N40



STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN



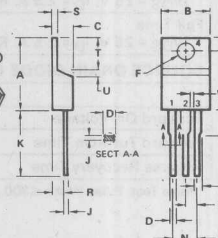
DIM	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	21.08	—	0.830	—
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-3 TYPE

MTP5N35
MTP5N40



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.79	1.27	0.030	0.050
V	1.14	—	0.045	—

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0\text{ mA}$)	$V_{(BR)DSS}$	350 400	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0\text{ mA}$, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 2.5\text{ Adc}$) ($I_D = 5.0\text{ Adc}$) ($I_D = 2.5\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	3.75 8.0 6.0	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 2.5\text{ Adc}$)	$r_{DS(on)}$	—	1.5	Ohms
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 2.5\text{ A}$)	g_{fs}	2.0	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{iss}	—	1200	pF
Output Capacitance ($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{oss}	—	300	pF
Reverse Transfer Capacitance ($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	80	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time ($V_{DS} = 25\text{ V}$, $I_D = 2.5\text{ A}$, $R_{gen} = 50\text{ ohms}$)	$t_{d(on)}$	—	50	ns
Rise Time ($V_{DS} = 25\text{ V}$, $I_D = 2.5\text{ A}$, $R_{gen} = 50\text{ ohms}$)	t_r	—	100	ns
Turn-Off Delay Time ($V_{DS} = 25\text{ V}$, $I_D = 2.5\text{ A}$, $R_{gen} = 50\text{ ohms}$)	$t_{d(off)}$	—	200	ns
Fall Time ($V_{DS} = 25\text{ V}$, $I_D = 2.5\text{ A}$, $R_{gen} = 50\text{ ohms}$)	t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage $I_S = 5.0\text{ A}$	V_{SD}	1.1	Vdc
Forward Turn-On Time $V_{GS} = 0$	t_{on}	250	ns
Reverse Recovery Time See Figures 17 and 18	t_{rr}	420	ns

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

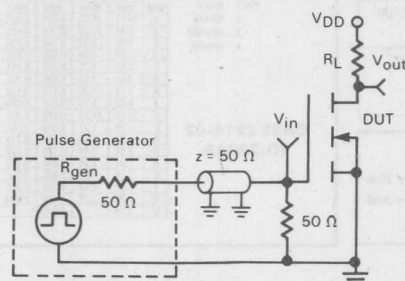
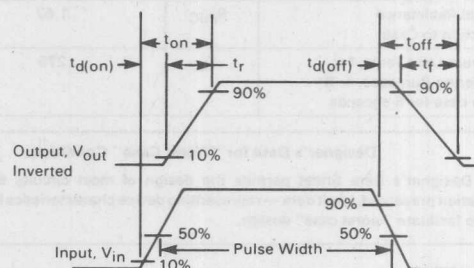


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

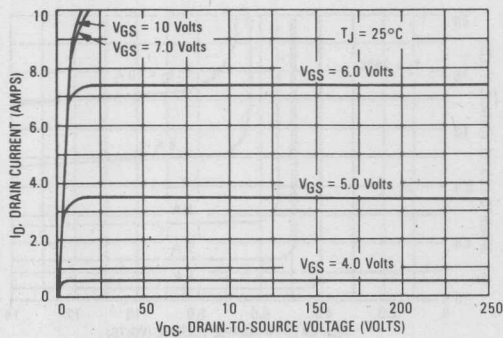


FIGURE 4 — ON-REGION CHARACTERISTICS

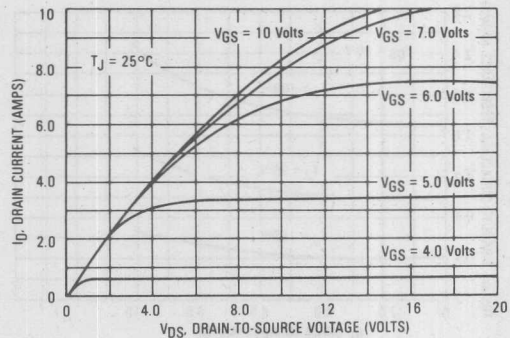


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

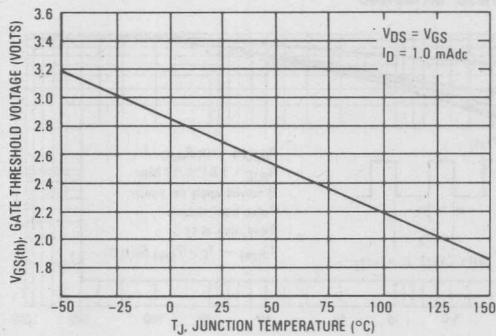


FIGURE 6 — TRANSFER CHARACTERISTICS

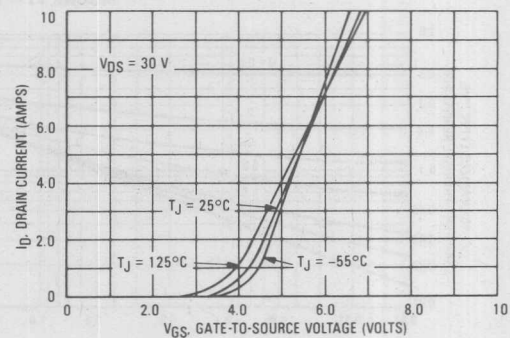


FIGURE 7 — ON-VOLTAGE versus TEMPERATURE

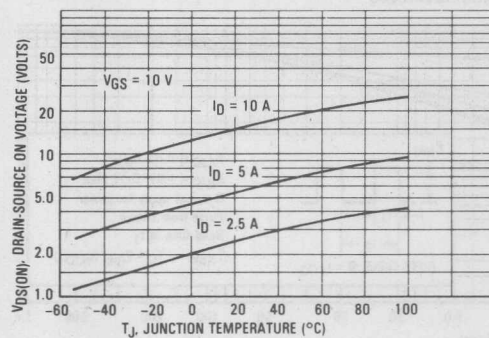
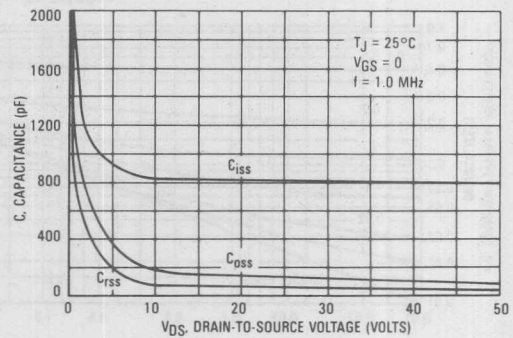


FIGURE 8 — CAPACITANCE VARIATION



TYPICAL CHARACTERISTICS

FIGURE 9 — ON-RESISTANCE versus DRAIN CURRENT

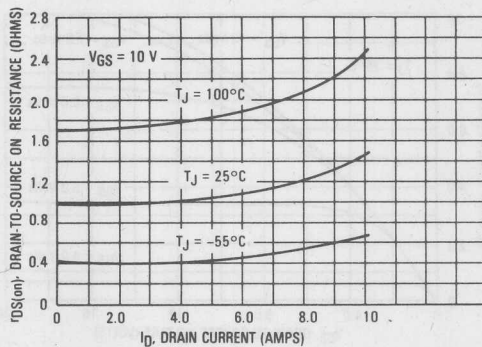
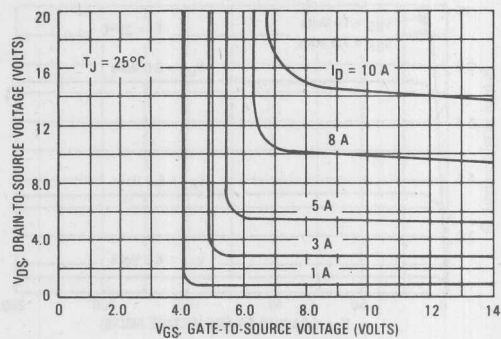


FIGURE 10 — ON-VOLTAGE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM5N35/MTM5N40

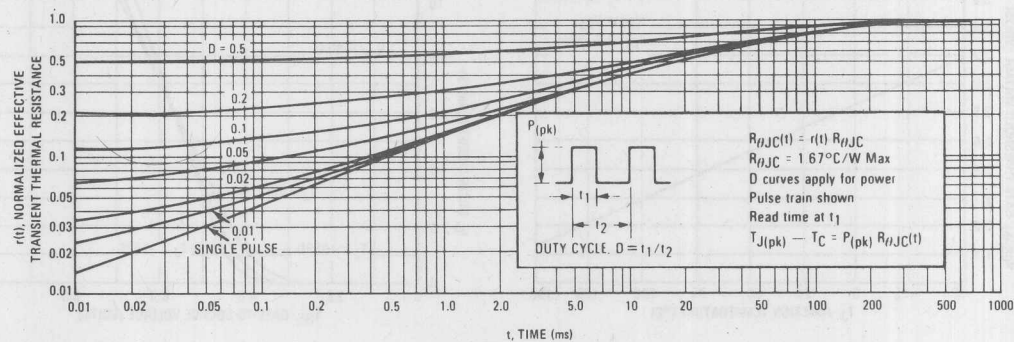


FIGURE 12 — MTP5N35/MTP5N40

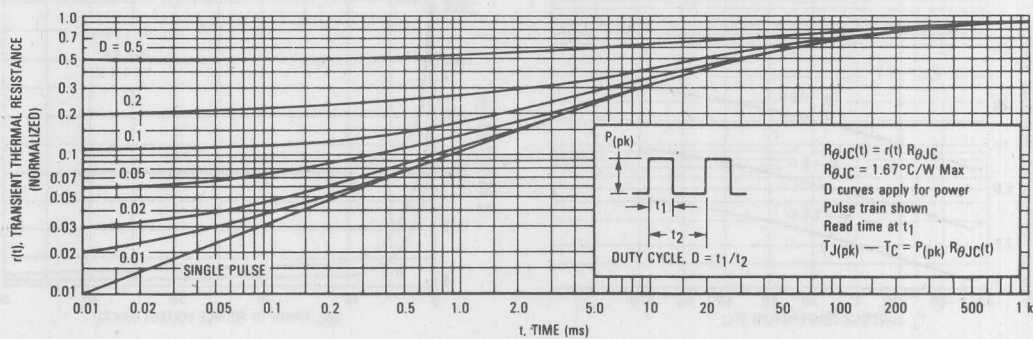
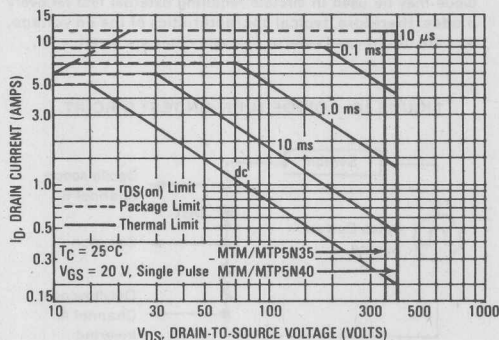


FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 13 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

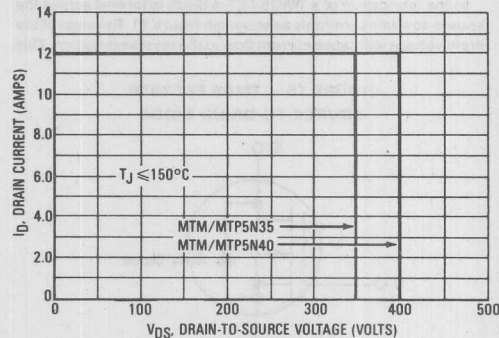
$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 13.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 11. Reversal of the drain voltage will cause current flow in the reverse direction. This

FIGURE 15 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

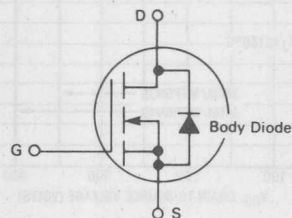
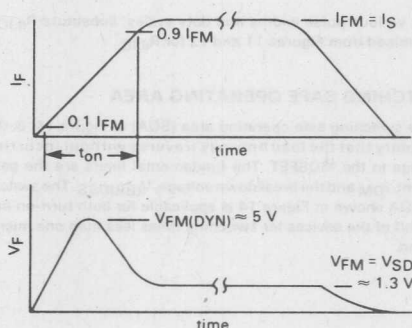


FIGURE 17 — DIODE TURN-ON WAVEFORMS



diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 16 — DIODE TURN-ON TEST CIRCUIT

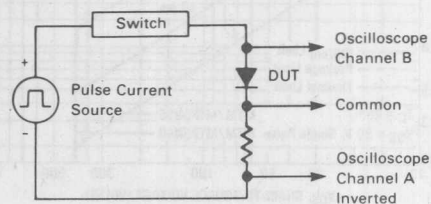


FIGURE 18 — REVERSE RECOVERY CHARACTERISTIC

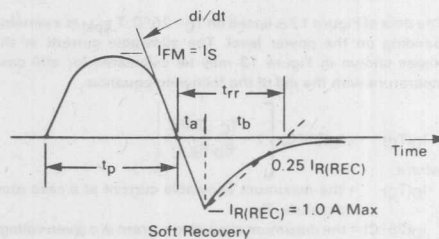
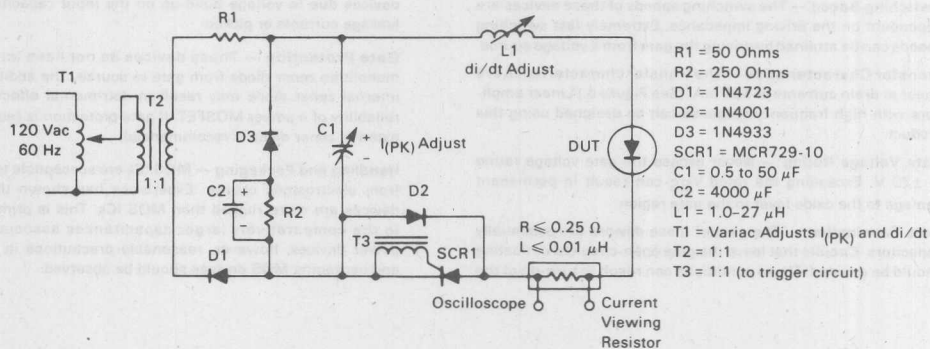


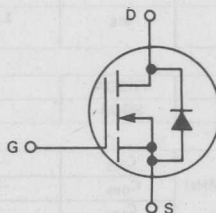
FIGURE 19 — JEDEC REVERSE RECOVERY CIRCUIT



**MOTOROLA****MTM6N55
MTM6N60****Designer's Data Sheet****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)

**MAXIMUM RATINGS**

Rating	Symbol	MTM6N55	MTM6N60	Unit
Drain — Source Voltage	V_{DSS}	550	600	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0$ m Ω)	V_{DGR}	550	600	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current				Adc
Continuous	I_D	6.0		
Pulsed	I_{DM}	30		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power	P_D	150		Watts
Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C		1.2		W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

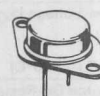
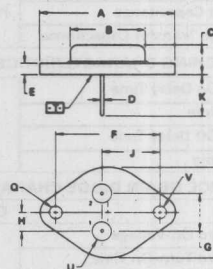
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

6 AMPERE**N-CHANNEL TMOS
POWER FET**

$r_{DS(on)} = 1.5$ OHMS
550 and 600 VOLTS

**MTM6N55
MTM6N60**

STYLE 3
PIN 1 GATE
2 SOURCE
CASE DRAIN

DIM	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	1.187 BSC		
G	10.92 BSC	0.430 BSC		
H	5.48 BSC	0.215 BSC		
J	16.89 BSC	0.665 BSC		
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	25.47	—	1.000
N	4.83	5.33	0.190	0.210
O	3.81	4.19	0.150	0.165

**CASE 1-05
TO-3 TYPE**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	550 600	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ BV _{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 3.0$ Adc) ($I_D = 6.0$ Adc) ($I_D = 3.0$ Adc, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	4.5 10 9.0	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 3.0$ Adc)	$r_{DS(on)}$	—	1.5	Ohms
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 3.0$ A)	g_{fs}	2.0	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	1800	pF
Output Capacitance		C_{oss}	—	350	pF
Reverse Transfer Capacitance		C_{rss}	—	150	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	$(V_{DS} = 125$ V, $I_D = 3.0$ A, $R_{gen} = 50$ ohms)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	120	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage $I_S = 6.0$ A	V_{SD}	1.0	Vdc
Forward Turn-On Time $V_{GS} = 0$, $di/dt = 25$ A/ μ s	t_{on}	175	ns
Reverse Recovery Time See Figures 14 and 15	t_{rr}	600	ns

*Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

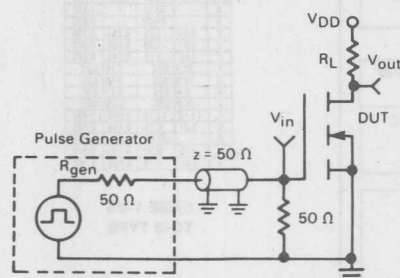
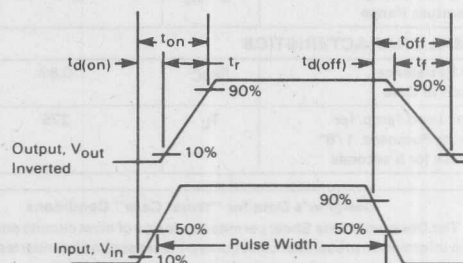


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

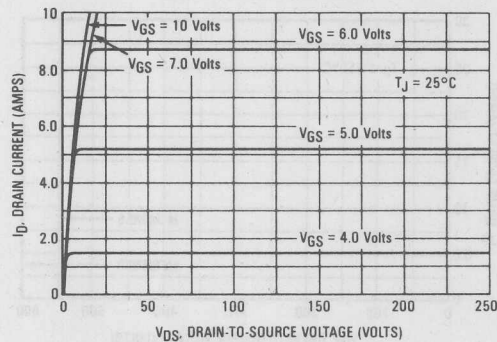


FIGURE 4 — ON-REGION CHARACTERISTICS

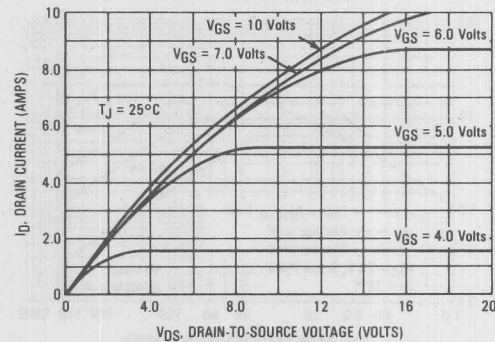


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

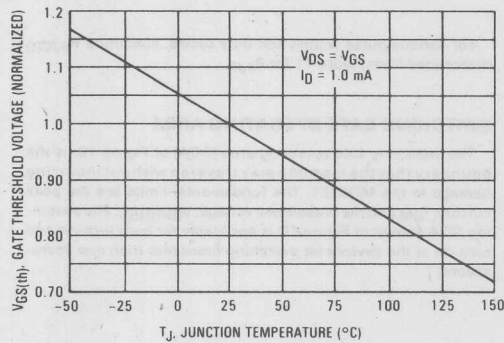


FIGURE 6 — TRANSFER CHARACTERISTICS

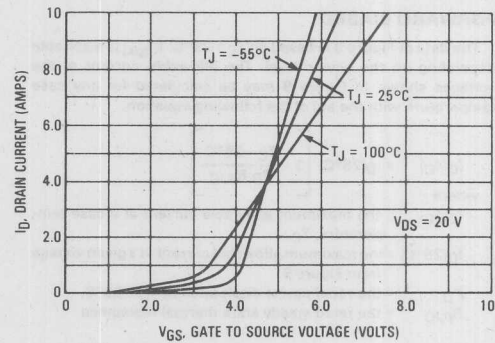


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

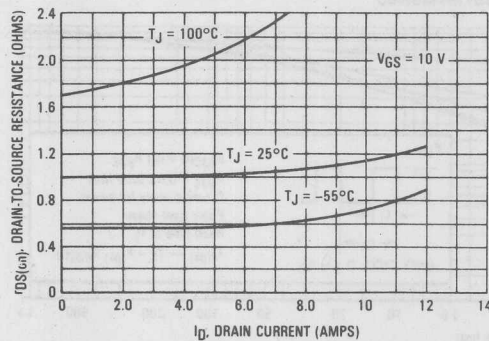
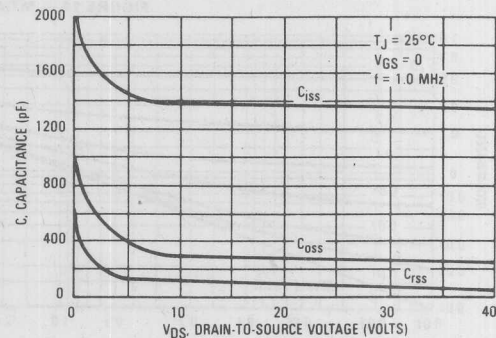


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

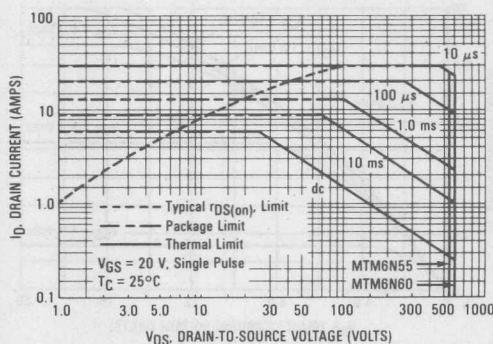
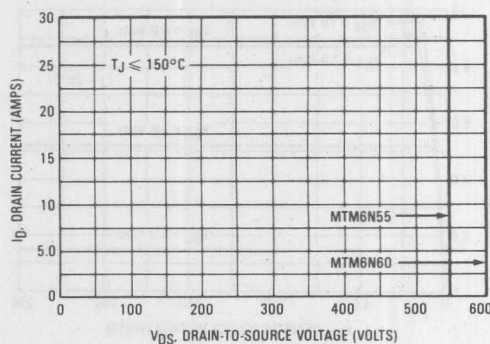


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

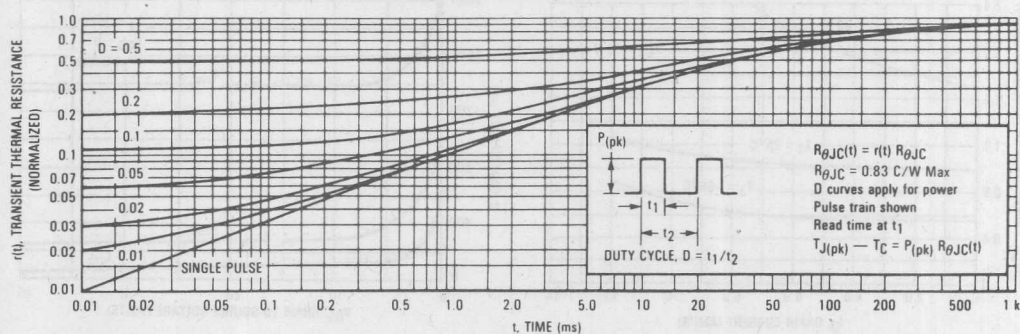
$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figure 11 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

FIGURE 11 — MTM6N55/MTM6N60



TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 11. Reversal of the drain voltage will cause current flow in the reverse direction. This

FIGURE 12 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

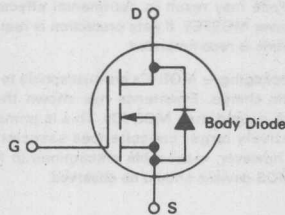
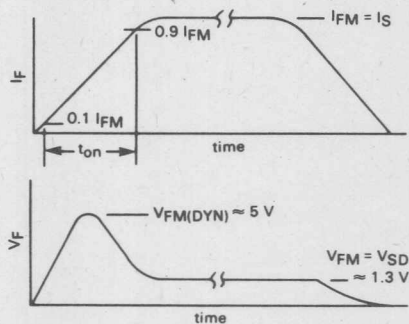


FIGURE 14 — DIODE TURN-ON WAVEFORMS



diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 13 — DIODE TURN-ON TEST CIRCUIT

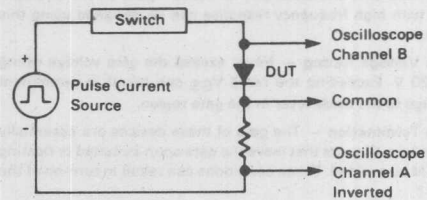


FIGURE 15 — REVERSE RECOVERY CHARACTERISTIC

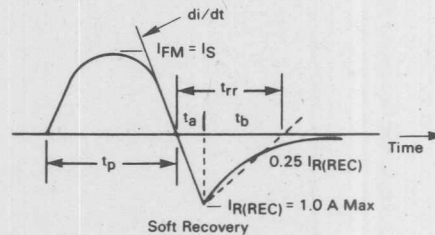
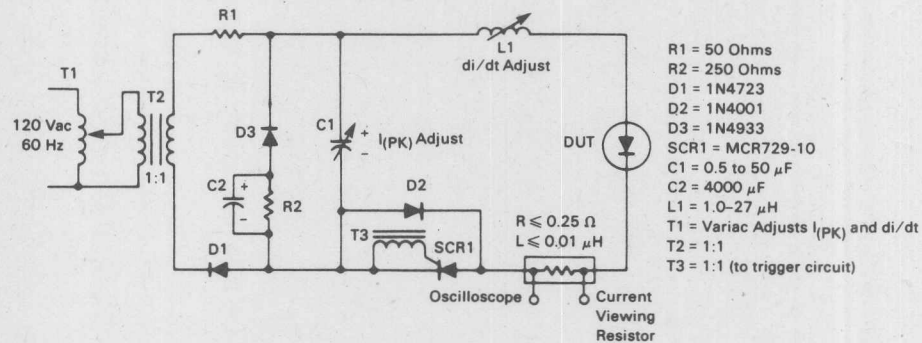


FIGURE 16 — JEDEC REVERSE RECOVERY CIRCUIT



MOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

FIGURE 1 — TRANSFER CHARACTERISTICS

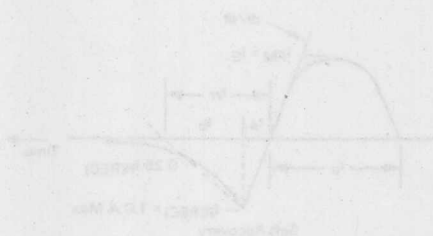
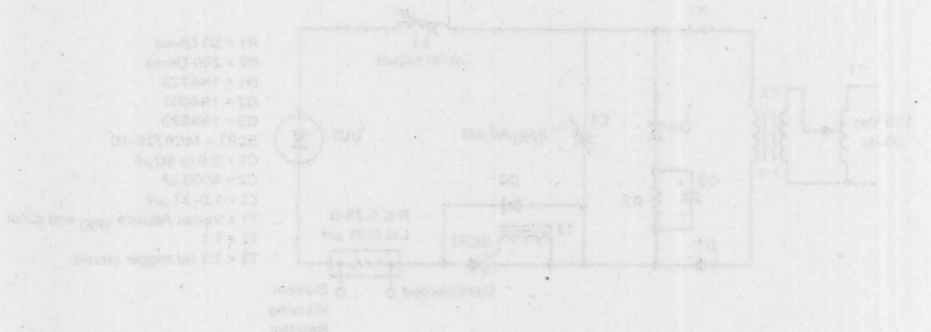


FIGURE 2 — GATE THRESHOLD VOLTAGE



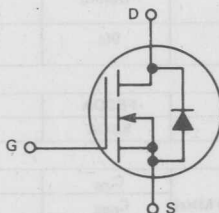
FIGURE 3 — GATE THRESHOLD VOLTAGE



**MOTOROLA****MTM7N45
MTM7N50****Designer's Data Sheet****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)

**MAXIMUM RATINGS**

Rating	Symbol	MTM7N45	MTM7N50	Unit
Drain — Source Voltage	V_{DSS}	450	500	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0$ m Ω)	V_{DGR}	450	500	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	7.0		Adc
Pulsed	I_{DM}	35		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150		Watts
		1.2		W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

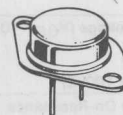
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

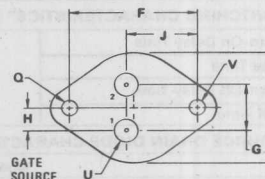
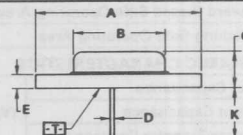
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

7 AMPERE**N-CHANNEL TMOS
POWER FET**

$r_{DS(on)} = 1.2$ OHM
450 and 500 VOLTS



CASE 1-05
TO-3 TYPE



STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. \square IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$\phi .13$ (0.005) M T V M

FOR LEADS:

$\phi .13$ (0.005) M T V M Q M

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.00	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	450 500	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mA _{dc}
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nA _{dc}

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 3.5$ A _{dc}) ($I_D = 7.0$ A _{dc}) ($I_D = 3.5$ A _{dc} , $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	4.2 10 8.4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 3.5$ A)	$r_{DS(on)}$	—	1.2	Ohms
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 3.5$ A)	g_{fs}	2.0	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	1800	pF
Output Capacitance		C_{oss}	—	350	pF
Reverse Transfer Capacitance		C_{rss}	—	150	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DS} = 125$ V, $I_D = 3.5$ A, $R_{gen} = 50$ ohms)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	250	ns
Fall Time		t_f	—	120	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage $I_S = 7.0$ A	V_{SD}	1.1	Vdc
Forward Turn-On Time $V_{GS} = 0$, $di/dt = 25$ A/ μ s	t_{on}	175	ns
Reverse Recovery Time See Figures 14 and 15	t_{rr}	600	ns

*Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

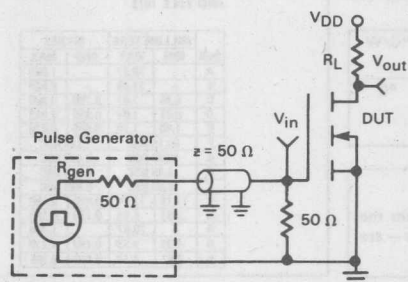
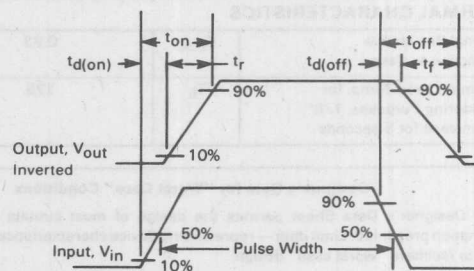


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

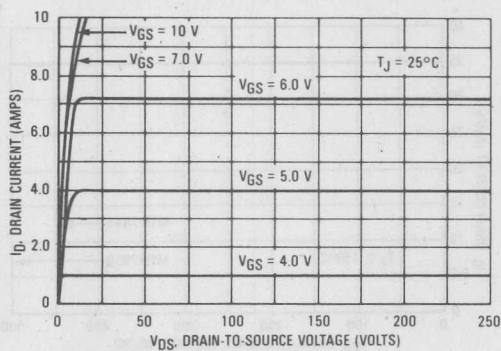


FIGURE 4 — ON-REGION CHARACTERISTICS

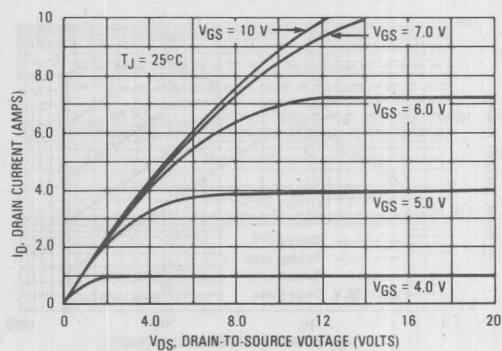


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

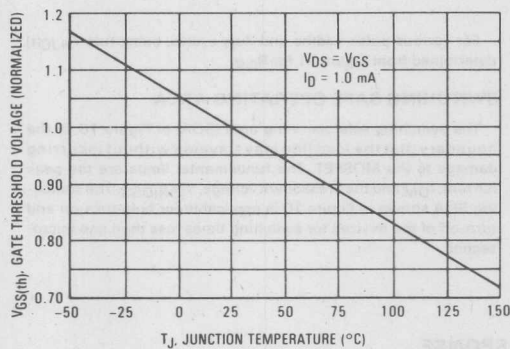


FIGURE 6 — TRANSFER CHARACTERISTICS

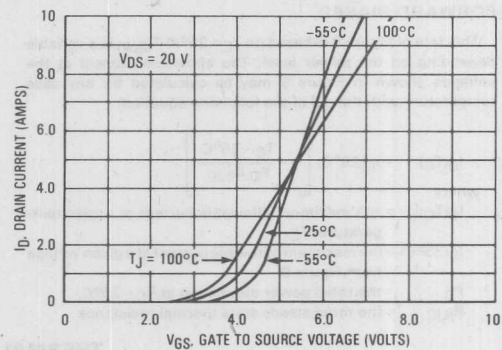


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

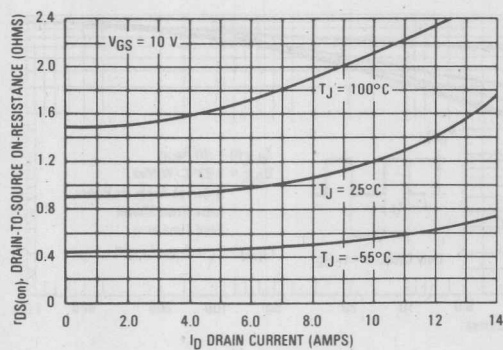
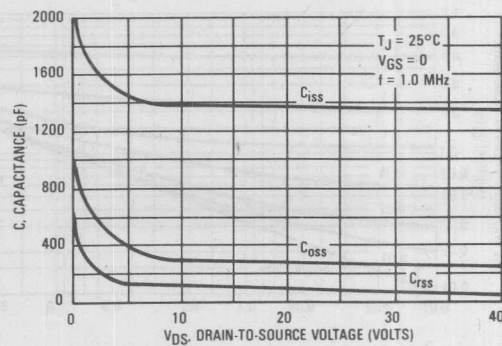


FIGURE 8 — CAPACITANCE VARIATION



TYPICAL CHARACTERISTICS

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

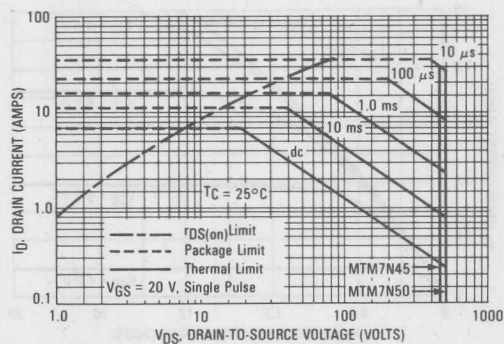
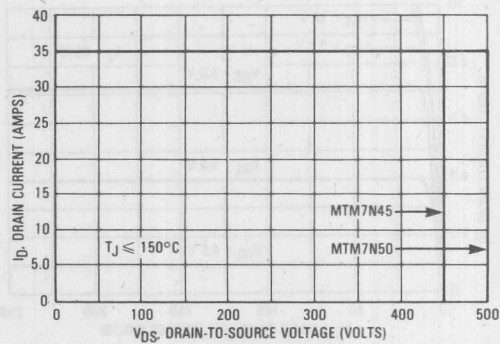


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

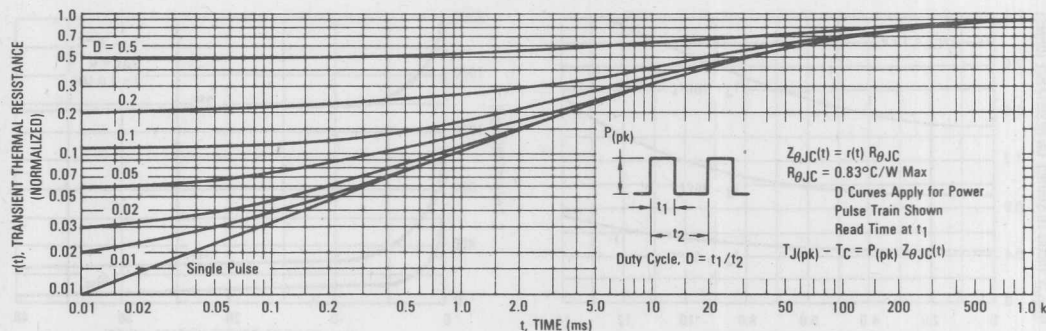
For various pulse widths and duty cycles, substitute $R_{\theta JC}(t)$ determined from Figure 11 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

THERMAL RESPONSE

FIGURE 11 — THERMAL RESPONSE



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 12. Reversal of the drain voltage will cause current flow in the reverse direction. This

FIGURE 12 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

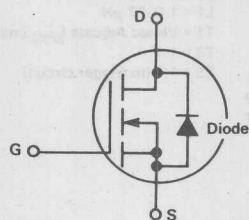
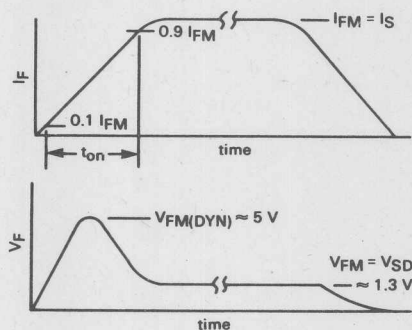


FIGURE 14 — DIODE TURN-ON WAVEFORMS



diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 13 — DIODE TURN-ON TEST CIRCUIT

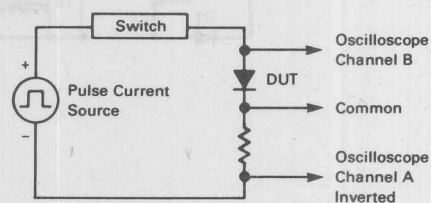


FIGURE 15 — REVERSE RECOVERY CHARACTERISTIC

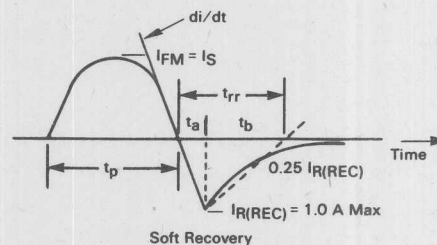
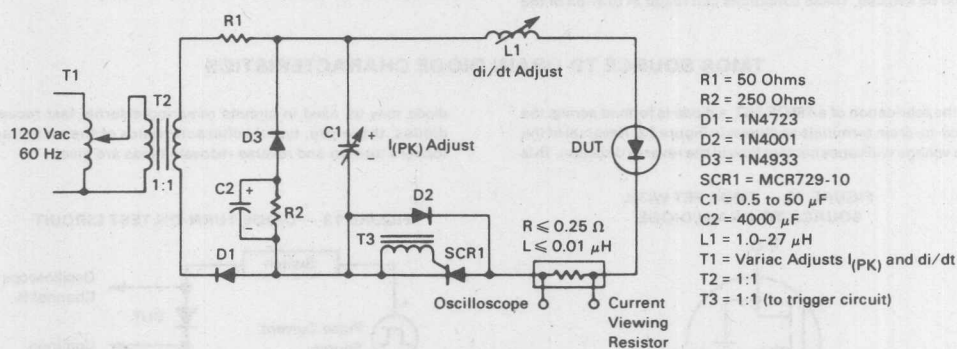


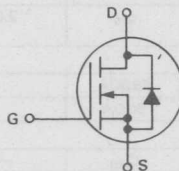
FIGURE 16 — JEDEC REVERSE RECOVERY CIRCUIT



**MOTOROLA****MTM8N12, MTM8N15
MTP8N12, MTP8N15****Designer's Data Sheet****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement; $V_{G(th)} = 4.5$ Volts (max)

**MAXIMUM RATINGS**

Rating	Symbol	MTM8N12 MTP8N12	MTM8N15 MTP8N15	Unit
Drain — Source Voltage	V_{DSS}	120	150	Vdc
Drain — Gate Voltage ($R_{GS} = 1 \text{ meg}\Omega$)	V_{DGR}	120	150	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	8.0		Adc
Pulsed	I_{DM}	20		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75		Watts
		0.6		W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

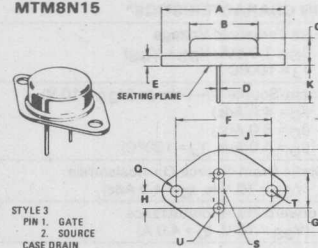
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C/W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

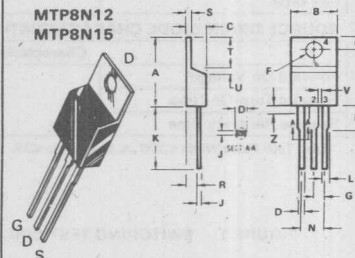
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

8 AMPERE**N-CHANNEL TMOS
POWER FET**

$r_{DS(on)} = 0.5 \text{ OHMS}$
120 and 150 VOLTS

**MTM8N12
MTM8N15****CASE 1-04
TO-3 TYPE**

DIM	MIN	MAX	MIN	MAX
A	—	38.37	—	1.506
B	—	21.06	—	0.830
C	6.35	7.62	0.250	0.300
D	6.35	7.62	0.250	0.300
E	1.40	1.75	0.055	0.070
F	28.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.98	0.210	0.235
J	10.64	11.15	0.420	0.440
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120

**MTP8N12
MTP8N15****CASE 221A-02
TO-220AB**

DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.95	10.29	0.390	0.405
C	4.00	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
E	3.81	3.73	0.142	0.147
F	2.41	2.67	0.095	0.105
G	2.79	3.30	0.110	0.130
H	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
P	2.54	3.04	0.100	0.120
Q	2.54	3.04	0.100	0.120
R	2.54	3.04	0.100	0.120
S	1.14	1.27	0.045	0.050
T	5.97	6.48	0.235	0.255
U	0.36	0.56	0.014	0.022
V	1.14	1.27	0.045	0.050
W	—	2.03	—	0.080

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	120 150	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 4.0$ Adc) ($I_D = 8.0$ Adc) ($I_D = 4.0$ Adc, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	2.0 4.5 3.2	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 4.0$ Adc)	$r_{DS(on)}$	—	0.5	Ohms
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 4.0$ A)	g_{fs}	2.0	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	650	pF
Output Capacitance		C_{oss}	—	300	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DS} = 25$ V, $I_D = 4.0$ A, $R_{gen} = 50$ ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	100	ns
Fall Time		t_f	—	50	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage ($I_S = 8.0$ A)	V_{SD}	1.7	Vdc
Forward Turn-On Time ($V_{GS} = 0$, $di/dt = 25$ A/ μ s)	t_{on}	80	ns
Reverse Recovery Time (See Figures 15 and 16)	t_{rr}	700	ns

*Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

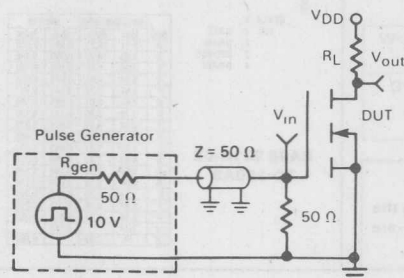
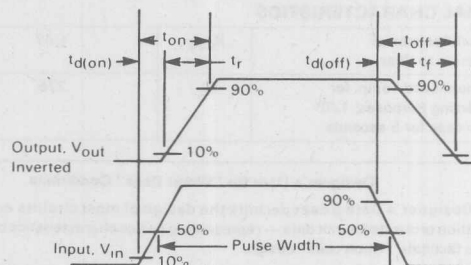


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

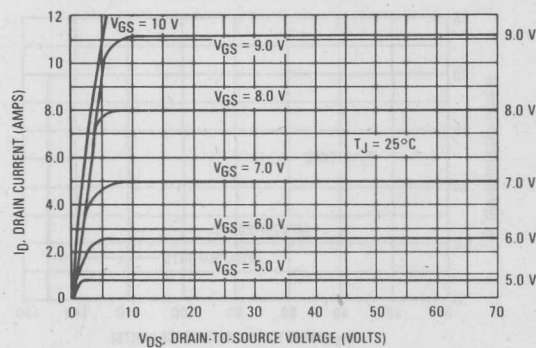


FIGURE 4 — ON-REGION CHARACTERISTICS

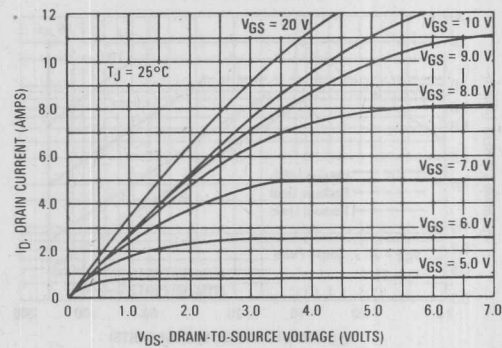


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

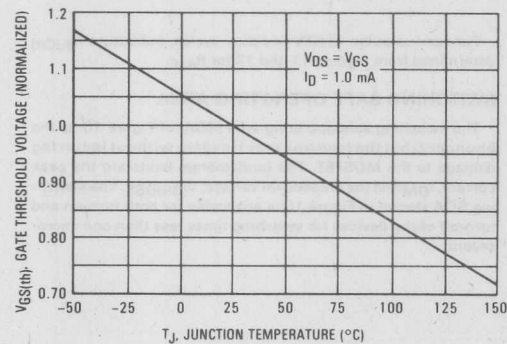


FIGURE 6 — TRANSFER CHARACTERISTICS

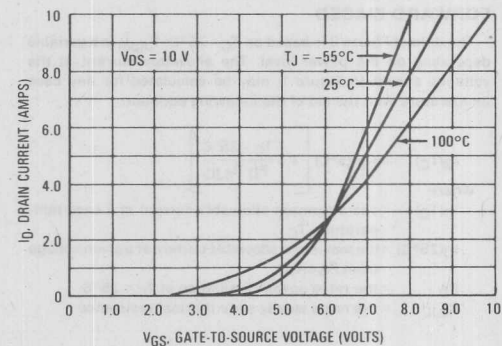


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

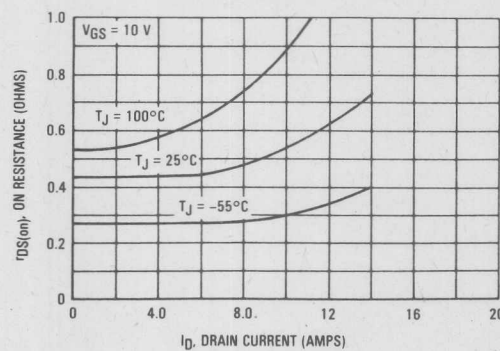
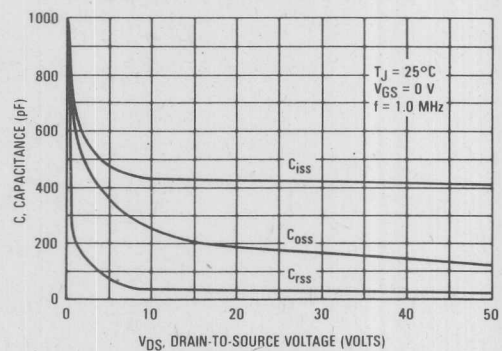


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

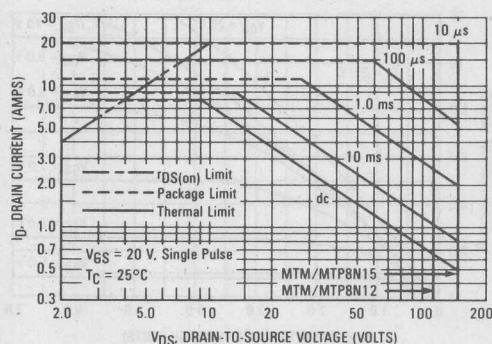
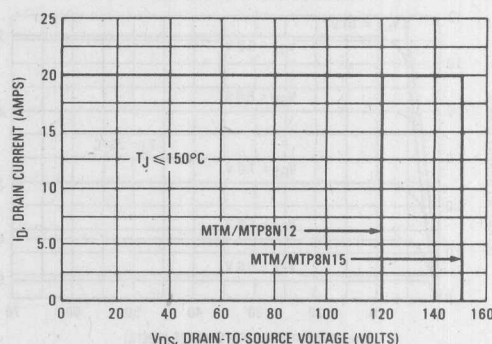


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

THERMAL RESPONSE

FIGURE 11 — MTM8N12/MTM8N15

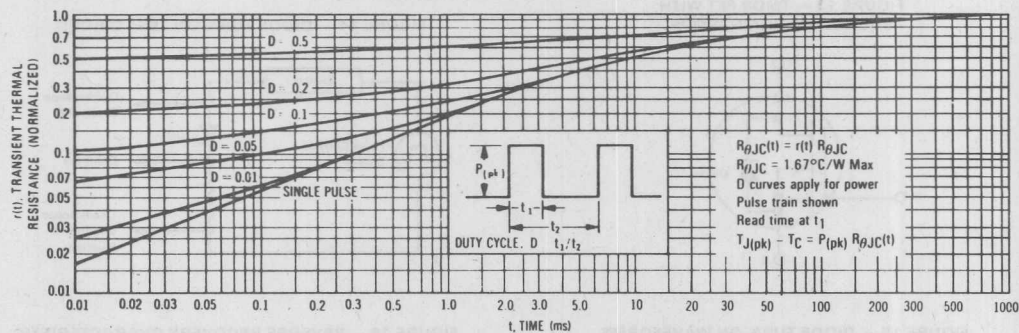
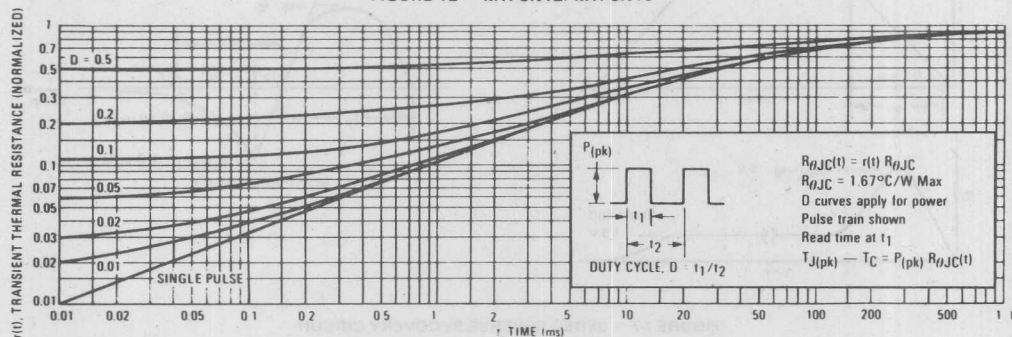


FIGURE 12 — MTP8N12/MTP8N15



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 3.0 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This

FIGURE 13 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

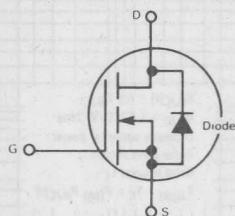
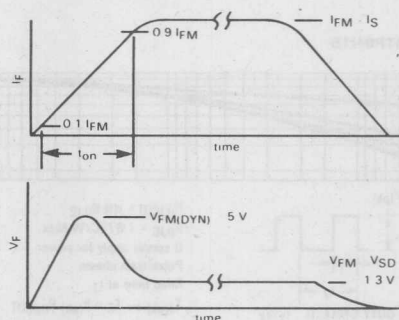


FIGURE 15 — DIODE TURN-ON WAVEFORMS



diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 14 — DIODE TURN-ON TEST CIRCUIT

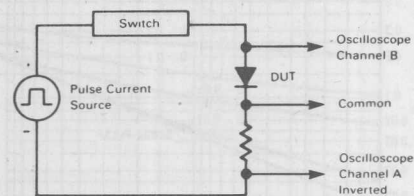


FIGURE 16 — REVERSE RECOVERY CHARACTERISTIC

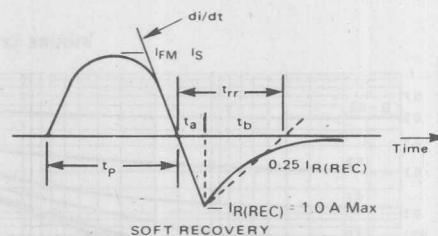
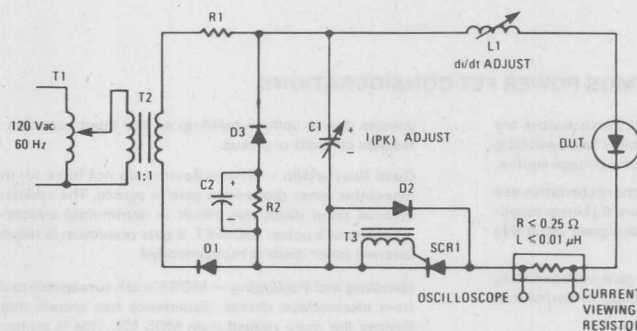


FIGURE 17 — JEDEC REVERSE RECOVERY CIRCUIT



- R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μ F
C2 = 4000 μ F
L1 = 1.0 - 27 mH
T1 = Variac Adjusts I_{PK} and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)


MOTOROLA

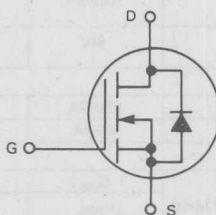
MTM8N18, MTM8N20 MTP8N18, MTP8N20

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS} , $V_{DS(on)}$ SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

Rating	Symbol	MTM8N18 MTP8N18	MTM8N20 MTP8N20	Unit
Drain — Source Voltage	V_{DSS}	180	200	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	180	200	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	8.0		Adc
Pulsed	I_{DM}	25		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75		Watts
		0.6		W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

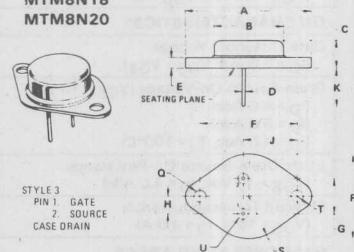
The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

8.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)} = 0.4 \text{ OHM}$
180 and 200 VOLTS

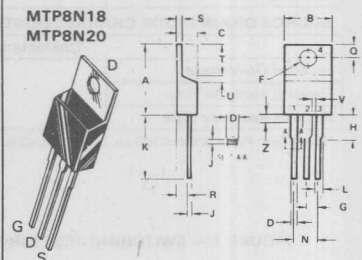
MTM8N18
MTM8N20



CASE 1-04
TO-204
(TO-3 TYPE)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.04	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.54	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120

MTP8N18
MTP8N20



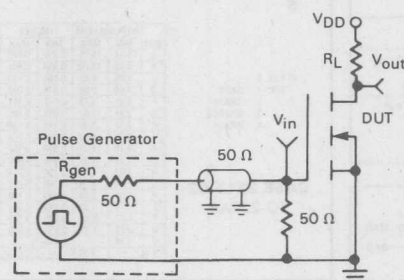
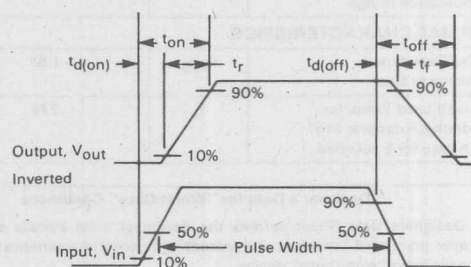
STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-02
TO-220AB

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—
Z	—	2.03	—	0.080

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0\text{ mA}$)	$V_{(BR)DSS}$	180 200	— —	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85\text{ }BV_{DSS}$, $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage ($I_D = 1.0\text{ mA}$, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 4.0\text{ Adc}$) ($I_D = 8.0\text{ Adc}$) ($I_D = 4.0\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	1.6 4.0 3.2	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 4.0\text{ Adc}$)	$r_{DS(on)}$	—	0.4	Ohms
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 4.0\text{ A}$)	g_{fs}	3.0	—	mos
SAFE OPERATING AREAS				
Forward Biased Safe Operating Area	FBSOA	See Figure 12		
Switching Safe Operating Area	SSOA	See Figure 13		
DYNAMIC CHARACTERISTICS				
Input Capacitance	C_{iss}	—	1000	pF
Output Capacitance	C_{oss}	—	300	pF
Reverse Transfer Capacitance	C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)				
Turn-On Delay Time	$t_{d(on)}$	—	40	ns
Rise Time	t_r	—	150	ns
Turn-Off Delay Time	$t_{d(off)}$	—	100	ns
Fall Time	t_f	—	100	ns
SOURCE DRAIN DIODE CHARACTERISTICS*				
Characteristic	Symbol	Typ	Unit	
Forward On-Voltage	V_{SD}	2.0	Vdc	
Forward Turn-On Time	t_{on}	250	ns	
Reverse Recovery Time	t_{rr}	325	ns	

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING****FIGURE 1 — SWITCHING TEST CIRCUIT****FIGURE 2 — SWITCHING WAVEFORMS**

TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

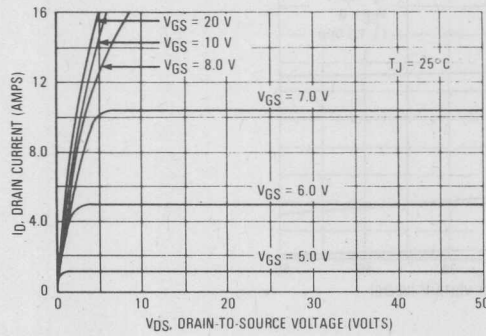


FIGURE 4 — ON-REGION CHARACTERISTICS

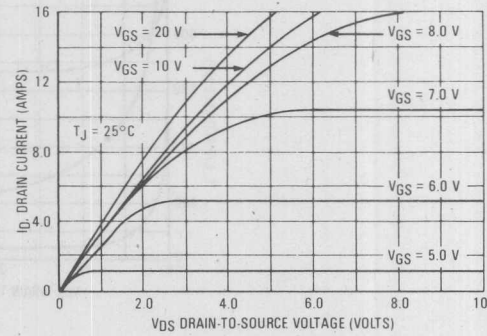


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

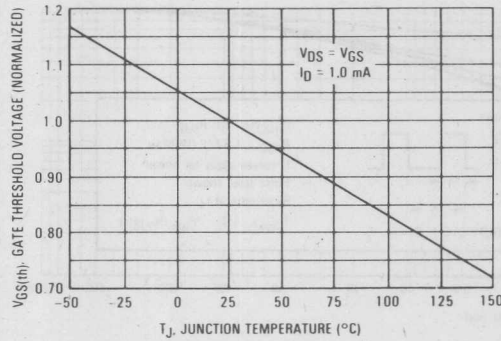


FIGURE 6 — TRANSFER CHARACTERISTICS

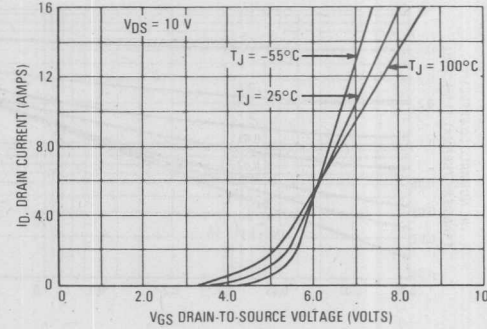


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

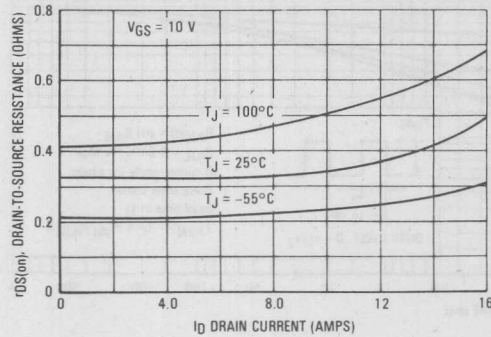
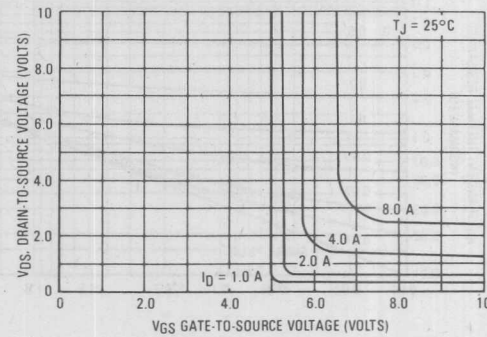
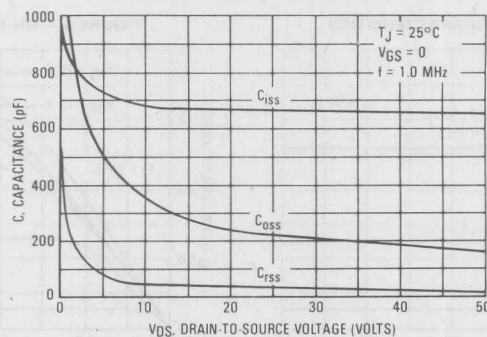


FIGURE 8 — ON-VOLTAGE VARIATION



TYPICAL CHARACTERISTICS

FIGURE 9 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 10 — MTM8N18/MTM8N20

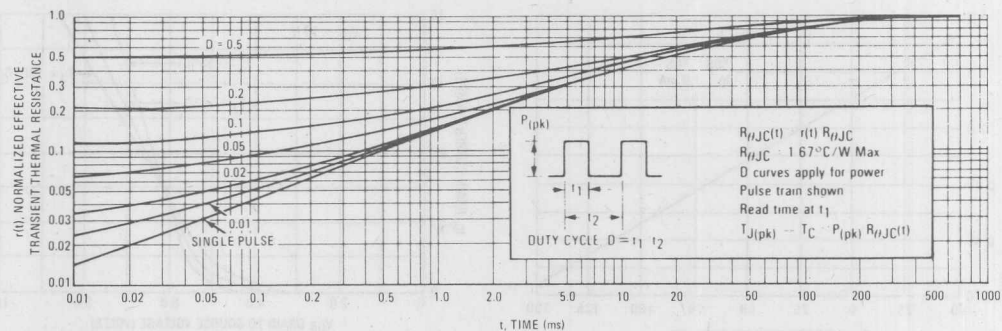
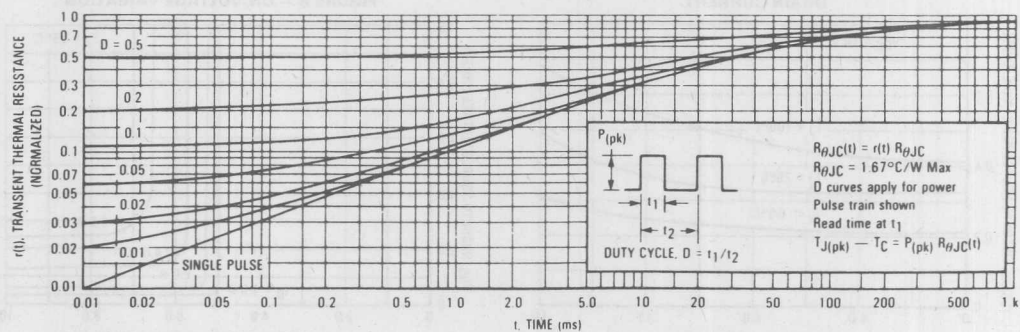


FIGURE 11 — MTP8N18/MTP8N20



SAFE OPERATING AREA INFORMATION

FIGURE 12 — MAXIMUM FORWARD BIASED SAFE OPERATING AREA

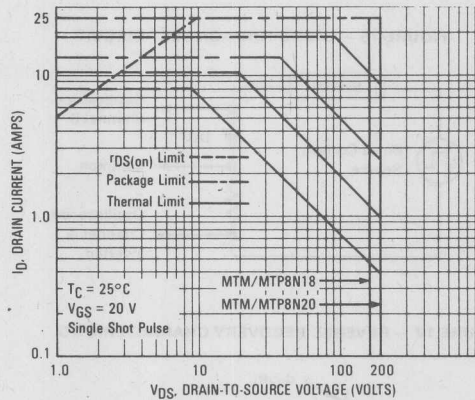
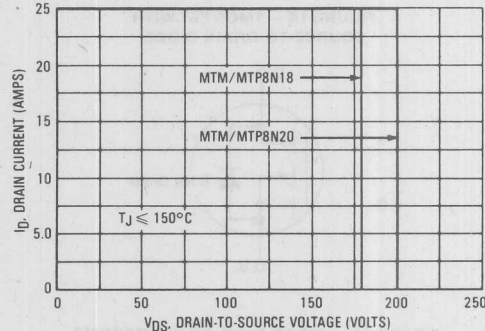


FIGURE 13 — MAXIMUM SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 12 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 12.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC}(t)$ determined from Figures 10 and 11 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 13, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 13 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 2.0 A. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This

diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 14 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

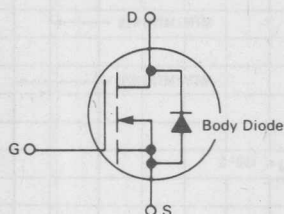


FIGURE 16 — DIODE TURN-ON WAVEFORMS

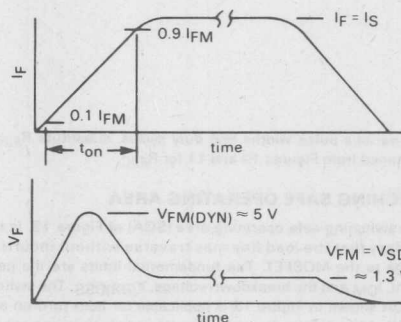


FIGURE 15 — DIODE TURN-ON TEST CIRCUIT

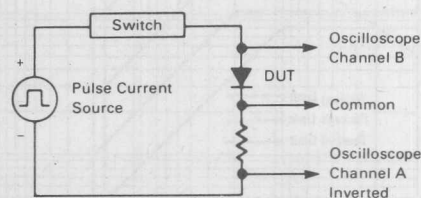


FIGURE 17 — REVERSE RECOVERY CHARACTERISTIC

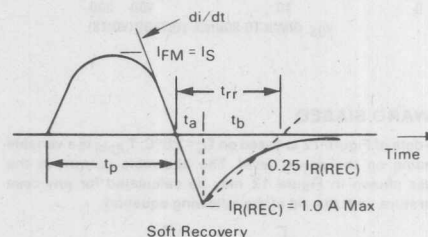
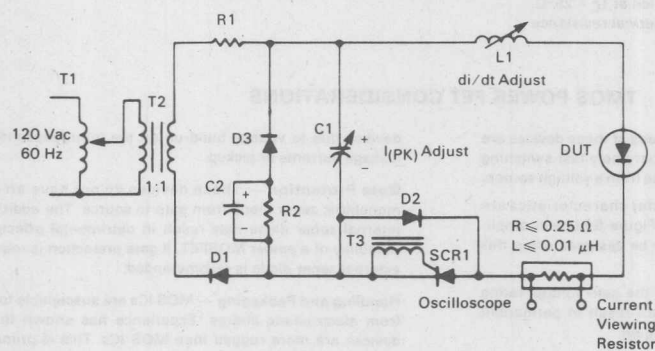


FIGURE 18 — JEDEC REVERSE RECOVERY CIRCUIT

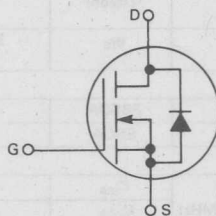


- R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μ F
C2 = 4000 μ F
L1 = 1.0-27 μ H
T1 = Variac Adjusts I_{PK} and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

**MOTOROLA****MTM8N35
MTM8N40****Designer's Data Sheet****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, and converters.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)

**MAXIMUM RATINGS**

Rating	Symbol	MTM8N35	MTM8N40	Unit
Drain — Source Voltage	V_{DSS}	350	400	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ m}\Omega$)	V_{DGR}	350	400	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	8.0		Adc
Pulsed	I_{DM}	40		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150 1.2		Watts W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

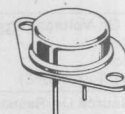
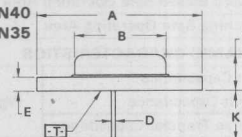
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

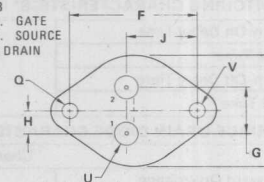
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

8 AMPERE**N-CHANNEL TMOS
POWER FET**

$r_{DS(on)} = 0.8 \text{ OHMS}$
350 and 400 VOLTS

**MTM8N40
MTM8N35**

STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

**NOTES:**

1. DIMENSIONS Q AND V ARE DATUMS.
2. \square IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\phi \pm 0.13 (0.005) \text{ M T V } \phi$$

FOR LEADS:

$$\phi \pm 0.13 (0.005) \text{ M T V } \phi \text{ Q } \phi$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

**CASE 1-05
TO-3**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0\text{ mA}$)	$V_{(BR)DSS}$	350 400	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0\text{ mA}$, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 4.0\text{ Adc}$) ($I_D = 8.0\text{ Adc}$) ($I_D = 4.0\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	3.2 8.0 5.6	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 4.0\text{ Adc}$)	$r_{DS(on)}$	—	0.8	Ohms
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 4.0\text{ A}$)	g_{fs}	3.0	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{iss}	—	1800	pF
Output Capacitance		C_{oss}	—	350	pF
Reverse Transfer Capacitance		C_{rss}	—	150	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DS} = 125\text{ V}$, $I_D = 4.0\text{ A}$, $R_{gen} = 50\text{ ohms}$)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	120	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	$I_S = 8.0\text{ A}$ $V_{GS} = 0, di/dt = 25\text{ A}/\mu\text{s}$ See Figures 14 and 15	V_{SD}	1.0	Vdc
Forward Turn-On Time		t_{on}	175	ns
Reverse Recovery Time		t_{rr}	600	ns

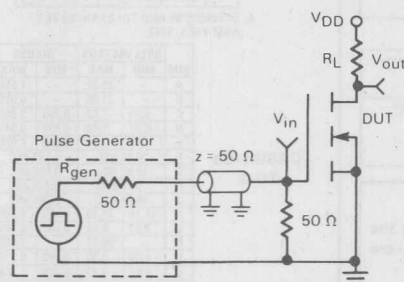
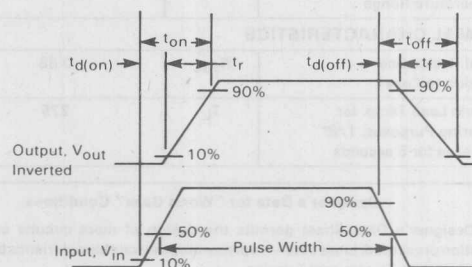
*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING****FIGURE 1 — SWITCHING TEST CIRCUIT****FIGURE 2 — SWITCHING WAVEFORMS**

FIGURE 3 — OUTPUT CHARACTERISTICS

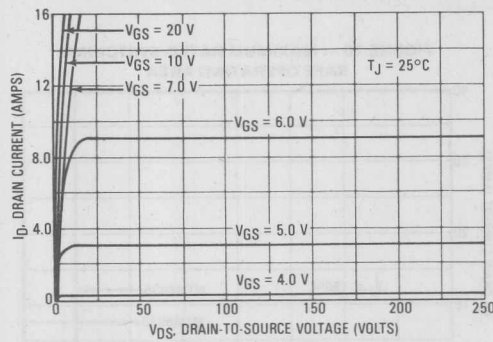


FIGURE 4 — ON-REGION CHARACTERISTICS

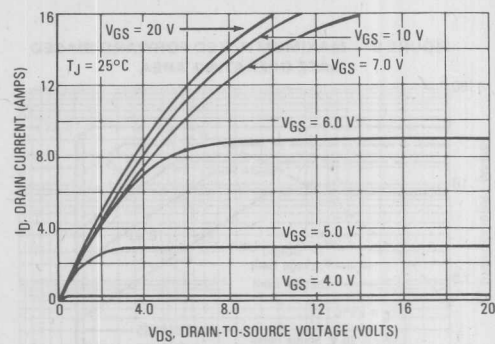


FIGURE 5 — GATE THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

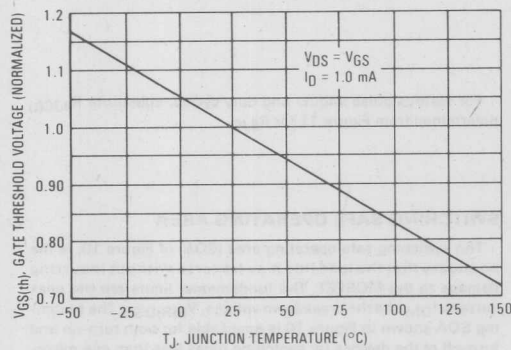


FIGURE 6 — TRANSFER CHARACTERISTICS

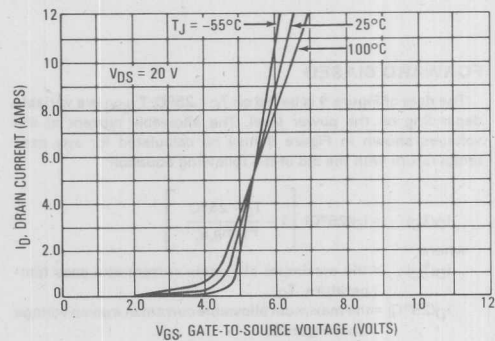


FIGURE 7 — ON RESISTANCE versus DRAIN CURRENT

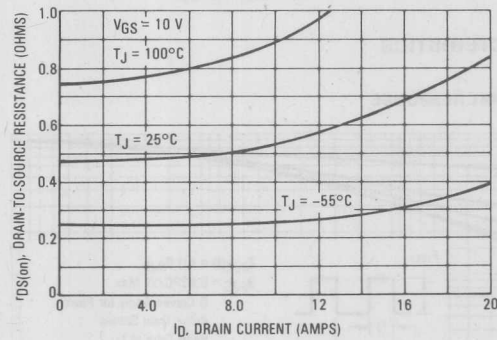
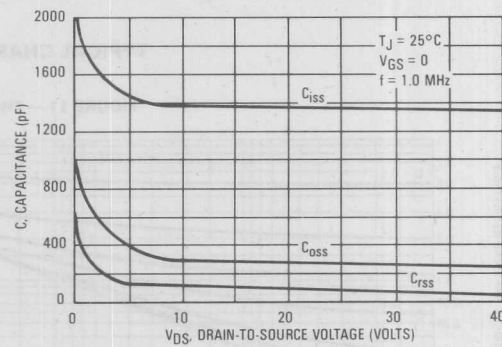


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

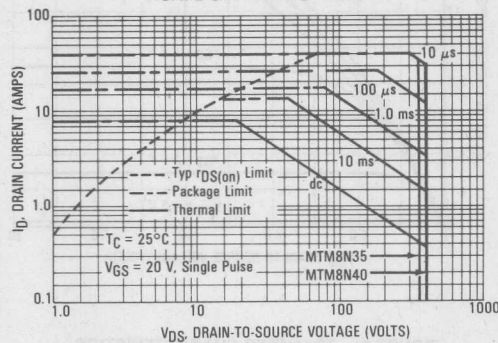
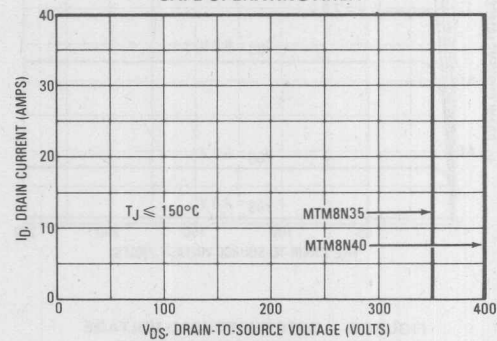


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

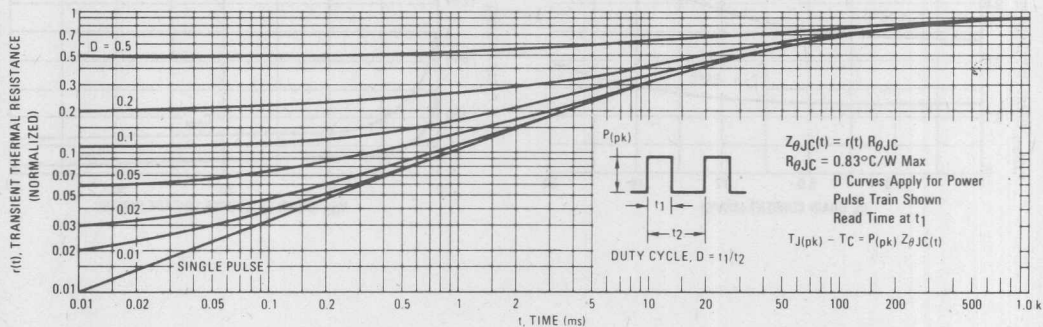
For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figure 11 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

TYPICAL CHARACTERISTICS

FIGURE 11 — THERMAL RESPONSE



TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 11. Reversal of the drain voltage will cause current flow in the reverse direction. This

FIGURE 12 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

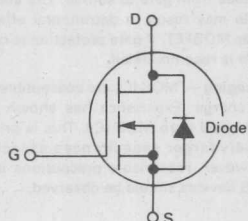
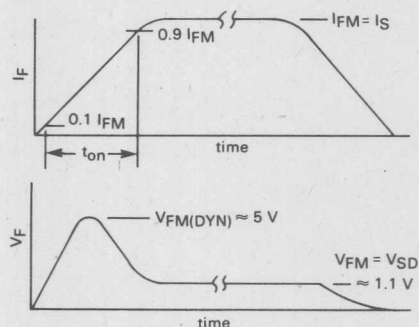


FIGURE 14 — DIODE TURN-ON WAVEFORMS



diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 13 — DIODE TURN-ON TEST CIRCUIT

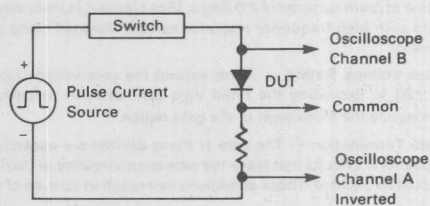


FIGURE 15 — REVERSE RECOVERY CHARACTERISTIC

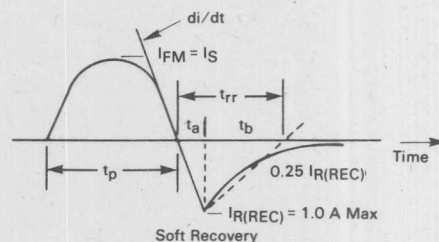
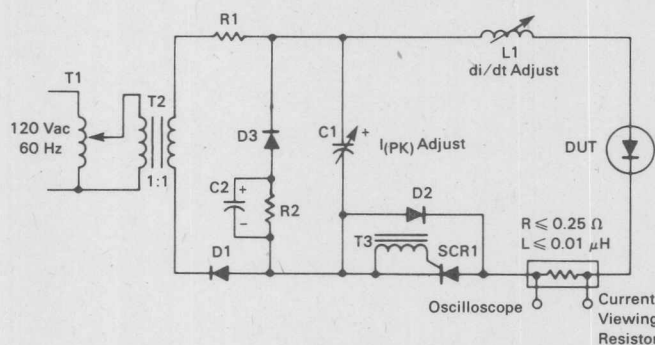


FIGURE 16 — JEDEC REVERSE RECOVERY CIRCUIT



- R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μ F
C2 = 4000 μ F
L1 = 1.0-27 μ H
T1 = Variac Adjusts I_{PK} and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 2.0 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

FIGURE 10 — TRANSFER CHARACTERISTICS

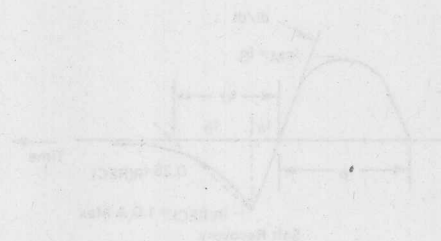


FIGURE 11 — DRAIN CURRENT REGULATION

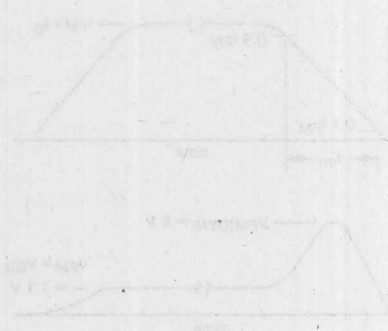
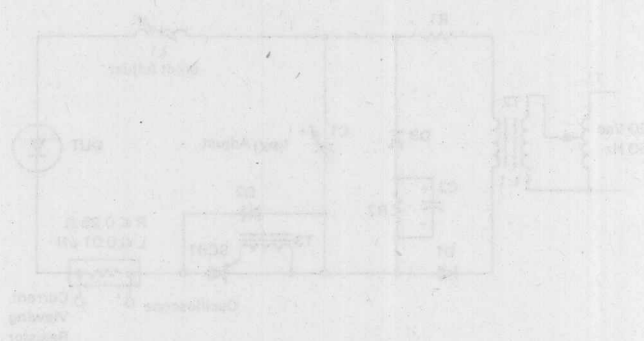


FIGURE 12 — THERMAL RECOVERY CHARACTERISTICS





MOTOROLA

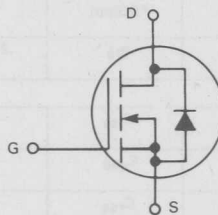
MTM10N05, MTM10N06 MTP10N05, MTP10N06

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

Rating	Symbol	MTM10N05 MTP10N05	MTM10N06 MTP10N06	Unit
Drain — Source Voltage	V_{DSS}	50	60	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	50	60	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	10		Adc
Pulsed	I_{DM}	28		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75		Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

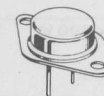
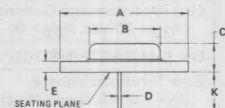
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

10 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)} = 0.28 \text{ OHM}$
50 and 60 VOLTS

MTM10N05
MTM10N06



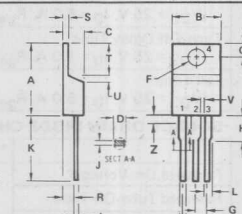
STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MIN	MAX	MIN	MAX
A	—	38.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.039	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120

CASE 1-04
TO-3 TYPE

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH
REFERENCED TO-3 OUTLINE SHALL APPLY.

MTP10N05
MTP10N06



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONS L AND H APPLIES TO ALL LEADS.
2. DIMENSION Z DEFINES A ZONE WHERE ALL
BODY AND LEAD IRREGULARITIES ARE
ALLOWED.
3. DIMENSIONING AND TOLERANCING PER ANSI
Y14.5 1973.
4. CONTROLLING DIMENSION: INCH

DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.68	4.82	0.180	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.63	5.33	0.180	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—
Z	—	2.03	—	0.080

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	50 60	— —	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 5.0$ Adc) ($I_D = 10$ Adc) ($I_D = 5.0$ Adc, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	1.4 3.4 2.8	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 5.0$ Adc)	$r_{DS(on)}$	—	0.28	Ohms
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 5.0$ A)	g_{fs}	2.5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	400	pF
Output Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{oss}	—	350	pF
Reverse Transfer Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{rss}	—	100	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time ($V_{DS} = 25$ V, $I_D = 5.0$ A, $R_{gen} = 50$ ohms)	$t_{d(on)}$	—	50	ns
Rise Time ($V_{DS} = 25$ V, $I_D = 5.0$ A, $R_{gen} = 50$ ohms)	t_r	—	120	ns
Turn-Off Delay Time ($V_{DS} = 25$ V, $I_D = 5.0$ A, $R_{gen} = 50$ ohms)	$t_{d(off)}$	—	50	ns
Fall Time ($V_{DS} = 25$ V, $I_D = 5.0$ A, $R_{gen} = 50$ ohms)	t_f	—	60	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage $I_S = 10$ A	V_{SD}	2.0	Vdc
Forward Turn-On Time $V_{GS} = 0$	t_{on}	200	ns
Reverse Recovery Time See Figure 16 and 17.	t_{rr}	300	ns

*Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

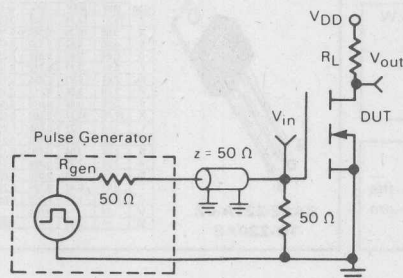
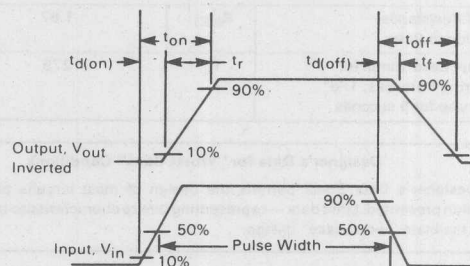


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

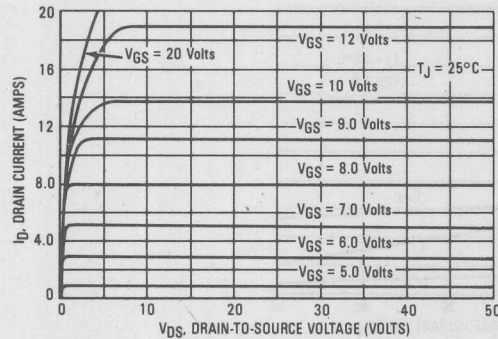


FIGURE 4 — ON-REGION CHARACTERISTICS

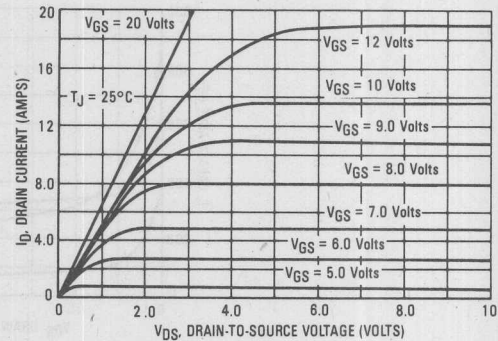


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

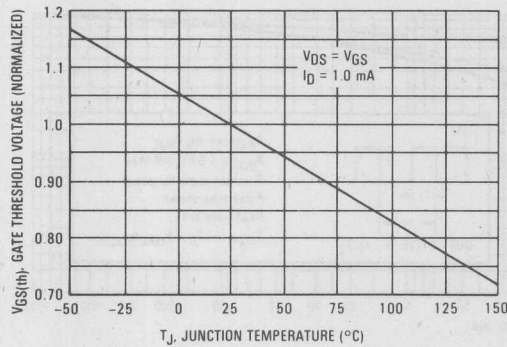


FIGURE 6 — TRANSFER CHARACTERISTICS

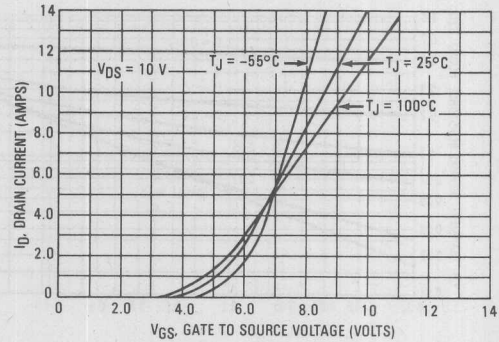


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

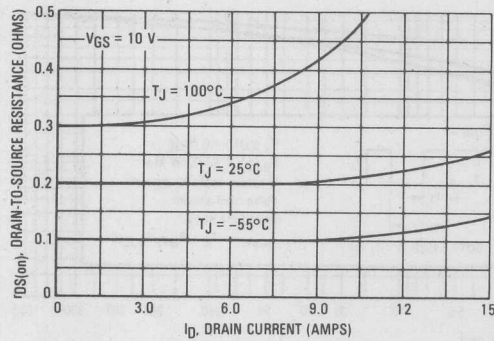
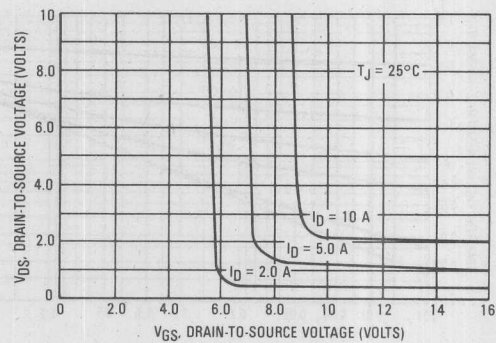
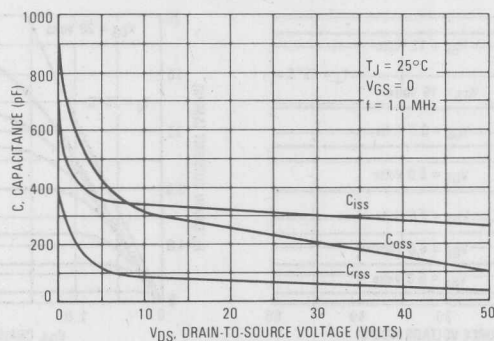


FIGURE 8 — ON-VOLTAGE VARIATION



TYPICAL CHARACTERISTICS

FIGURE 9 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 10 — MTM10N05/MTM10N06

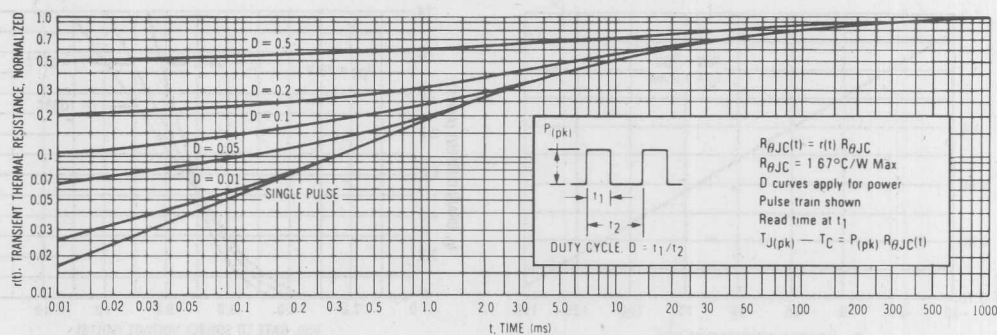
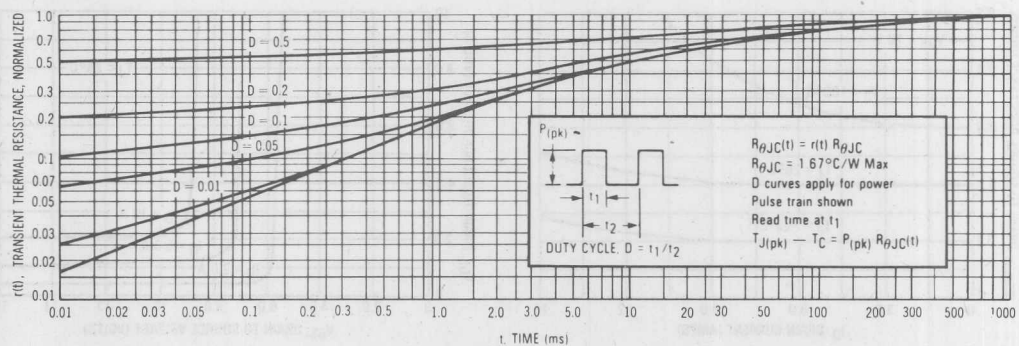


FIGURE 11 — MTP10N05/MTP10N06



SAFE OPERATING AREA INFORMATION

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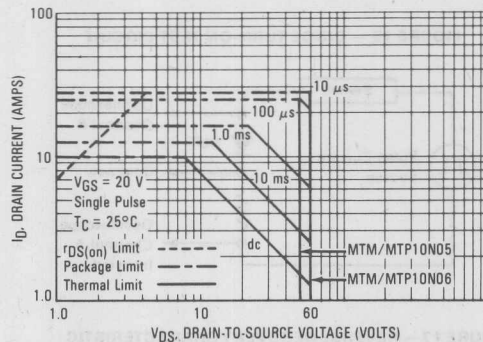
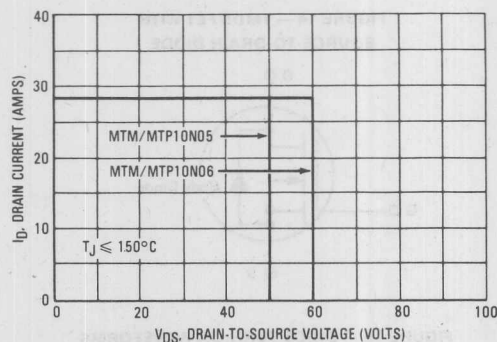


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$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 12.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 10 and 11 for $R_{\theta JC}$.

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Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

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FIGURE 14 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

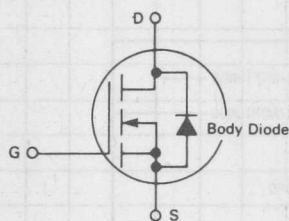


FIGURE 16 — DIODE TURN-ON WAVEFORMS

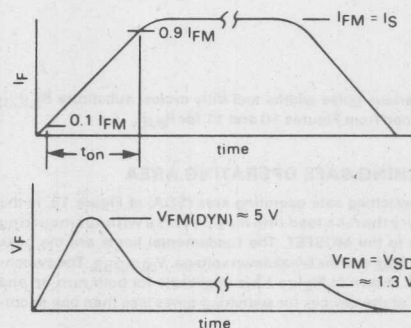


FIGURE 15 — DIODE TURN-ON TEST CIRCUIT

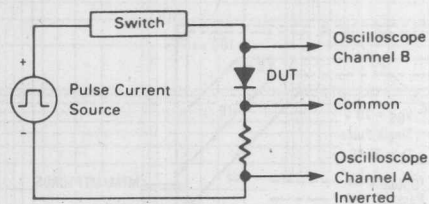


FIGURE 17 — REVERSE RECOVERY CHARACTERISTIC

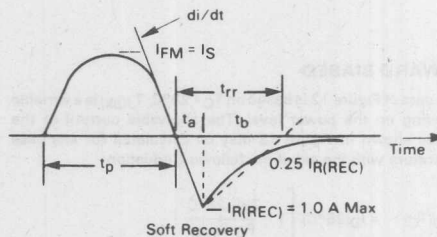
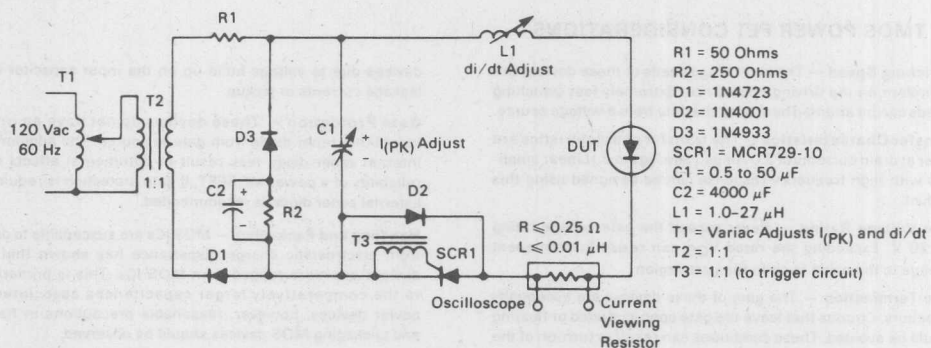


FIGURE 18 — JEDEC REVERSE RECOVERY CIRCUIT





MOTOROLA

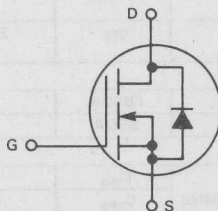
MTM10N08 MTM10N10 MTP10N08 MTP10N10

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- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

Rating	Symbol	MTM10N08 MTP10N08	MTM10N10 MTP10N10	Unit
Drain — Source Voltage	V_{DSS}	80	100	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	80	100	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	10		Adc
Pulsed	I_{DM}	25		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

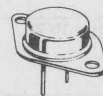
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

10 AMPERE

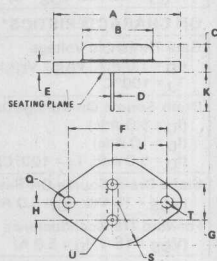
N-CHANNEL TMOS POWER FET

$r_{DS(on)} = 0.33 \text{ OHM}$
80 and 100 VOLTS

MTM10N08
MTM10N10



STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN



NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

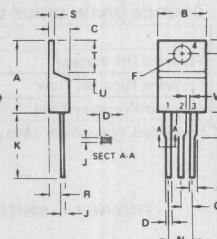
CASE 1-04
TO-3 TYPE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	35.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.02	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120

MTP10N08
MTP10N10



STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



CASE 221A-02
TO-220AB

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
E	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.38	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	80 100	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 5.0$ Adc) ($I_D = 10$ Adc) ($I_D = 5.0$ Adc, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	1.65 4.0 3.3	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 5.0$ Adc)	$r_{DS(on)}$	—	0.33	Ohms
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 5.0$ A)	g_{fs}	2.5	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	600	pF
Output Capacitance		C_{oss}	—	400	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DS} = 25$ V, $I_D = 5.0$ A, $R_{gen} = 50$ ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	100	ns
Fall Time		t_f	—	50	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage	V_{SD}	2.0	Vdc
Forward Turn-On Time	t_{on}	80	ns
Reverse Recovery Time	t_{rr}	700	ns

*Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

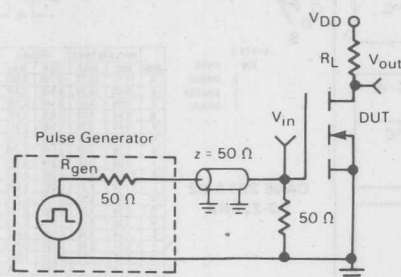
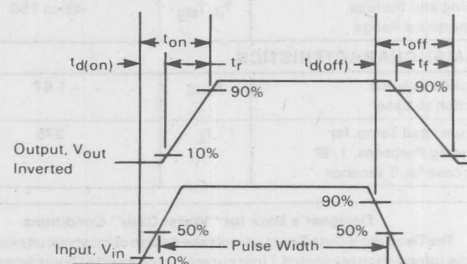


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

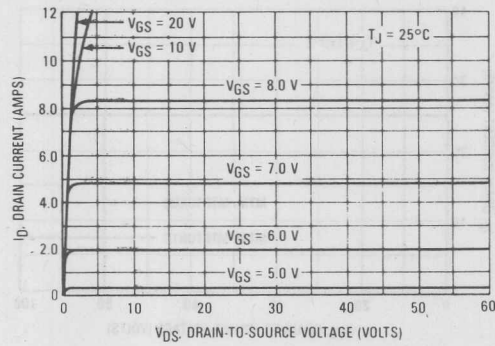


FIGURE 4 — ON-REGION CHARACTERISTICS

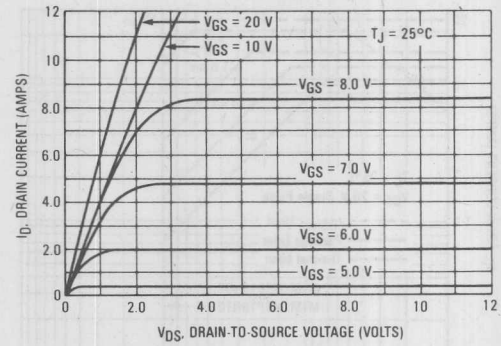


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

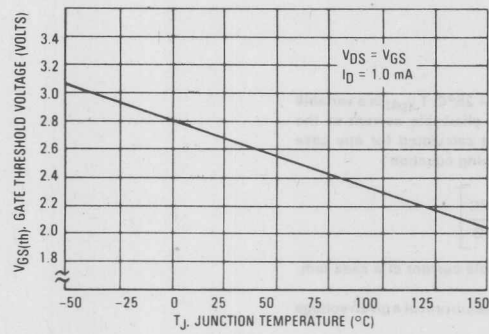


FIGURE 6 — TRANSFER CHARACTERISTICS

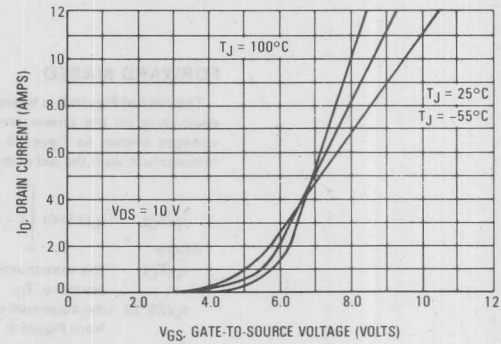


FIGURE 7 — $r_{DS(on)}$, ON-RESISTANCE versus DRAIN CURRENT

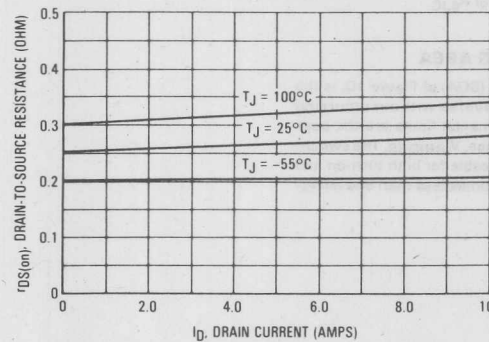
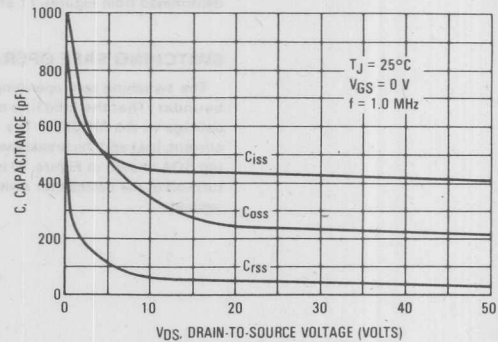


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

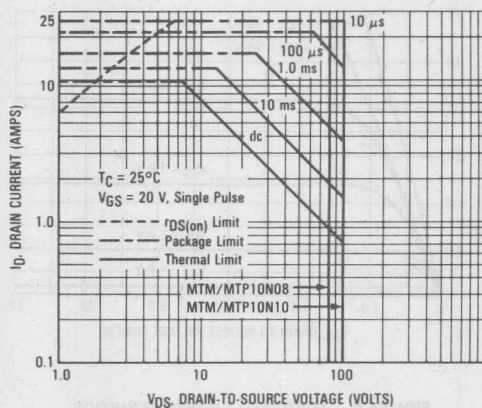
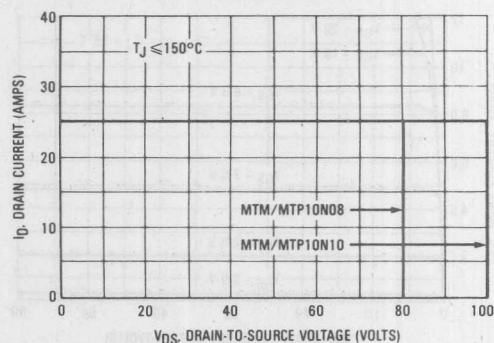


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

THERMAL RESPONSE

FIGURE 11 — MTM10N08/10N10

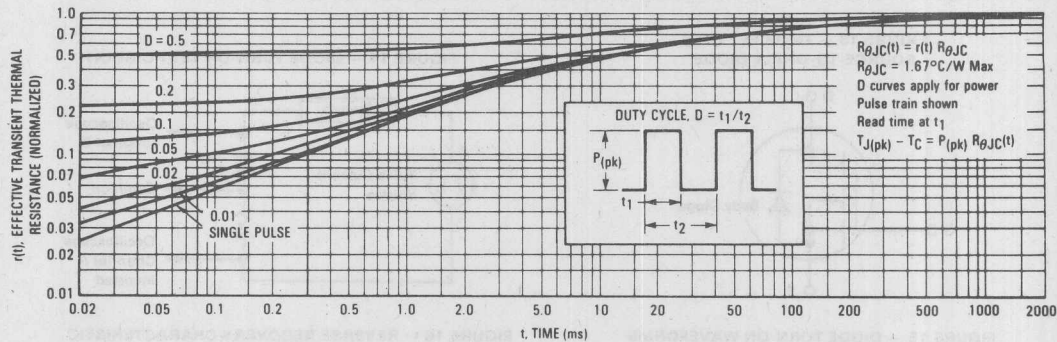
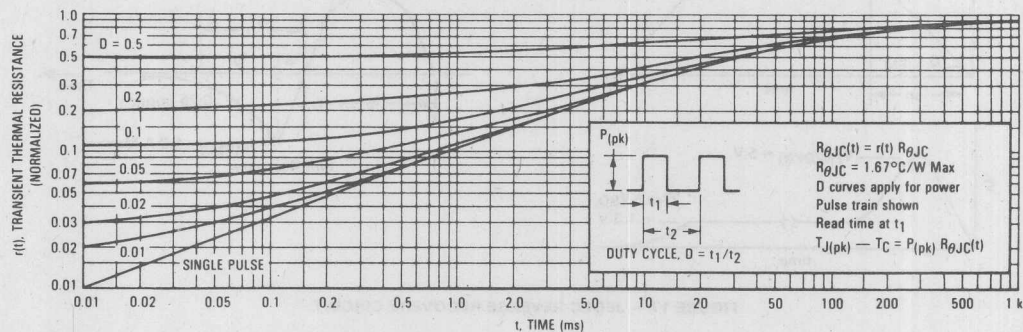


FIGURE 12 — MTP10N08/10N10



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 1.0 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This

diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 13 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

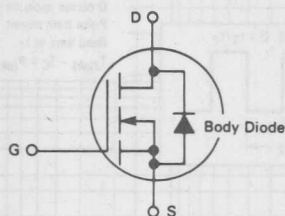


FIGURE 15 — DIODE TURN-ON WAVEFORMS

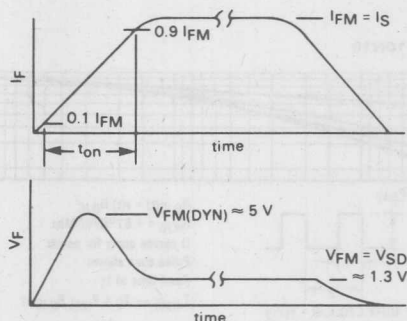


FIGURE 14 — DIODE TURN-ON TEST CIRCUIT

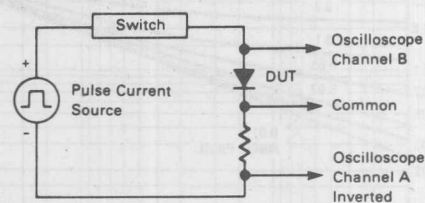


FIGURE 16 — REVERSE RECOVERY CHARACTERISTIC

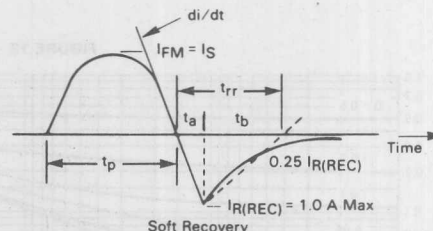
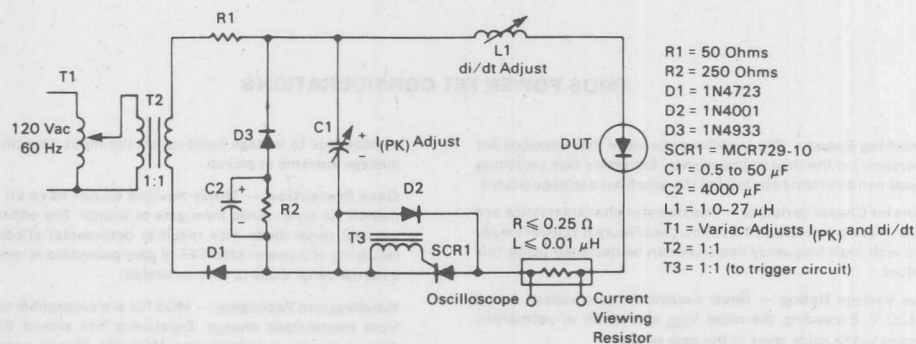


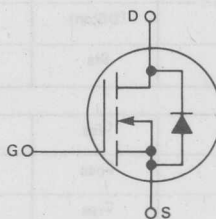
FIGURE 17 — JEDEC REVERSE RECOVERY CIRCUIT



**MOTOROLA****MTM10N12, MTM10N15
MTP10N12, MTP10N15****Designer's Data Sheet****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS} , $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads

**MAXIMUM RATINGS**

Rating	Symbol	MTM10N12 MTP10N12	MTM10N15 MTP10N15	Unit
Drain — Source Voltage	V_{DSS}	120	150	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	120	150	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current				Adc
Continuous	I_D	10		
Pulsed	I_{DM}	28		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power	P_D			Watts
Dissipation @ $T_C = 25^\circ\text{C}$		75		
Derate above 25°C		0.6		W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

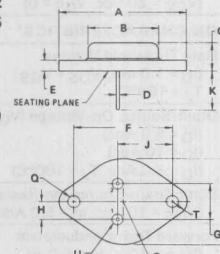
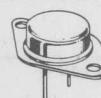
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

10 AMPERE**N-CHANNEL TMOS
POWER FET**

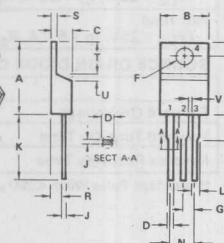
$r_{DS(on)} = 0.3 \text{ OHM}$
120 and 150 VOLTS

**MTM10N12
MTM10N15**

STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MIN	MAX	MIN	MAX
A	—	38.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	10.64	11.15	0.420	0.440
K	11.18	12.15	0.440	0.480
R	3.81	4.19	0.150	0.165
S	—	26.67	—	1.050
T	2.54	3.05	0.100	0.120

CASE 1-04
TO-3 TYPE

**MTP10N12
MTP10N15**

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
E	3.61	3.73	0.142	0.147
F	2.41	2.67	0.095	0.105
G	2.79	3.30	0.110	0.130
H	0.36	0.56	0.014	0.022
J	12.70	14.27	0.500	0.562
K	1.14	1.27	0.045	0.050
L	4.83	5.33	0.190	0.210
M	2.54	3.04	0.100	0.120
N	2.04	2.79	0.080	0.110
O	1.14	1.39	0.045	0.055
P	5.97	6.48	0.235	0.255
Q	0.76	1.27	0.030	0.050
R	1.14	—	0.045	—

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	120 150	— —	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^{\circ}\text{C}$	I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$) $T_J = 100^{\circ}\text{C}$	V_{GS}	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 5.0$ Adc) ($I_D = 10$ Adc) ($I_D = 5.0$ Adc, $T_J = 100^{\circ}\text{C}$)	$V_{DS(on)}$	— — —	1.5 3.0 2.5	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 5.0$ Adc)	$r_{DS(on)}$	—	0.3	Ohms
Forward Transconductance ($V_{DS} = 10$ V, $I_D = 5.0$ A)	g_{fs}	2.5	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	1200	pF
Output Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{oss}	—	500	pF
Reverse Transfer Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{rss}	—	120	pF
SWITCHING CHARACTERISTICS* ($T_J = 100^{\circ}\text{C}$)				
Turn-On Delay Time ($V_{DS} = 25$ V, $I_D = 5.0$ A, $R_{gen} = 50$ ohms)	$t_{d(on)}$	—	50	ns
Rise Time ($V_{DS} = 25$ V, $I_D = 5.0$ A, $R_{gen} = 50$ ohms)	t_r	—	180	ns
Turn-Off Delay Time ($V_{DS} = 25$ V, $I_D = 5.0$ A, $R_{gen} = 50$ ohms)	$t_{d(off)}$	—	200	ns
Fall Time ($V_{DS} = 25$ V, $I_D = 5.0$ A, $R_{gen} = 50$ ohms)	t_f	—	100	ns
SOURCE DRAIN DIODE CHARACTERISTICS*				
Characteristic		Symbol	Typ	Unit
Forward On-Voltage	$I_S = 10$ A $V_{GS} = 0$, $di/dt = 25$ A/ μ s See Figures 17 and 18	V_{SD}	1.3	Vdc
Forward Turn-On Time		t_{on}	250	ns
Reverse Recovery Time		t_{rr}	325	ns

*Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

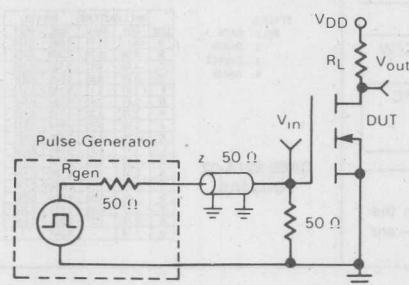
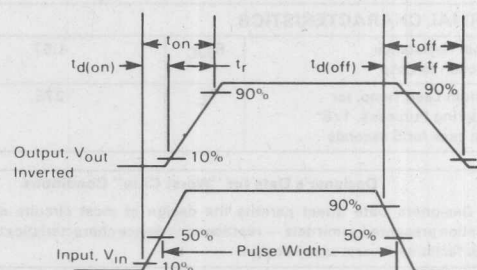


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

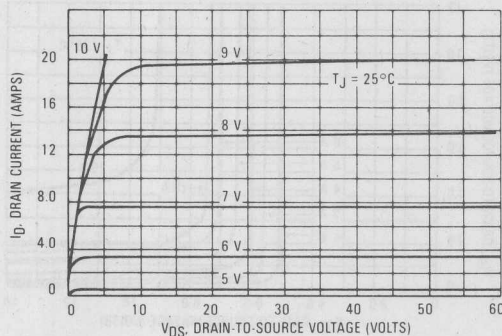


FIGURE 4 — ON-REGION CHARACTERISTICS

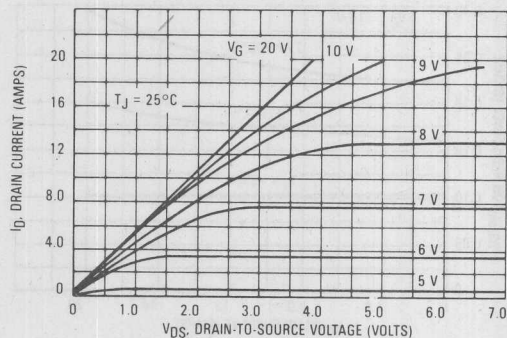


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

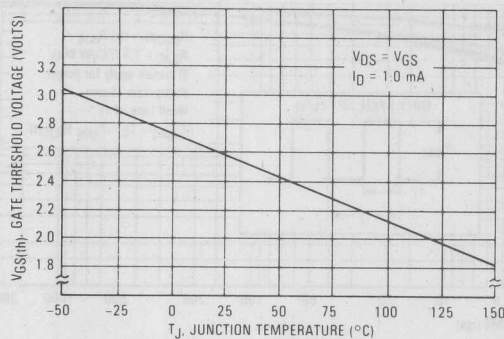


FIGURE 6 — TRANSFER CHARACTERISTICS

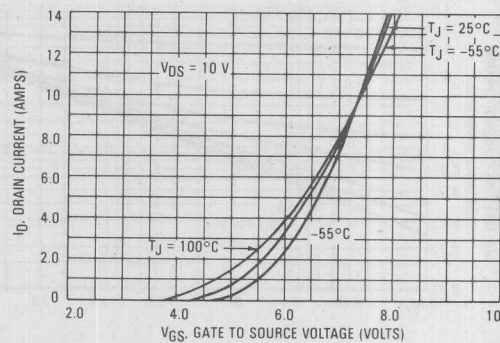


FIGURE 7 — ON-VOLTAGE VARIATION versus TEMPERATURE

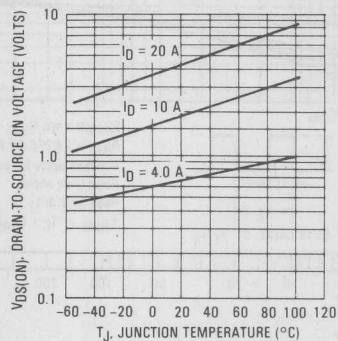
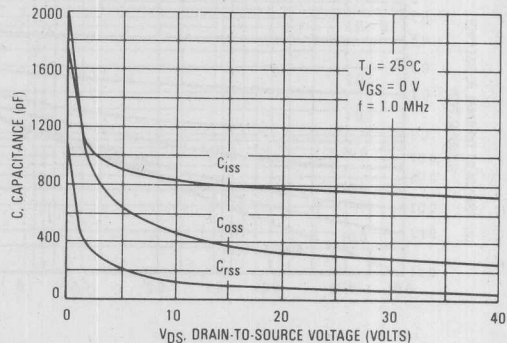


FIGURE 8 — CAPACITANCE VARIATION



TYPICAL CHARACTERISTICS

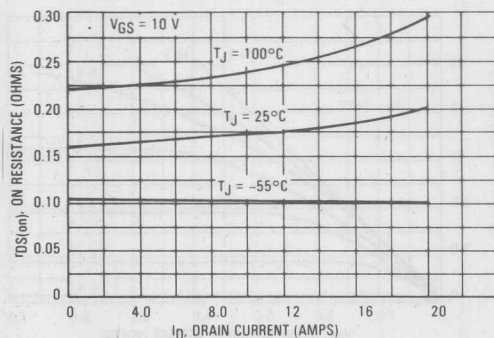
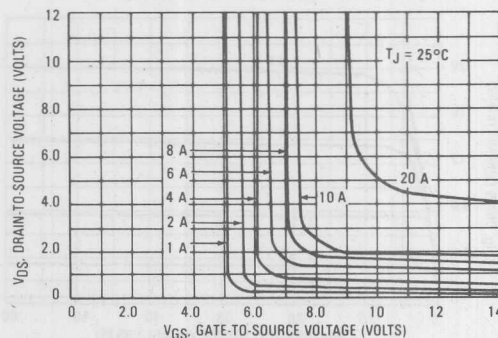
FIGURE 9 — ON-RESISTANCE versus
DRAIN CURRENT


FIGURE 10 — ON-VOLTAGE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM10N12/MTM10N15

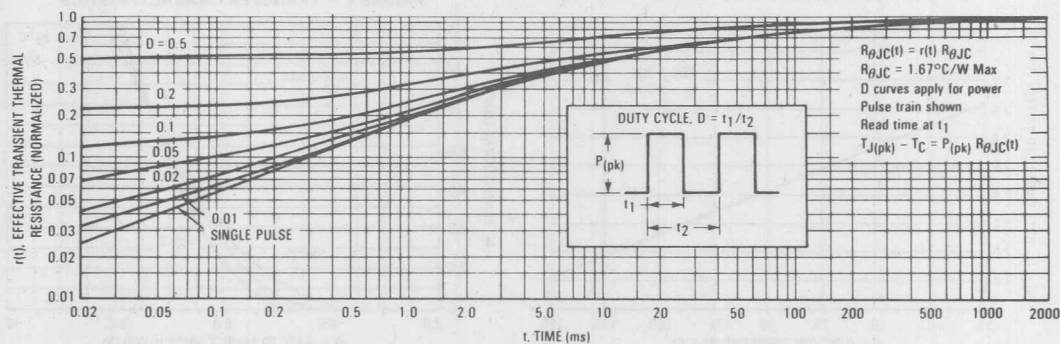
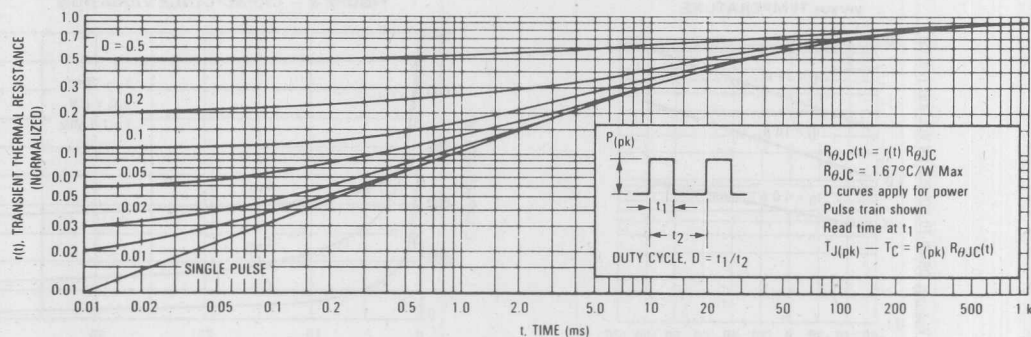
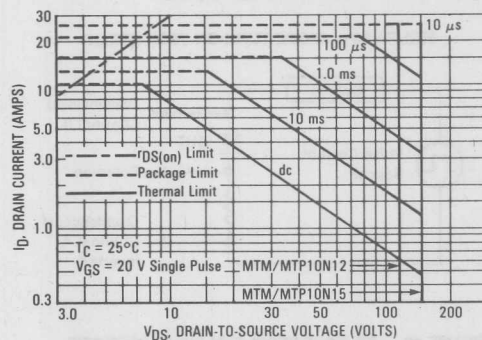


FIGURE 12 — MTP10N12/MTP10N15



SAFE OPERATING AREA INFORMATION

FIGURE 13 — MAXIMUM RATED FORWARD BIAS
SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 13 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

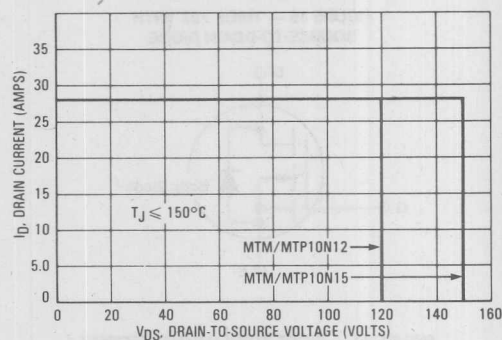
$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 13.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

FIGURE 14 — MAXIMUM RATED SWITCHING
SAFE OPERATING AREA



For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on

of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse di-

FIGURE 15 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

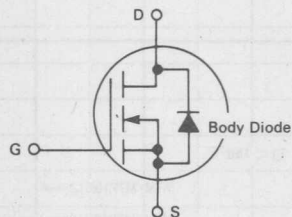
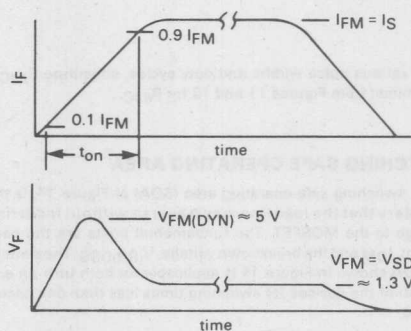


FIGURE 17 — DIODE TURN-ON WAVEFORMS



rection. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 16 — DIODE TURN-ON TEST CIRCUIT

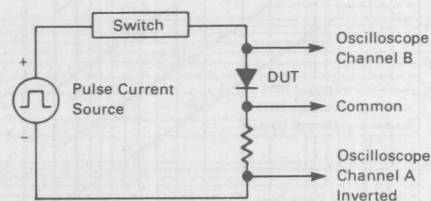


FIGURE 18 — REVERSE RECOVERY CHARACTERISTIC

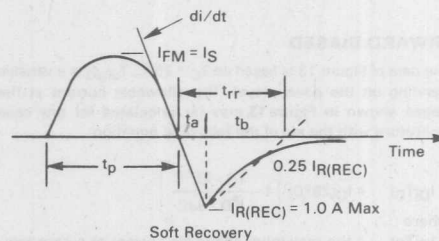
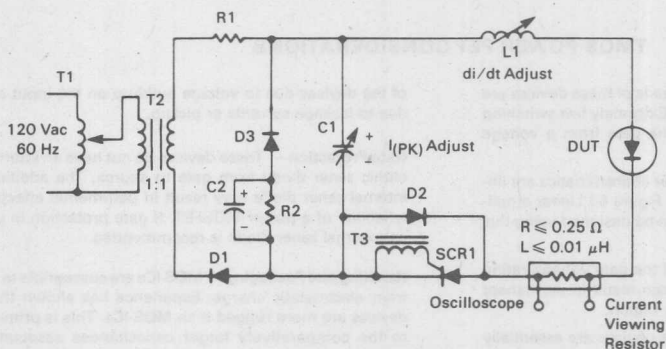


FIGURE 19 — JEDEC REVERSE RECOVERY CIRCUIT



- R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μ F
C2 = 4000 μ F
L1 = 1.0-27 μ H
T1 = Variac Adjusts I_{PK} and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)



MOTOROLA

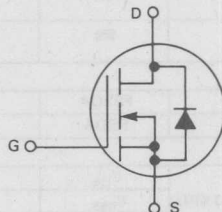
MTM12N05, MTM12N06 MTP12N05, MTP12N06

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)



MAXIMUM RATINGS

Rating	Symbol	MTM12N05 MTP12N05	MTM12N06 MTP12N06	Unit
Drain — Source Voltage	V_{DSS}	50	60	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0$ M Ω)	V_{DGR}	50	60	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	12		Adc
Pulsed	I_{DM}	30		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6		Watts W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

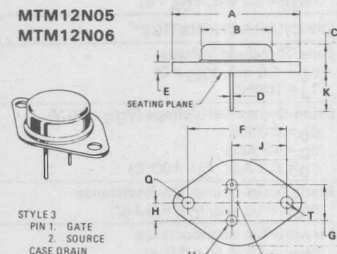
The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

12 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)} = 0.2$ OHM
50 and 60 VOLTS

MTM12N05
MTM12N06

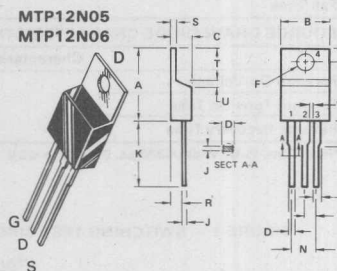


STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.37	—	1.550	—
B	21.08	—	0.830	—
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.80	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.84	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	26.67	—	1.050	—
U	2.54	3.05	0.100	0.120

USE CASE
1-04 TO-3
TYPE OUTLINE

MTP12N05
MTP12N06



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.81	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.38	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0\text{ mA}$)	$V_{(BR)DSS}$	50 60	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85\text{ Rated } V_{DSS}$, $V_{GS} = 0$, $T_J = 100^\circ\text{C}$)	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0\text{ mA}$, $V_{DS} = 0$, $T_J = 100^\circ\text{C}$)	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 6.0\text{ Adc}$) ($I_D = 12\text{ Adc}$) ($I_D = 6.0\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	1.2 3.2 2.4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 6.0\text{ Adc}$)	$r_{DS(on)}$	—	0.2	Ohms
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 6.0\text{ A}$)	g_{fs}	3.0	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{iss}	—	800	pF
Output Capacitance		C_{oss}	—	700	pF
Reverse Transfer Capacitance		C_{rss}	—	160	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DS} = 25\text{ V}$, $I_D = 6.0\text{ A}$, $R_{gen} = 50\text{ ohms}$)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	160	ns
Turn-Off Delay Time		$t_{d(off)}$	—	80	ns
Fall Time		t_f	—	110	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage	V_{SD}	2.0	Vdc
Forward Turn-On Time	t_{on}	80	ns
Reverse Recovery Time	t_{rr}	700	ns

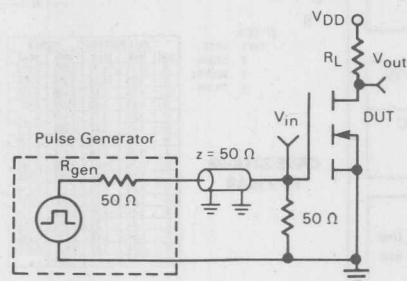
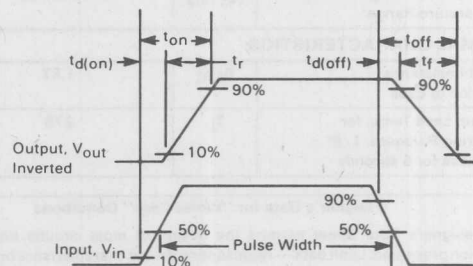
*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING****FIGURE 1 — SWITCHING TEST CIRCUIT****FIGURE 2 — SWITCHING WAVEFORMS**

FIGURE 3 — OUTPUT CHARACTERISTICS

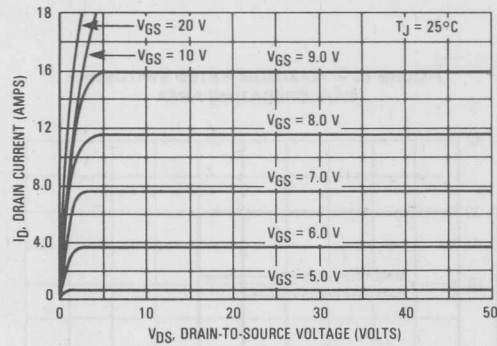


FIGURE 4 — ON-REGION CHARACTERISTICS

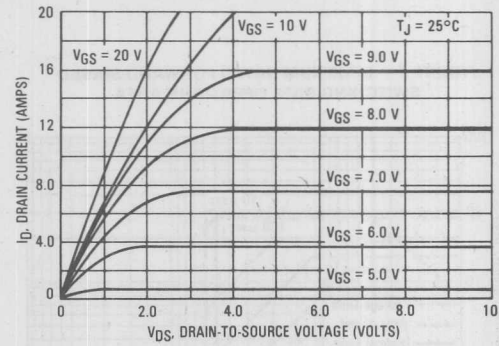


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

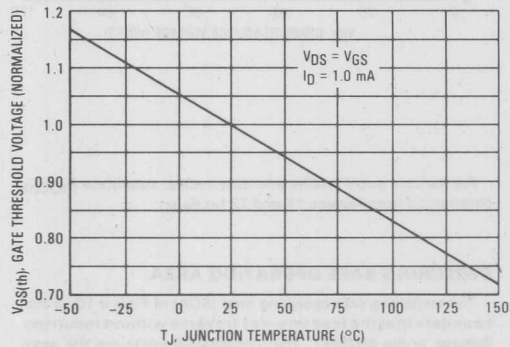


FIGURE 6 — TRANSFER CHARACTERISTICS

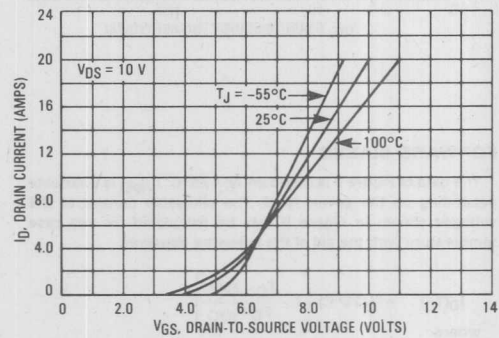


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

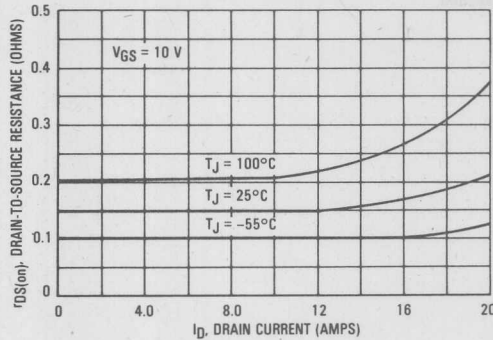
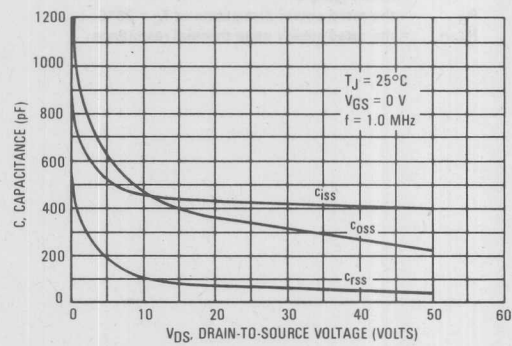


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SWITCHING SAFE OPERATING AREA

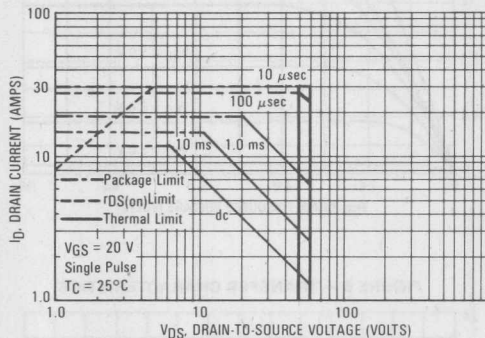
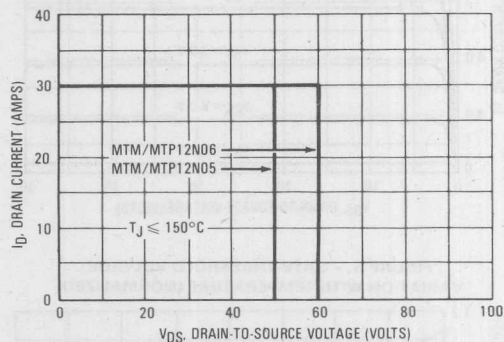


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

THERMAL RESPONSE

FIGURE 11 — MTM12N05/MTM12N06

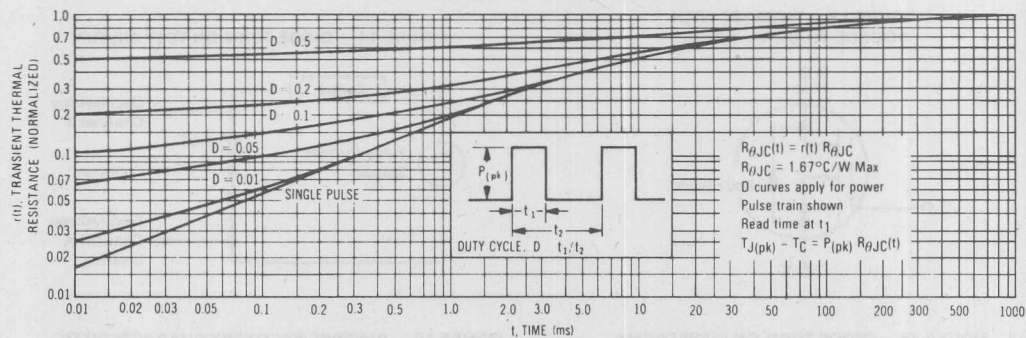
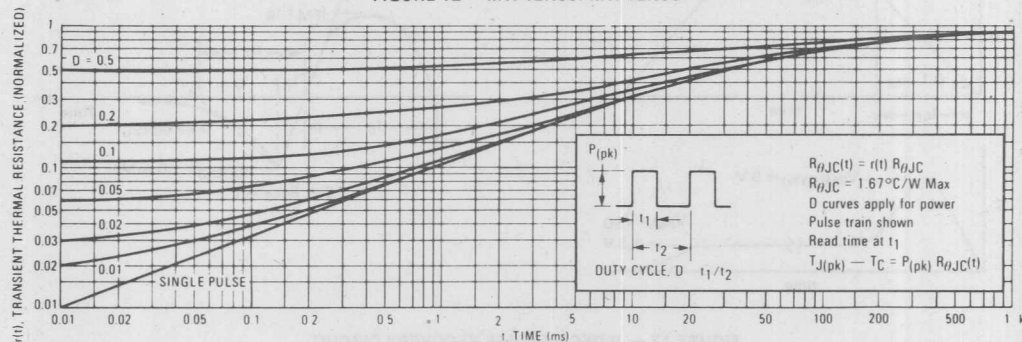


FIGURE 12 — MTP12N05/MTP12N06



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 3.0 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on

of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse di-

rection. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 13 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

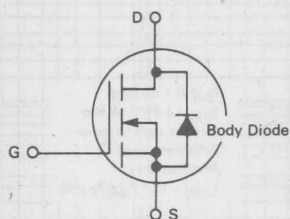


FIGURE 14 — DIODE TURN-ON TEST CIRCUIT

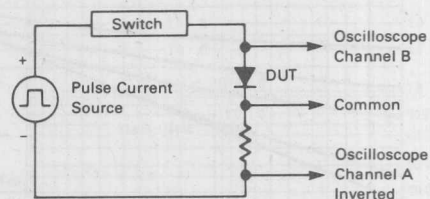


FIGURE 15 — DIODE TURN-ON WAVEFORMS

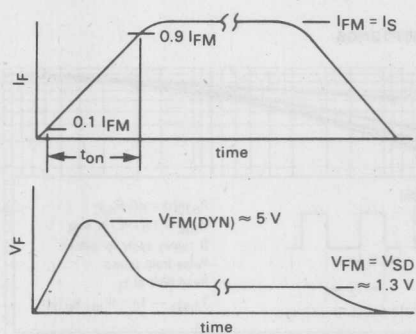


FIGURE 16 — REVERSE RECOVERY CHARACTERISTIC

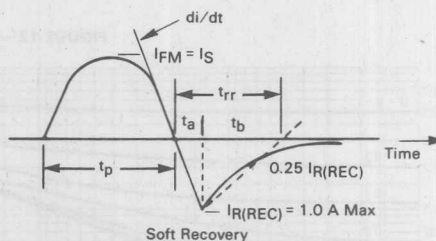
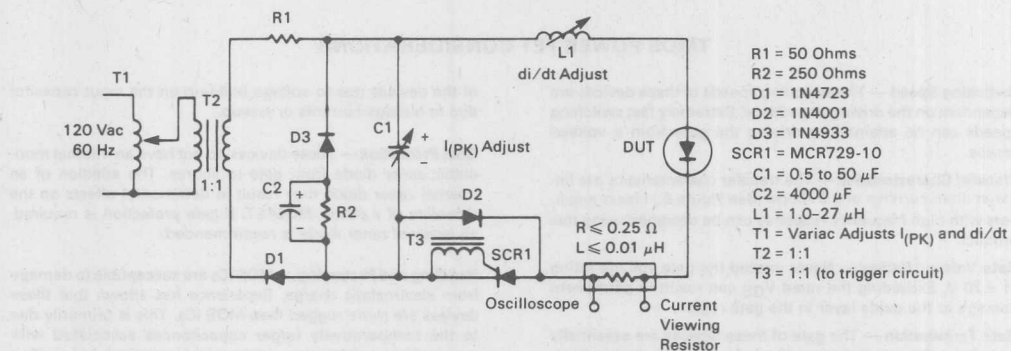


FIGURE 17 — JEDEC REVERSE RECOVERY CIRCUIT



**MOTOROLA**

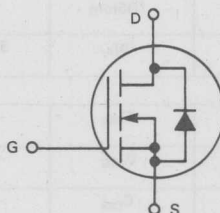
MTM12N08
MTM12N10
MTP12N08
MTP12N10

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

Rating	Symbol	MTM12N08 MTP12N08	MTM12N10 MTP12N10	Unit
Drain — Source Voltage	V_{DSS}	80	100	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ m}\Omega$)	V_{DGR}	80	100	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	12		Adc
Pulsed	I_{DM}	30		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75		Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C/W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

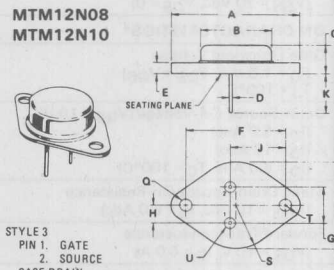
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

12 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)} = 0.25 \text{ OHM}$
 80 and 100 VOLTS

MTM12N08
 MTM12N10



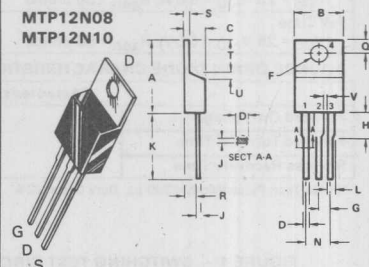
STYLE 3
 PIN 1. GATE
 PIN 2. SOURCE
 CASE DRAIN

NOTES:
 1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

CASE 1-04
 TO-3 TYPE

DIM	MIN	MAX	MIN	MAX
A	—	38.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.87	1.02	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.30	30.40	1.177	1.197
G	10.87	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.84	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	26.67	—	1.050
N	2.54	3.05	0.100	0.120

MTP12N08
 MTP12N10



STYLE 5
 PIN 1. GATE
 PIN 2. DRAIN
 PIN 3. SOURCE
 PIN 4. DRAIN

CASE 221A-02
 TO-220AB

DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.84	0.89	0.035	0.035
E	3.81	3.73	0.142	0.147
F	2.41	2.67	0.095	0.105
G	2.79	3.30	0.110	0.130
H	0.36	0.56	0.014	0.022
J	12.10	14.27	0.500	0.562
K	1.14	1.27	0.045	0.050
L	4.83	5.33	0.190	0.210
M	2.54	3.04	0.100	0.120
N	2.04	2.79	0.080	0.110
O	1.14	1.39	0.045	0.055
P	5.97	6.48	0.235	0.255
Q	0.76	1.27	0.030	0.050
R	1.14	—	—	0.045

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	80 100	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_C = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mA _{dc}
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nA _{dc}

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 6.0$ A _{dc}) ($I_D = 12$ A _{dc}) ($I_D = 6.0$ A _{dc} , $T_C = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	1.5 3.0 2.5	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 6.0$ A _{dc})	$r_{DS(on)}$	—	0.25	Ohms
Forward Transconductance ($V_{DS} = 10$ V, $I_D = 6.0$ A)	g_{fs}	3.0	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1$ MHz)	C_{iss}	—	1200	pF
Output Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1$ MHz)	C_{oss}	—	500	pF
Reverse Transfer Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1$ MHz)	C_{rss}	—	120	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time ($V_{DS} = 25$ V, $I_D = 6.0$ A, $R_{gen} = 50$ ohms)	$t_{d(on)}$	—	50	ns
Rise Time ($V_{DS} = 25$ V, $I_D = 6.0$ A, $R_{gen} = 50$ ohms)	t_r	—	150	ns
Turn-Off Delay Time ($V_{DS} = 25$ V, $I_D = 6.0$ A, $R_{gen} = 50$ ohms)	$t_{d(off)}$	—	200	ns
Fall Time ($V_{DS} = 25$ V, $I_D = 6.0$ A, $R_{gen} = 50$ ohms)	t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage $I_S = 12$ A	V_{SD}	1.3	Vdc
Forward Turn-On Time $V_{GS} = 0$	t_{on}	250	ns
Reverse Recovery Time See Figures 17 and 18	t_{rr}	325	ns

*Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

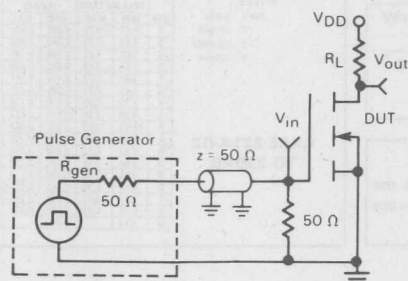
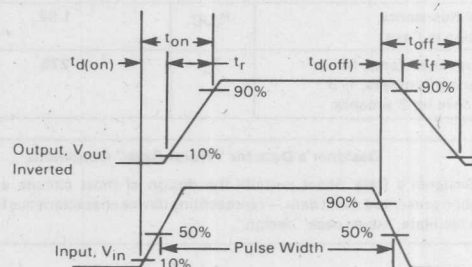


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

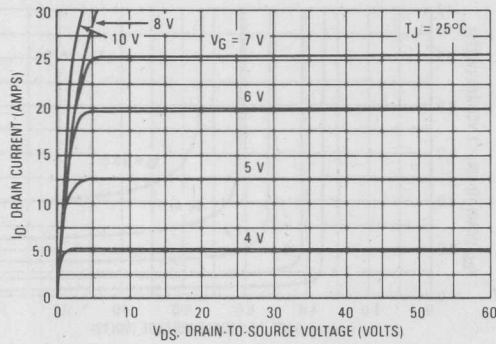


FIGURE 4 — ON-REGION CHARACTERISTICS

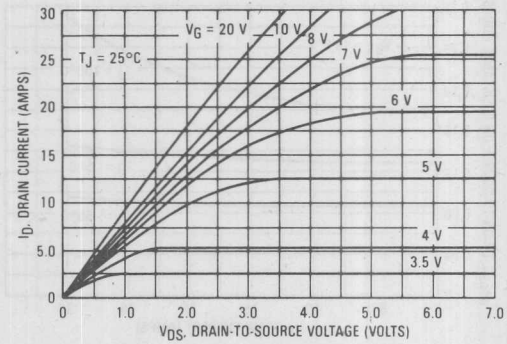


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

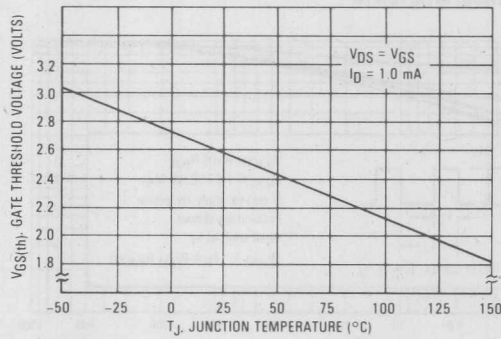


FIGURE 6 — TRANSFER CHARACTERISTICS

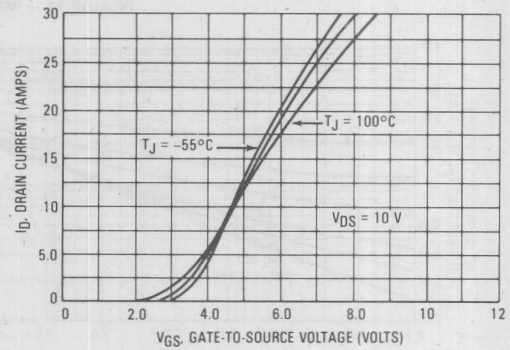


FIGURE 7 — ON-VOLTAGE versus TEMPERATURE

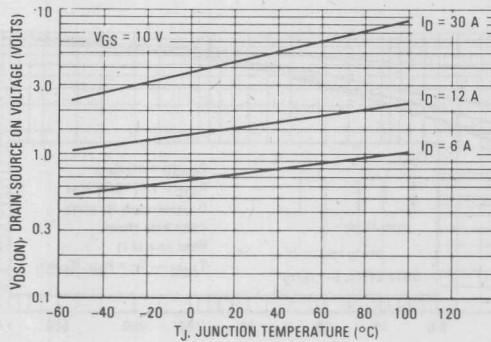
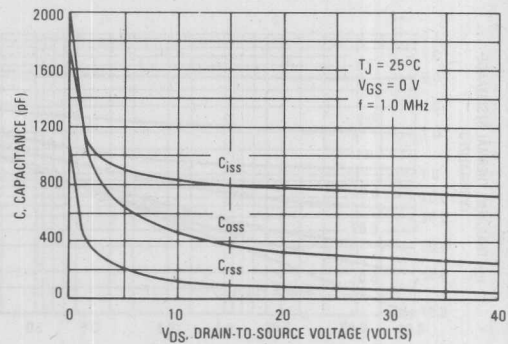


FIGURE 8 — CAPACITANCE VARIATION



TYPICAL CHARACTERISTICS

FIGURE 9 — ON-RESISTANCE versus DRAIN CURRENT

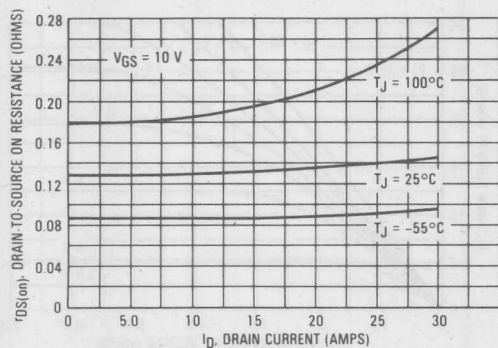
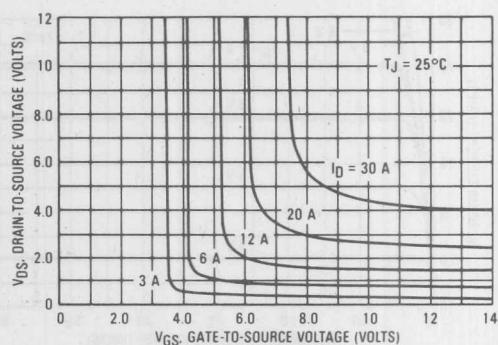


FIGURE 10 — ON-VOLTAGE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM12N08/MTM12N10

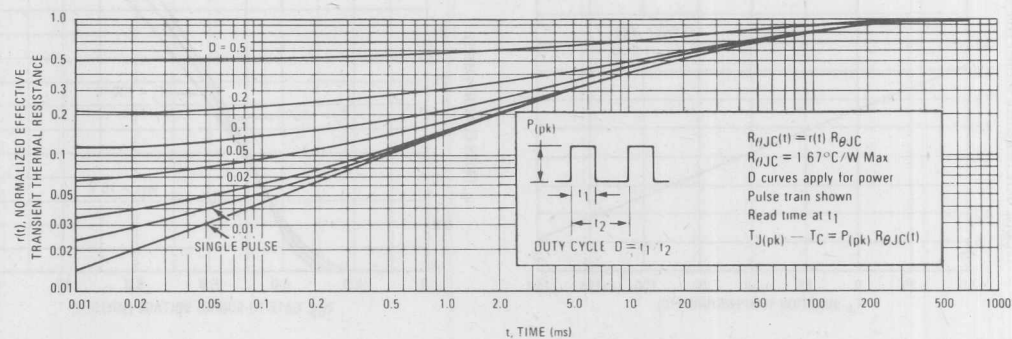
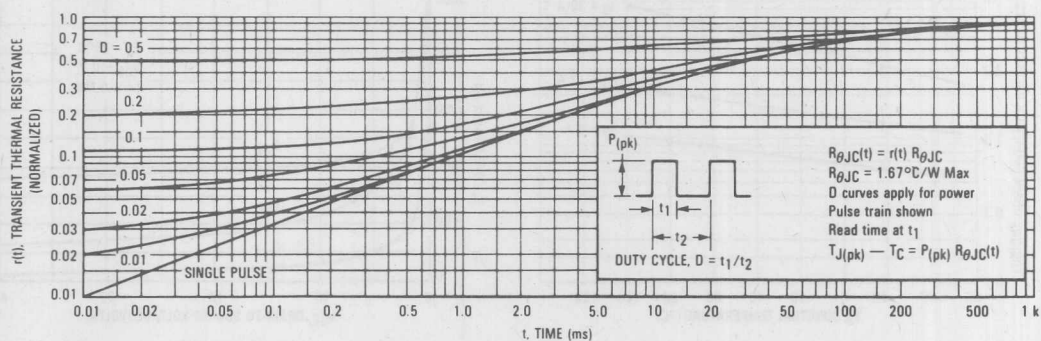


FIGURE 12 — MTP12N08/MTM12N10



OPERATING AREA INFORMATION

FIGURE 13 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

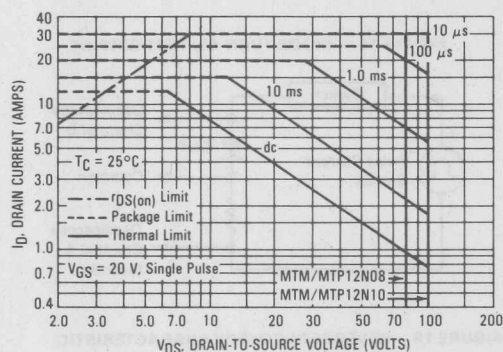
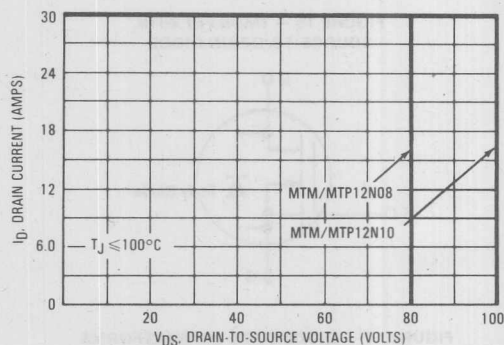


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 13 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 13.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 11. Reversal of the drain voltage will cause current flow in the reverse direction. This

diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 15 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

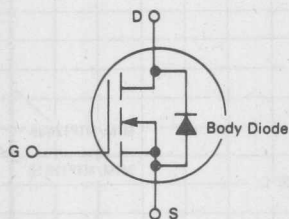


FIGURE 17 — DIODE TURN-ON WAVEFORMS

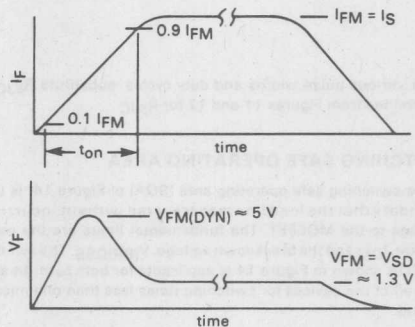


FIGURE 16 — DIODE TURN-ON TEST CIRCUIT

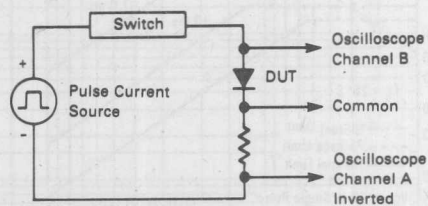


FIGURE 18 — REVERSE RECOVERY CHARACTERISTIC

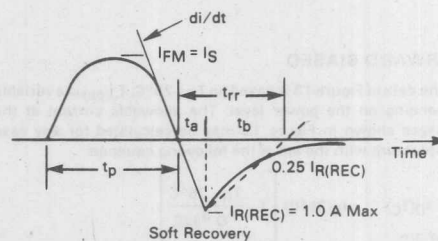
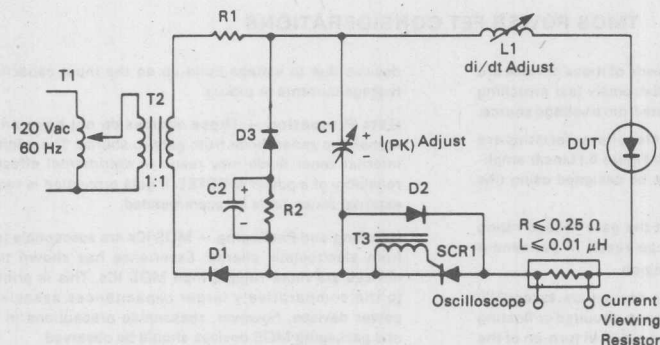


FIGURE 19 — JEDEC REVERSE RECOVERY CIRCUIT



- R1 = 50 Ohms
- R2 = 250 Ohms
- D1 = 1N4723
- D2 = 1N4001
- D3 = 1N4933
- SCR1 = MCR729-10
- C1 = 0.5 to 50 μ F
- C2 = 4000 μ F
- L1 = 1.0-27 μ H
- T1 = Variac Adjusts I_{PK} and di/dt
- T2 = 1:1
- T3 = 1:1 (to trigger circuit)

**MOTOROLA**

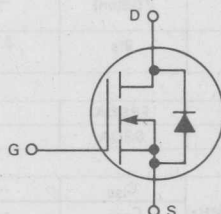
MTM15N05
MTM15N06
MTP15N05
MTP15N06

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid, relay drivers and motor drives.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

Rating	Symbol	MTM15N05 MTP15N05	MTM15N06 MTP15N06	Unit
Drain — Source Voltage	V_{DSS}	50	60	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	50	60	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	15		Adc
Pulsed	I_{DM}	40		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75		Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

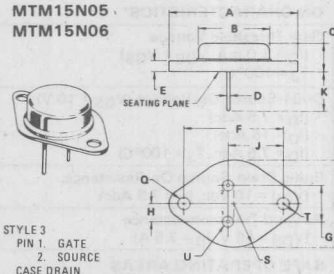
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

15 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)} = 0.16 \text{ OHMS}$
 50 and 60 VOLTS

MTM15N05
 MTM15N06



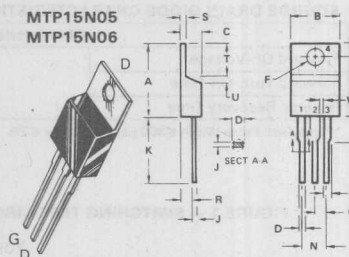
STYLE 3
 PIN 1. GATE
 2. SOURCE
 CASE DRAIN

NOTES:
 1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO 3 OUTLINE SHALL APPLY.

DIM	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	8.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	18.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	28.67	—	1.090	—
U	2.54	3.05	0.100	0.120

CASE 1-04
 TO-3 TYPE

MTP15N05
 MTP15N06



STYLE 5
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
E	3.61	3.73	0.142	0.147
F	2.41	2.67	0.095	0.105
G	2.79	3.30	0.110	0.130
H	0.36	0.56	0.014	0.022
J	12.70	14.27	0.500	0.562
K	1.14	1.27	0.045	0.050
L	4.83	5.33	0.190	0.210
N	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—

CASE 221A-02
 TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0\text{ mA}$)	$V_{(BR)DSS}$	50 60	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85\text{ Rated } V_{DSS}$, $V_{GS} = 0$, $T_J = 100^\circ\text{C}$)	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0\text{ mA}$, $V_{DS} = V_{GS}$, $T_J = 100^\circ\text{C}$)	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 7.5\text{ Adc}$) ($I_D = 15\text{ Adc}$) ($I_D = 7.5\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	1.2 2.9 2.4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 7.5\text{ Adc}$)	$r_{DS(on)}$	—	0.16	Ohms
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 7.5\text{ A}$)	g_{fs}	3.5	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	700	pF
Reverse Transfer Capacitance		C_{rss}	—	250	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DS} = 25\text{ V}$, $I_D = 7.5\text{ A}$, $R_{gen} = 50\text{ ohms}$)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage ($I_S = 15\text{ A}$)	V_{SD}	1.5	Vdc
Forward Turn-On Time ($V_{GS} = 0$)	t_{on}	250	ns
Reverse Recovery Time (See Figures 15 and 16)	t_{rr}	325	ns

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

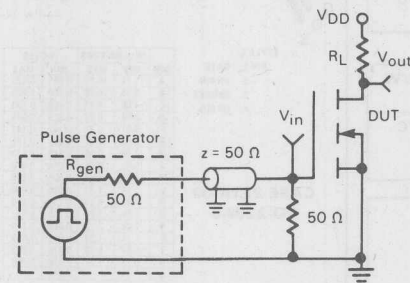
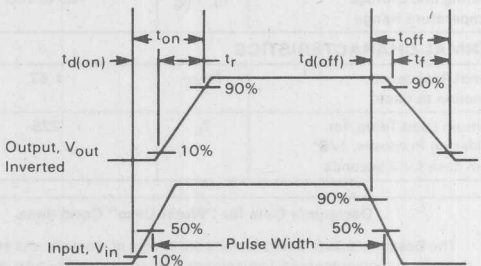


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

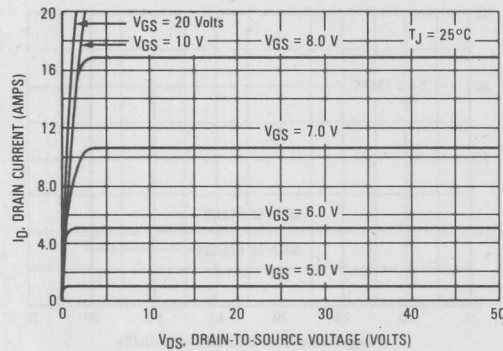


FIGURE 4 — ON-REGION CHARACTERISTICS

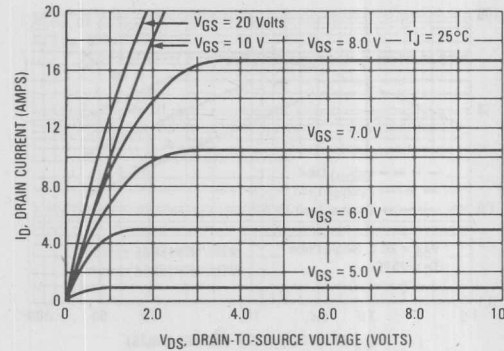


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

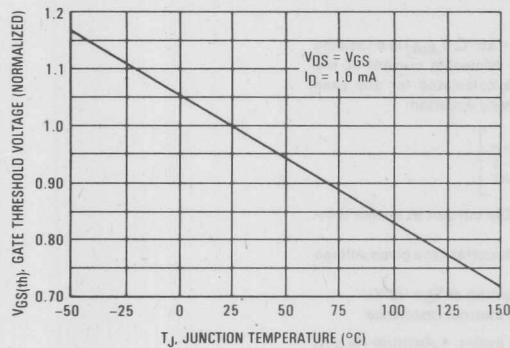


FIGURE 6 — TRANSFER CHARACTERISTICS

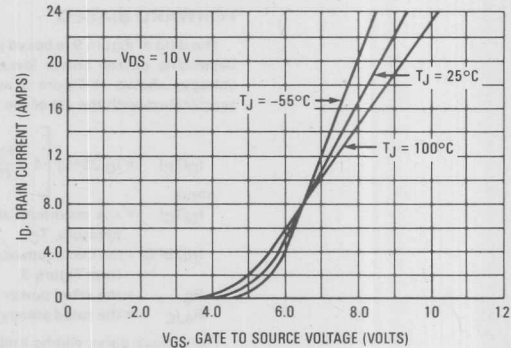


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

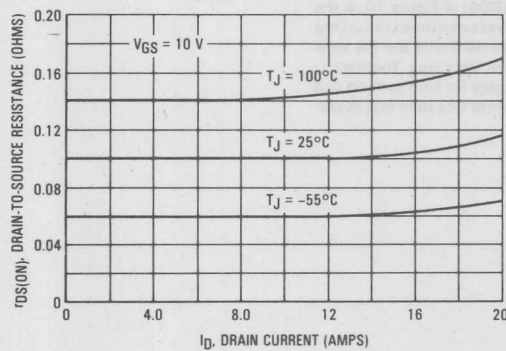
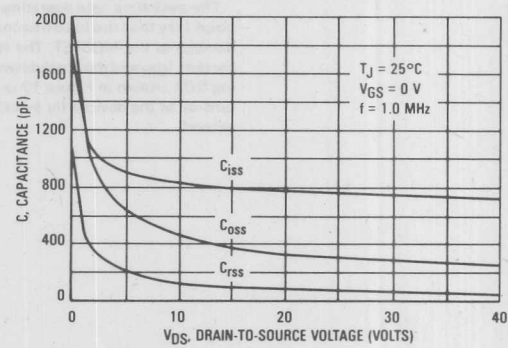


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIAS
SAFE OPERATING AREA

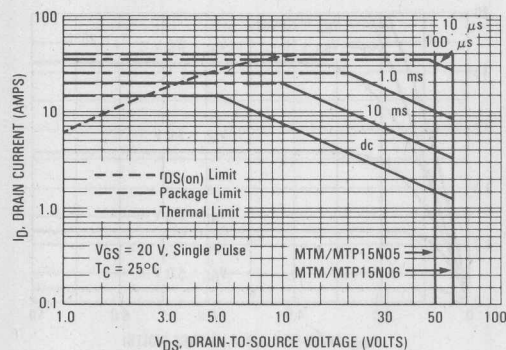
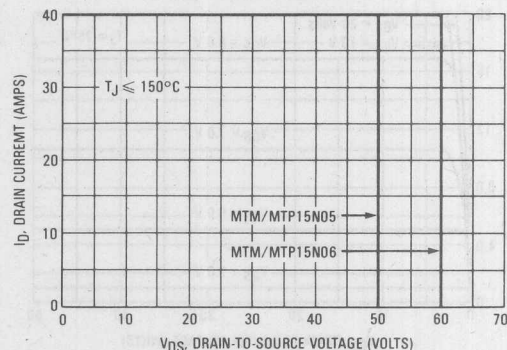


FIGURE 10 — MAXIMUM RATED SWITCHING
SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

THERMAL RESPONSE

FIGURE 11 — MTM15N05/MTM15N06

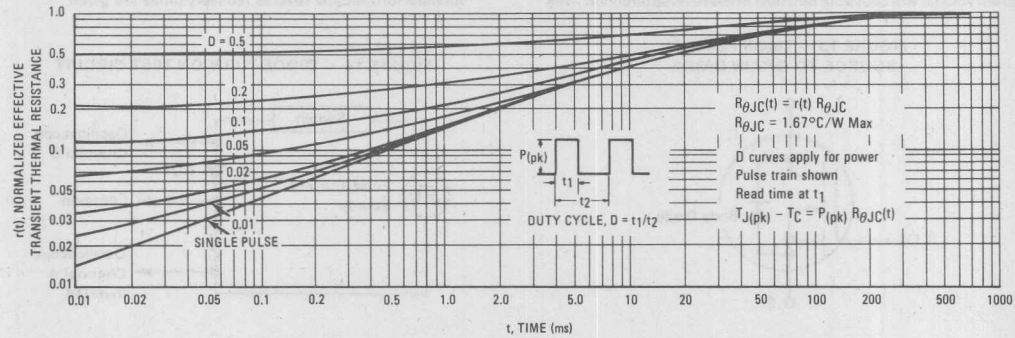
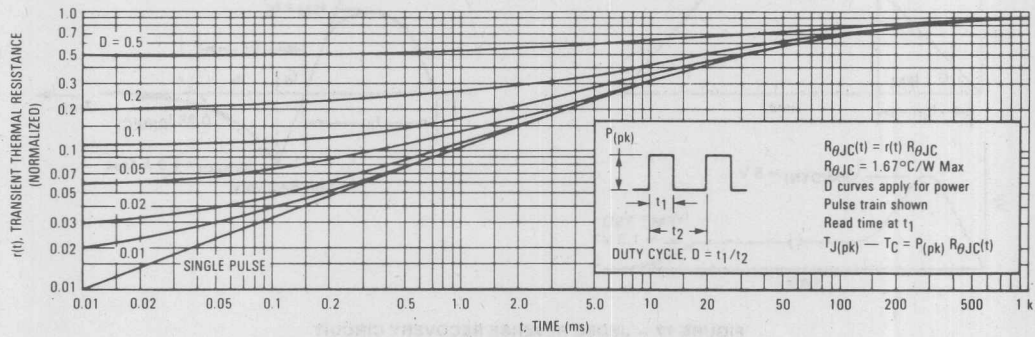


FIGURE 12 — MTP15N05/MTP15N06



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 3.0 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 11. Reversal of the drain voltage will cause current flow in the reverse direction. This

diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 13 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

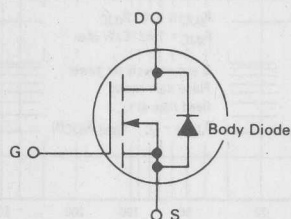


FIGURE 14 — DIODE TURN-ON TEST CIRCUIT

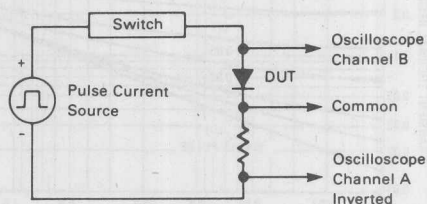


FIGURE 15 — DIODE TURN-ON WAVEFORMS

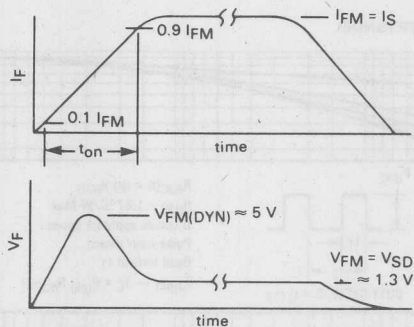


FIGURE 16 — REVERSE RECOVERY CHARACTERISTIC

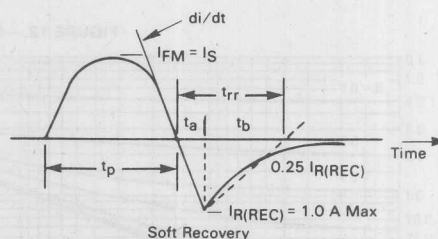
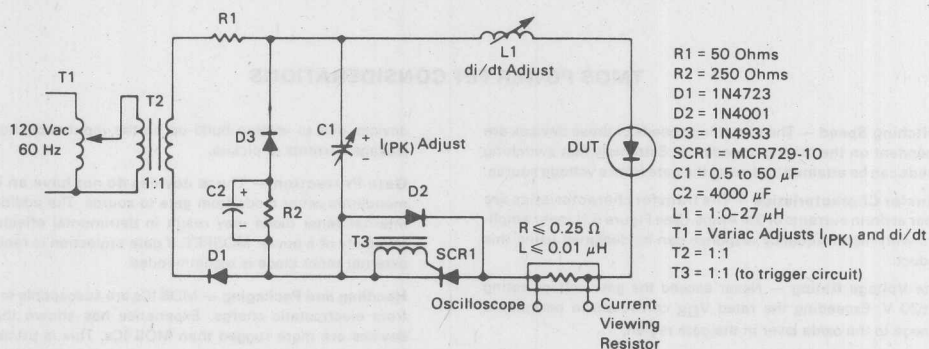


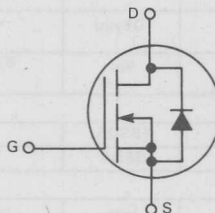
FIGURE 17 — JEDEC REVERSE RECOVERY CIRCUIT



**MOTOROLA****MTM15N35
MTM15N40****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, and motor controls.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)

**MAXIMUM RATINGS**

Rating	Symbol	MTM15N35	MTM15N40	Unit
Drain — Source Voltage	V_{DSS}	350	400	Vdc
Drain — Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	350	400	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current	I_D	15		Adc
Continuous	I_{DM}	70		
Pulsed				
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power	P_D	250		Watts
Dissipation @ $T_C = 25^\circ\text{C}$		2.0		W/ $^\circ\text{C}$
Derate above 25°C				
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

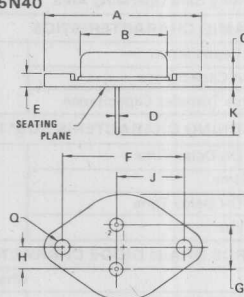
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

15 AMPERE**N-CHANNEL TMOS
POWER FET**

$r_{DS(on)} = 0.4 \text{ OHMS}$
350 and 400 VOLTS

**MTM15N35
MTM15N40****STYLE 3:**

PIN 1. GATE
2. SOURCE
CASE. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.84	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

**CASE 197-01
TO-3 TYPE**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	350 400	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 7.5$ Adc) ($I_D = 15$ Adc) ($I_D = 7.5$ Adc, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	—	3.0 7.5 5.5	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 7.5$ Adc)	$r_{DS(on)}$	—	0.4	Ohms
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 7.5$ A)	g_{fs}	6.0	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

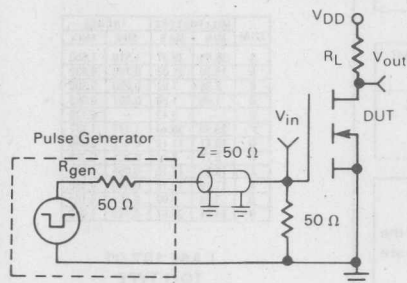
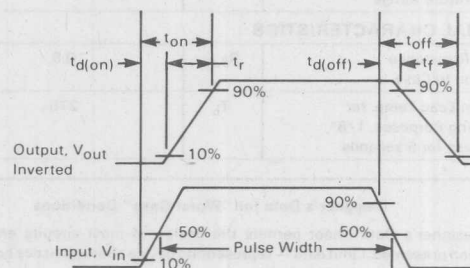
Input Capacitance	$(V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	3600	pF
Output Capacitance		C_{oss}	—	700	pF
Reverse Transfer Capacitance		C_{rss}	—	300	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	$(V_{DS} = 125$ V, $I_D = 7.5$ A, $R_{gen} = 50$ ohms)	$t_{d(on)}$	—	120	ns
Rise Time		t_r	—	300	ns
Turn-Off Delay Time		$t_{d(off)}$	—	400	ns
Fall Time		t_f	—	240	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage	V_{SD}	1.0	Vdc
Forward Turn-On Time	t_{on}	175	ns
Reverse Recovery Time	t_{rr}	600	ns

*Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING****FIGURE 1 — SWITCHING TEST CIRCUIT****FIGURE 2 — SWITCHING WAVEFORMS**

TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

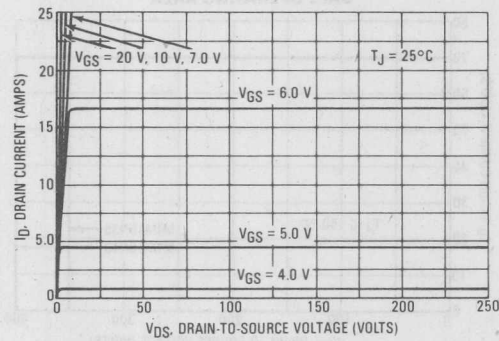


FIGURE 4 — ON CHARACTERISTICS

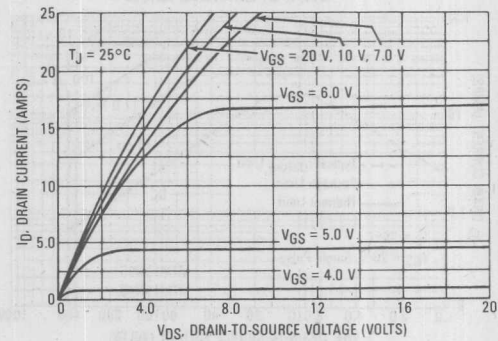


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

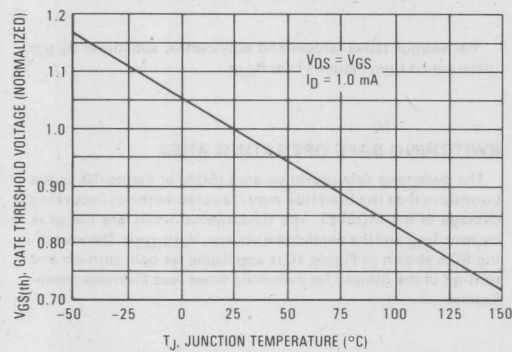


FIGURE 6 — TRANSFER CHARACTERISTICS

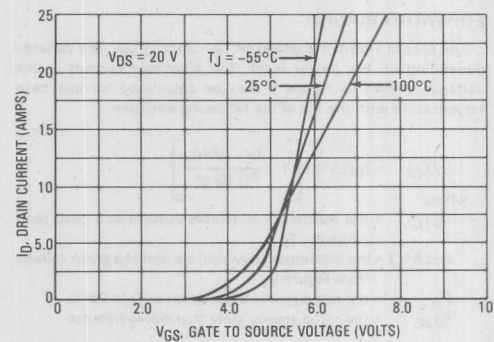


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

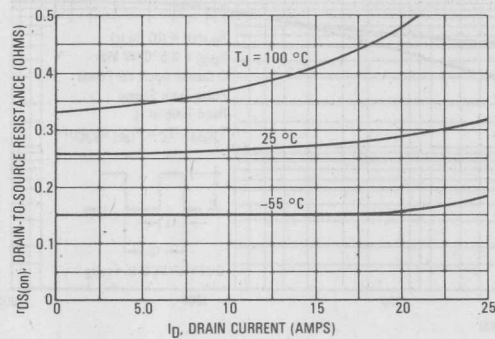
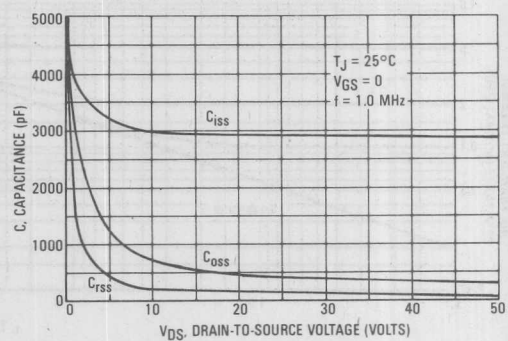


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

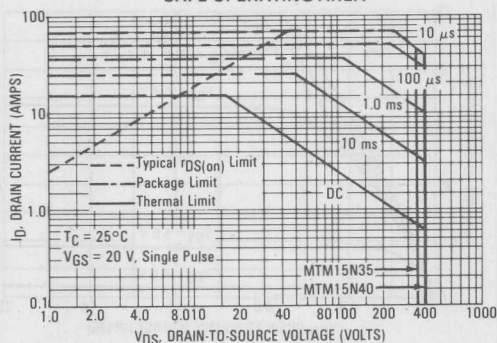
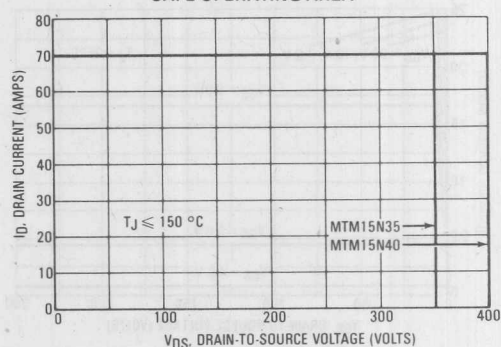


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = the rated steady state thermal resistance

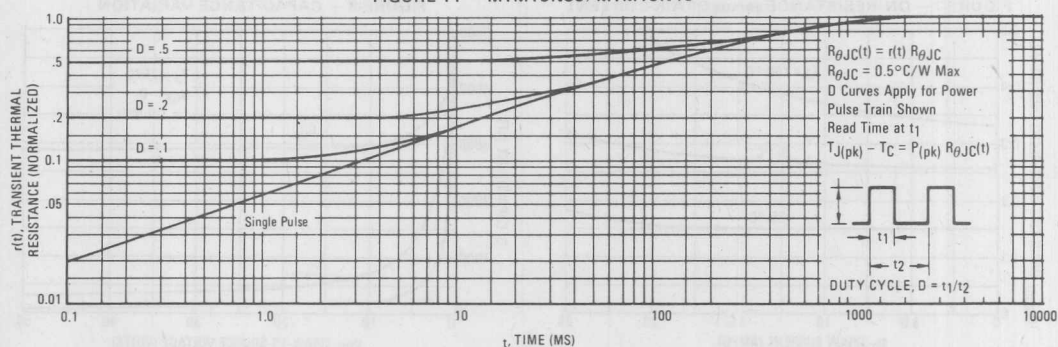
For various pulse widths and duty cycles, substitute $R_{\theta JC}(t)$ determined from Figure 11 for $R_{\theta JC}$

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

THERMAL RESPONSE

FIGURE 11 — MTM15N35/MTM15N40



TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This

FIGURE 12 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

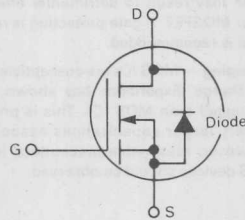
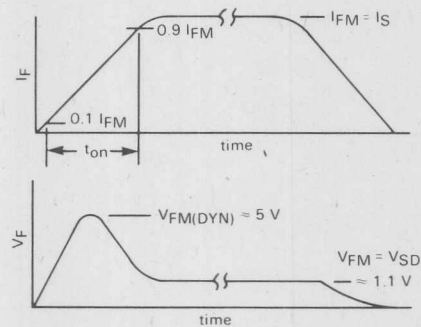


FIGURE 14 — BODY DIODE TURN-ON WAVEFORMS



diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 13 — DIODE TURN-ON TEST CIRCUIT

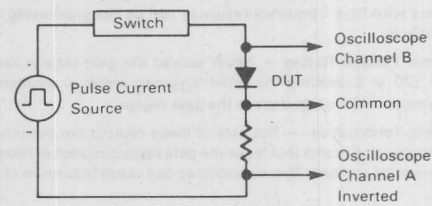


FIGURE 15 — REVERSE RECOVERY CHARACTERISTIC

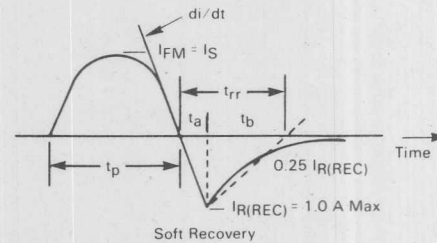
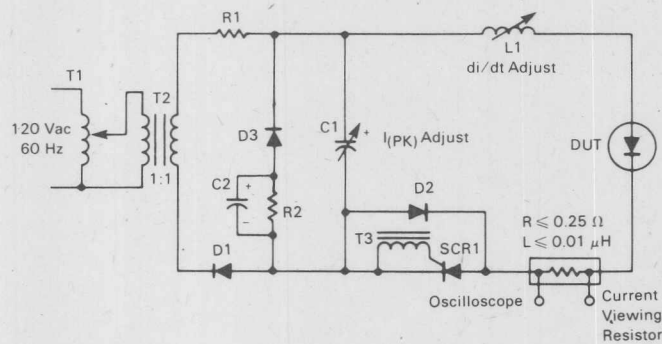


FIGURE 16 — JEDEC REVERSE RECOVERY CIRCUIT



- R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μ F
C2 = 4000 μ F
L1 = 1.0-27 μ H
T1 = Variac Adjusts I_{PK} and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

MOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 3.0 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

FIGURE 12 — REVERSE RECOVERY CHARACTERISTICS

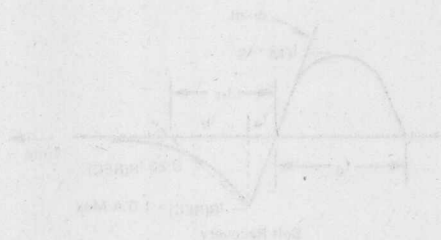


FIGURE 13 — BODY DIODE TURN-ON WAVEFORM

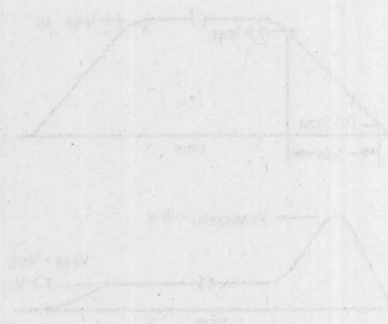
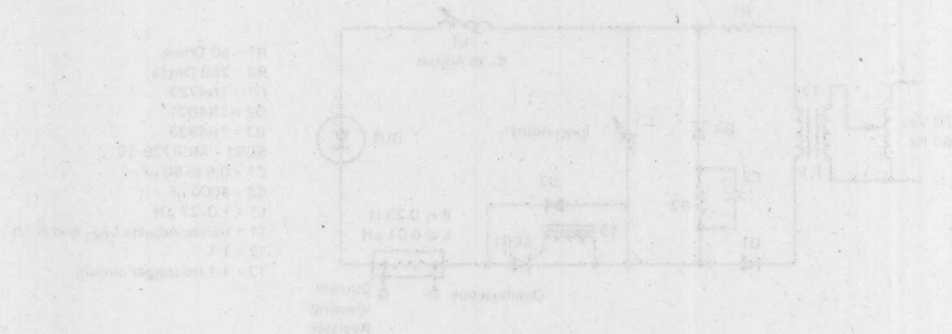


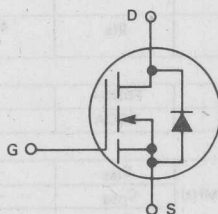
FIGURE 14 — 100% REVERSE RECOVERY CIRCUIT



**MOTOROLA****MTM15N45
MTM15N50****Designer's Data Sheet****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, and motor controls.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.5$ Volts (max)

**MAXIMUM RATINGS**

Rating	Symbol	MTM15N45	MTM15N50	Unit
Drain — Source Voltage	V_{DSS}	450	500	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGO}	450	500	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	15		Adc
Pulsed	I_{DM}	65		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250		Watts
Derate above 25°C		2.0		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

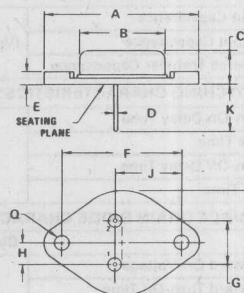
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

15 AMPERE**N-CHANNEL TMOS
POWER FET**

$r_{DS(on)} = 0.5 \text{ OHM}$
450 and 500 VOLTS

**MTM15N45
MTM15N50**

STYLE 1
PIN 1. GATE
2. SOURCE
CASE. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E		3.43		0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-3 TYPE

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0\text{ mA}$)	$V_{(BR)DSS}$	450 500	— —	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ Rated V_{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($I_D = 1.0\text{ mA}$, $V_{DS} = V_{GS}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 7.5\text{ Adc}$) ($I_D = 15\text{ Adc}$) ($I_D = 7.5\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— — —	3.75 9.0 7.5	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 7.5\text{ Adc}$)	$r_{DS(on)}$	—	0.5	Ohms
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 7.5\text{ A}$)	g_{fs}	4.0	—	mhos

SAFE OPERATING AREAS

Forward Biased Safe Operating Area	FBSOA	See Figure 9
Switching Safe Operating Area	SSOA	See Figure 10

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{iss}	—	3600	pF
Output Capacitance		C_{oss}	—	700	pF
Reverse Transfer Capacitance		C_{rss}	—	300	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DS} = 125\text{ V}$, $I_D = 7.5\text{ A}$, $R_{gen} = 50\text{ ohms}$)	$t_{d(on)}$	—	120	ns
Rise Time		t_r	—	300	ns
Turn-Off Delay Time		$t_{d(off)}$	—	400	ns
Fall Time		t_f	—	240	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage	V_{SD}	1.5	Vdc
Forward Turn-On Time	t_{on}	175	ns
Reverse Recovery Time	t_{rr}	600	ns

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

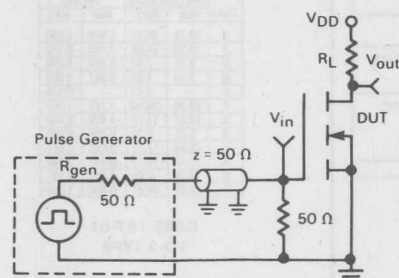
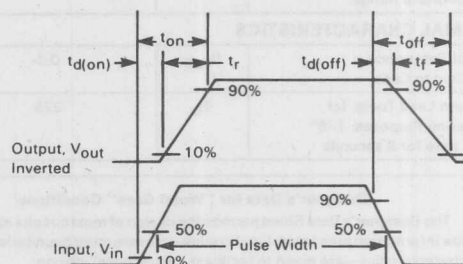


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

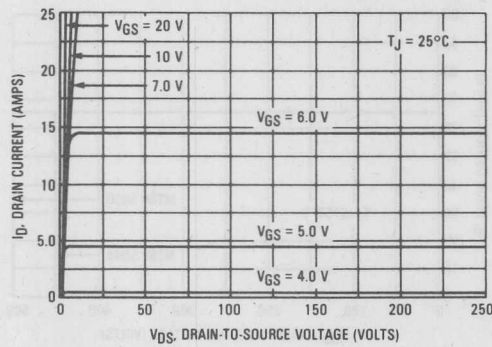


FIGURE 4 — ON-REGION CHARACTERISTICS

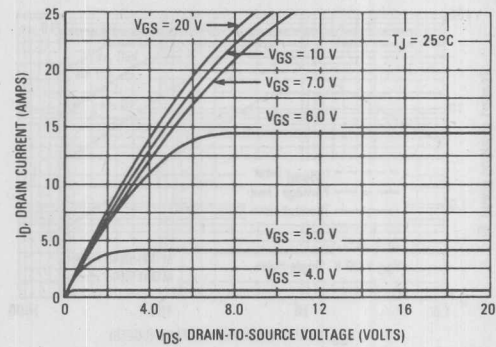


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

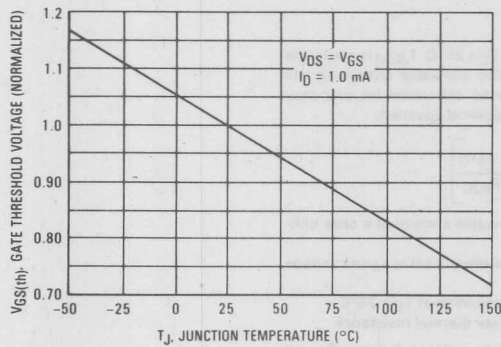


FIGURE 6 — TRANSFER CHARACTERISTICS

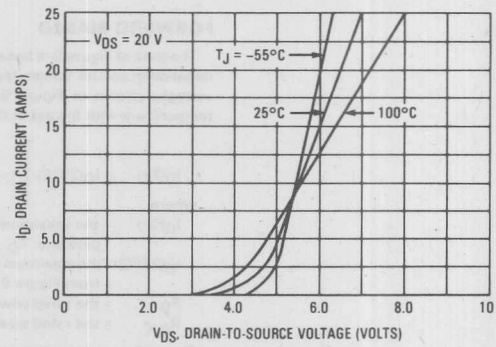


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

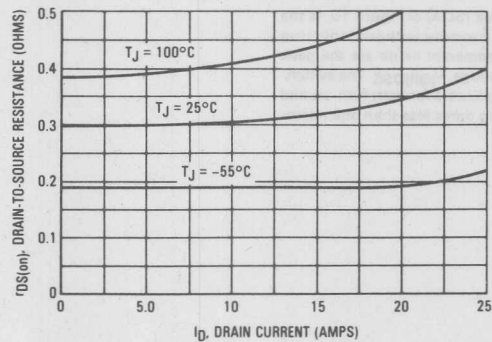
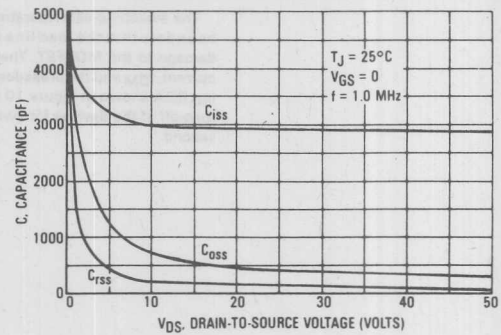
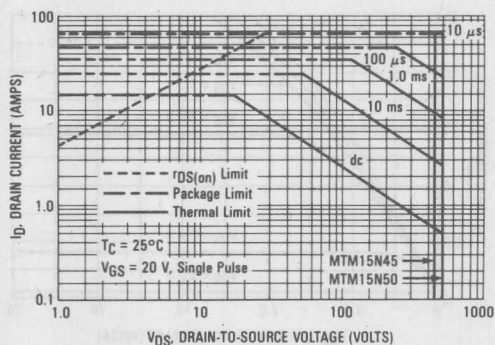
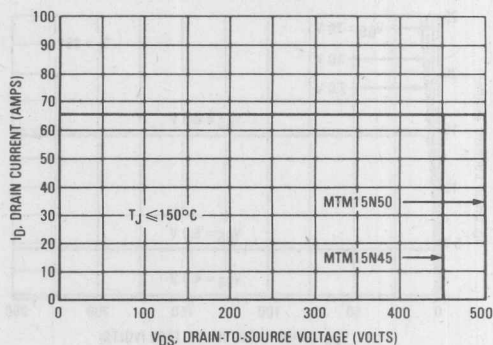


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIAS
SAFE OPERATING AREAFIGURE 10 — MAXIMUM RATED SWITCHING
SAFE OPERATING AREA

FORWARD BIASED

The data of Figure 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

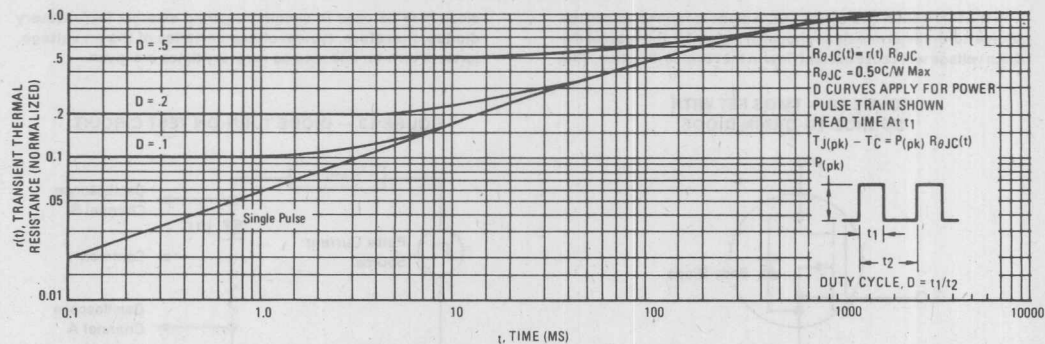
$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figure 11 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

FIGURE 11 — MTM15N45/MTM15N50



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 2.5 Amps. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This

diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 12 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

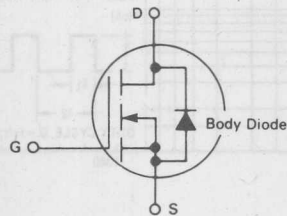


FIGURE 14 — DIODE TURN-ON WAVEFORMS

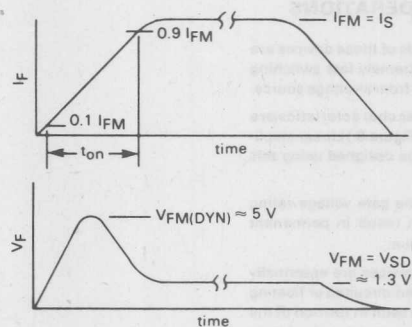


FIGURE 13 — DIODE TURN-ON TEST CIRCUIT

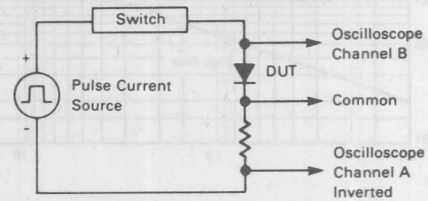


FIGURE 15 — REVERSE RECOVERY CHARACTERISTIC

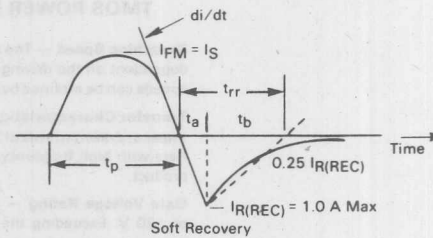
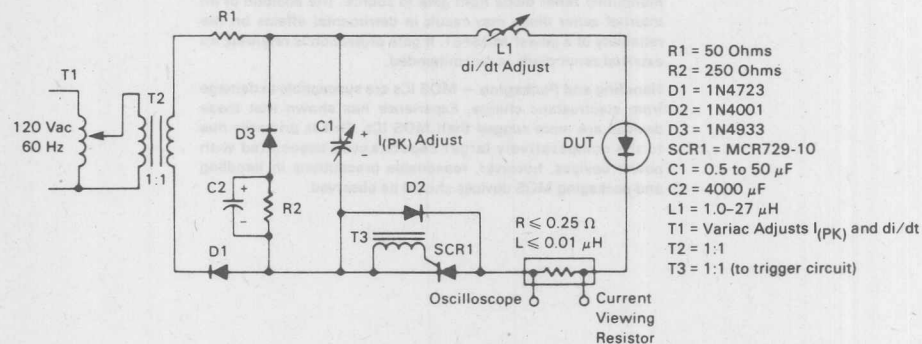


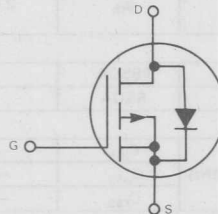
FIGURE 16 — JEDEC REVERSE RECOVERY CIRCUIT



**MOTOROLA****MTM814, MTM815
MTP814, MTP815****Designer's Data Sheet****P-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS} , $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)} = 4.0$ Volts (max)

**MAXIMUM RATINGS**

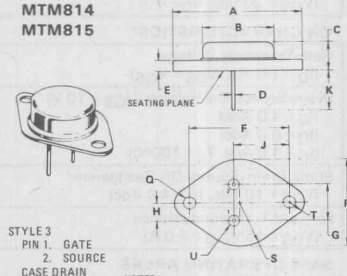
Rating	Symbol	MTM814 MTP814	MTM815 MTP815	Unit
Drain — Source Voltage	V_{DSS}	80	100	Vdc
Drain — Gate Voltage	V_{DGO}	80	100	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current				Adc
Continuous	I_D	8.0		
Pulsed	I_{DM}	20		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power	P_D	75		Watts
Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C		0.6		W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

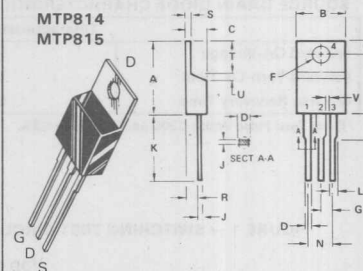
8 AMPERE**P-CHANNEL TMOS
POWER FET****80 and 100 VOLTS****MTM814
MTM815**

STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

**CASE 1-04
TO-3 TYPE**

DIM	MIN	MAX	MIN	MAX
A	—	39.27	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.50	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.58	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120

**MTP814
MTP815**

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

**CASE 221A-02
TO-220AB**

DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
O	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	—	0.045	—

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	80 100	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85$ BV _{DSS} , $V_{GS} = 0$) $T_J = 100^\circ\text{C}$	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage ($I_D = 1.0$ mA, $V_{DS} = V_{GS}$)	$V_{GS(th)}$	1.5	4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 4.0$ Adc) ($I_D = 8.0$ Adc) ($I_D = 4.0$ Adc, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	—	1.6 3.2 3.0	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 4.0$ Adc)	$r_{DS(on)}$	—	0.4	Ohms
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 4.0$ A)	g_{fs}	2.0	—	mhos
SAFE OPERATING AREAS				
Forward Biased Safe Operating Area	FBSOA		See Figure 13	
Switching Safe Operating Area	SSOA		See Figure 14	
DYNAMIC CHARACTERISTICS				
Input Capacitance	C_{iss}	—	1200	pF
Output Capacitance	C_{oss}	—	600	pF
Reverse Transfer Capacitance	C_{rss}	—	180	pF
SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)				
Turn-On Delay Time	$t_{d(on)}$	—	80	ns
Rise Time	t_r	—	150	ns
Turn-Off Delay Time	$t_{d(off)}$	—	200	ns
Fall Time	t_f	—	150	ns
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage	$I_S = 8.0$ A	V_{SD}	1.3	Vdc
Forward Turn-On Time	$V_{GS} = 0$	t_{on}	250	ns
Reverse Recovery Time	See Figures 17 and 18	t_{rr}	325	ns

*Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.**RESISTIVE SWITCHING**

FIGURE 1 — SWITCHING TEST CIRCUIT

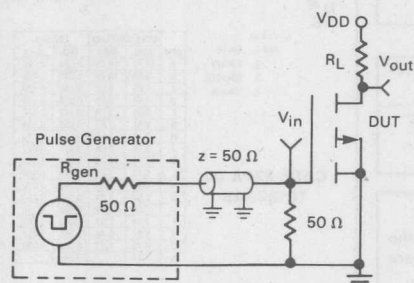
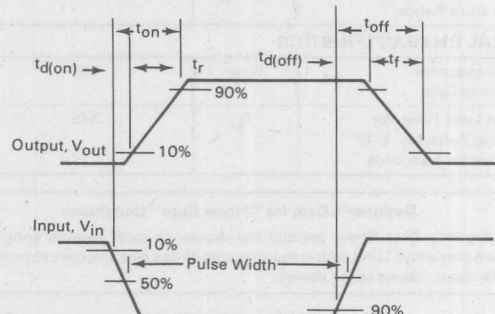


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 OUTPUT CHARACTERISTICS

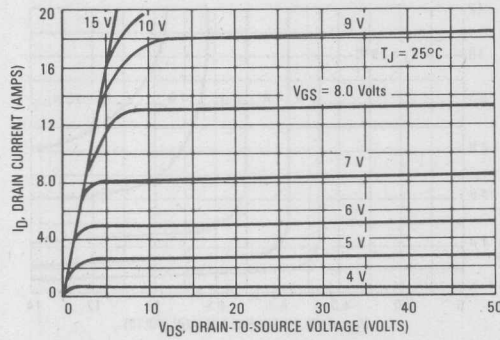


FIGURE 4 — ON-REGION CHARACTERISTICS

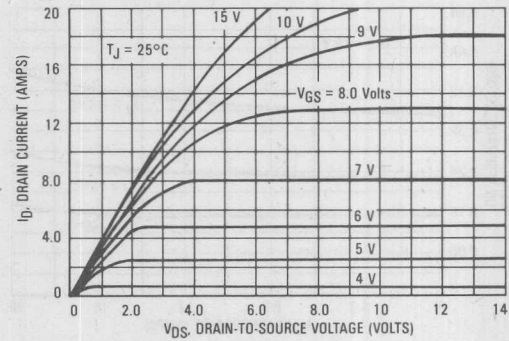


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

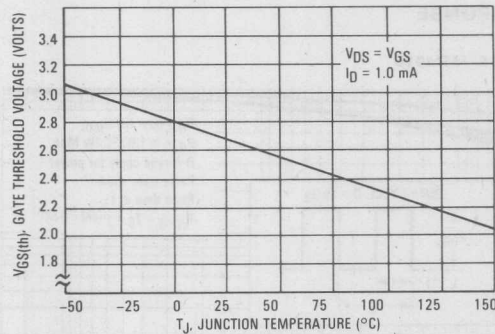


FIGURE 6 — TRANSFER CHARACTERISTICS

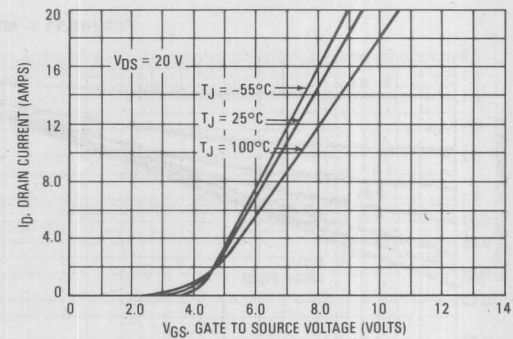


FIGURE 7 — ON-VOLTAGE versus TEMPERATURE

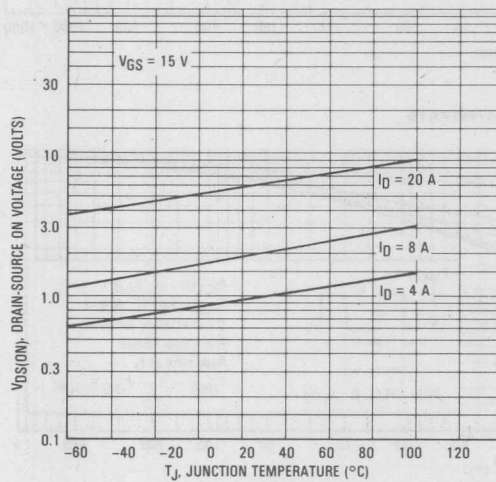
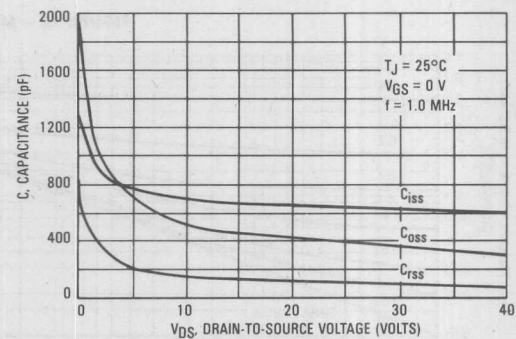


FIGURE 8 — CAPACITANCE VARIATION



TYPICAL CHARACTERISTICS

FIGURE 9 — ON-RESISTANCE versus DRAIN CURRENT

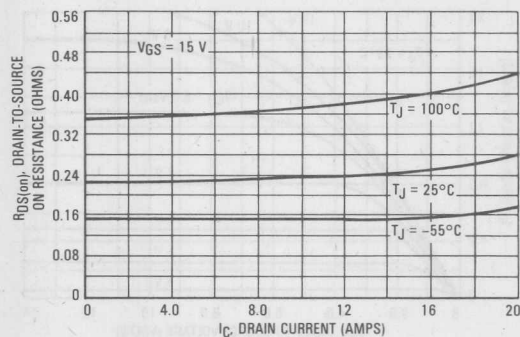
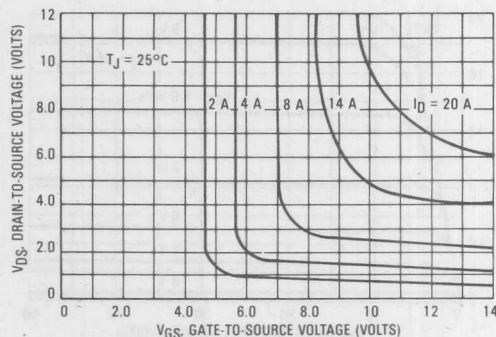


FIGURE 10 — ON-VOLTAGE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM814/MTM815

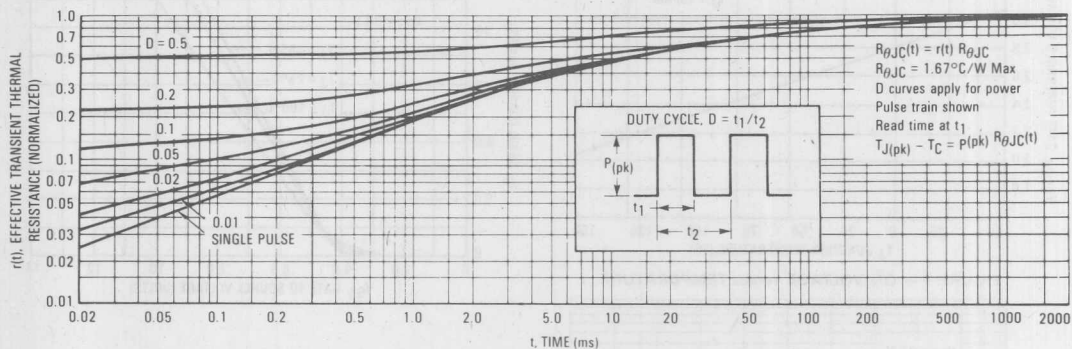
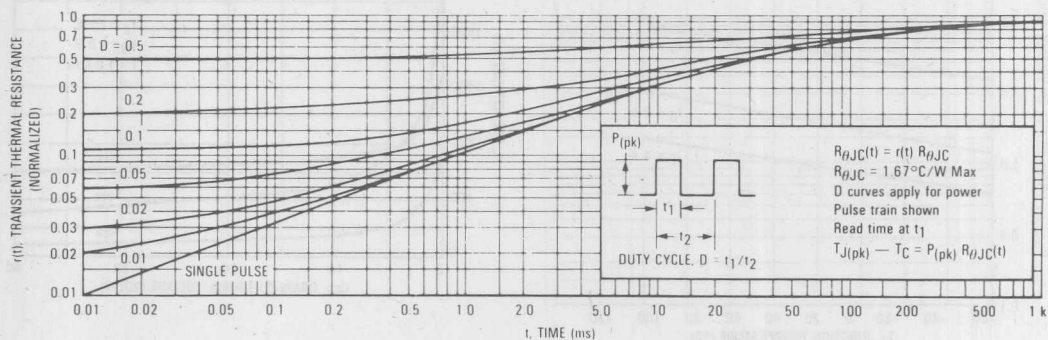
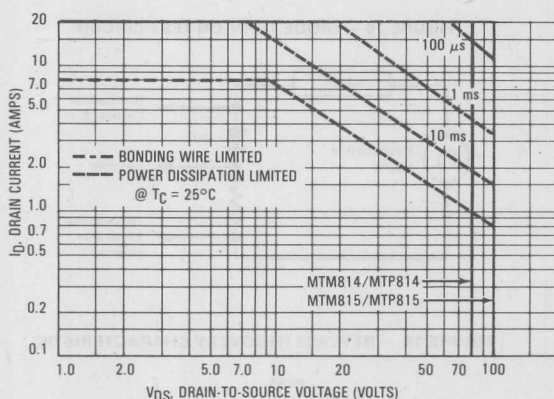


FIGURE 12 — MTP814/MTP815



SAFE OPERATING AREA INFORMATION

FIGURE 13 — MAXIMUM FORWARD BIASED
SAFE OPERATING AREA



FORWARD BIASED

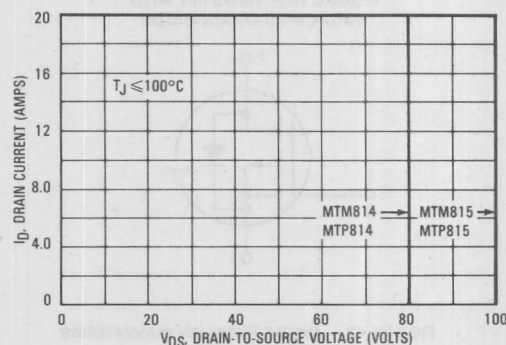
The data of Figure 13 is based on $T_C = 25^\circ\text{C}$. $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 13 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

- $I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .
- $I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 13.
- P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.
- $R_{\theta JC}$ = the rated steady state thermal resistance

FIGURE 14 — MAXIMUM SWITCHING
SAFE OPERATING AREA



For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This

FIGURE 15 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

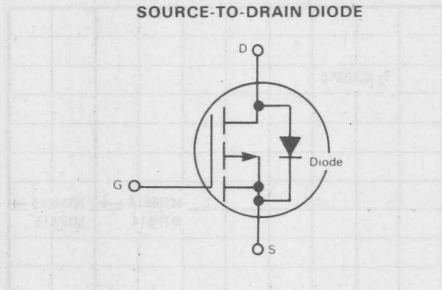
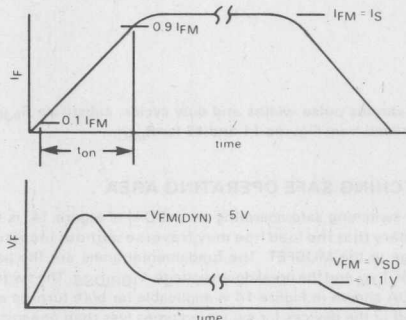


FIGURE 17 — DIODE TURN-ON WAVEFORMS



diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 16 — DIODE TURN-ON TEST CIRCUIT

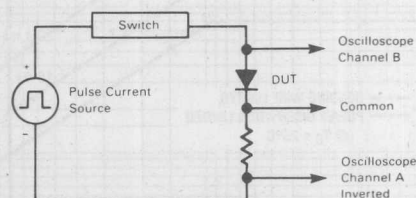


FIGURE 18 — REVERSE RECOVERY CHARACTERISTIC

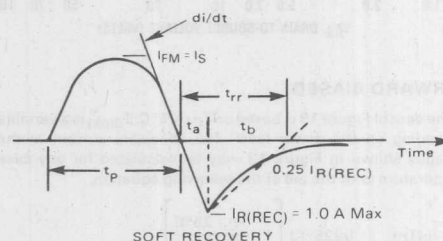
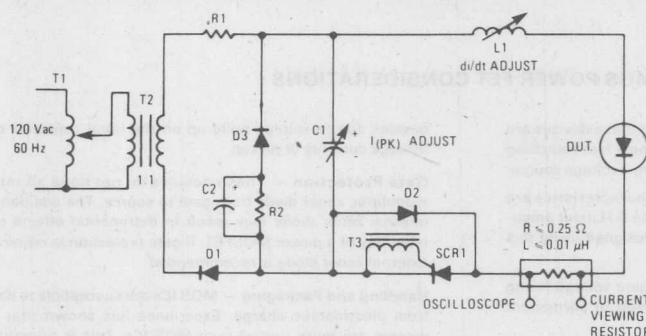


FIGURE 19 — JEDEC REVERSE RECOVERY CIRCUIT

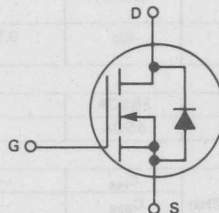


- R1 = 50 Ohms
- R2 = 250 Ohms
- D1 = 1N4723
- D2 = 1N4001
- D3 = 1N4933
- SCR1 = MCR729-10
- C1 = 0.5 to 50 μ F
- C2 = 4000 μ F
- L1 = 1.0 - 27 μ H
- T1 = Variac Adjusts $I_{(PK)}$ and di/dt
- T2 = 1:1
- T3 = 1:1 (to trigger circuit)

**MOTOROLA****MTP5N05, MTP5N06****Designer's Data Sheet****N-CHANNEL ENHANCEMENT MODE SILICON GATE
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads

**MAXIMUM RATINGS**

Rating	Symbol	MTP5N05	MTP5N06	Unit
Drain — Source Voltage	V_{DSS}	50	60	Vdc
Drain — Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	50	60	Vdc
Gate — Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	5.0		Adc
Pulsed	I_{DM}	10		
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	50		Watts
		0.4		W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

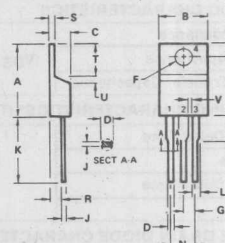
Thermal Resistance Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

5 AMPERE**N-CHANNEL TMOS
POWER FET**

$r_{DS(on)} = 0.6 \text{ OHMS}$
50 and 60 VOLTS

**MTP5N05
MTP5N06**

STYLE:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.85	10.29	0.389	0.409
C	4.06	4.82	0.160	0.190
D	0.84	0.89	0.035	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.38	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

**CASE 221A-02
TO-220AB**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0\text{ mA}$)	MTP5N05 MTP5N06	$V_{(BR)DSS}$	50 60	— —	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85\text{ Rated }V_{DSS}$, $V_{GS} = 0$) $T_J = 100^\circ\text{C}$		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0$)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage ($I_D = 1.0\text{ mA}$, $V_{DS} = 0$) $T_J = 100^\circ\text{C}$		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 2.5\text{ Adc}$) ($I_D = 5.0\text{ Adc}$) ($I_D = 2.5\text{ Adc}$, $T_J = 100^\circ\text{C}$)		$V_{DS(on)}$	— — —	1.5 3.75 3.0	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 2.5\text{ Adc}$)		$r_{DS(on)}$	—	0.6	Ohms
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 2.5\text{ A}$)		g_{fs}	0.75	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA		See Figure 10	
Switching Safe Operating Area		SSOA		See Figure 11	
DYNAMIC CHARACTERISTICS					
Input Capacitance	$(V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1.0\text{ MHz})$	C_{iss}	—	300	pF
Output Capacitance		C_{oss}	—	250	pF
Reverse Transfer Capacitance		C_{rss}	—	60	pF
SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)					
Turn-On Delay Time	$(V_{DS} = 25\text{ V}$, $I_D = 2.5\text{ A}$, $R_{gen} = 50\text{ ohms})$	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	80	ns
Turn-Off Delay Time		$t_{d(off)}$	—	30	ns
Fall Time		t_f	—	30	ns
SOURCE DRAIN DIODE CHARACTERISTICS*					
	Characteristic	Symbol	Typ	Unit	
Forward On-Voltage	$I_S = 5.0\text{ A}$	V_{SD}	1.9	Vdc	
Forward Turn-On Time	$V_{GS} = 0$	t_{on}	150	ns	
Reverse Recovery Time	See Figures 15 and 16	t_{rr}	250	ns	

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

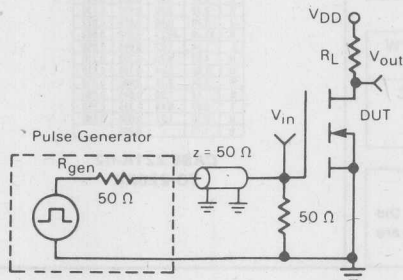
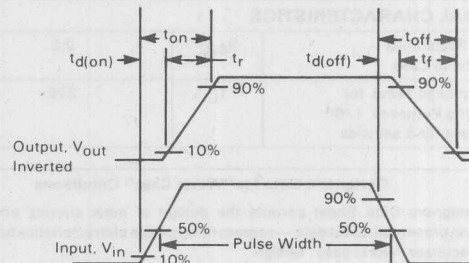


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

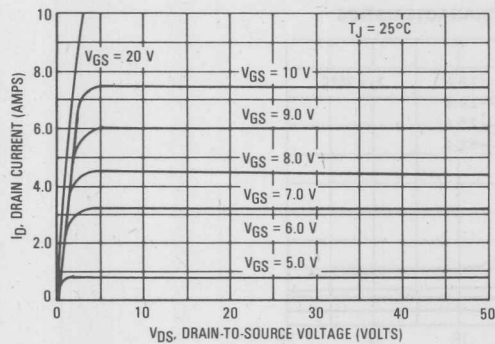


FIGURE 4 — ON-REGION CHARACTERISTICS

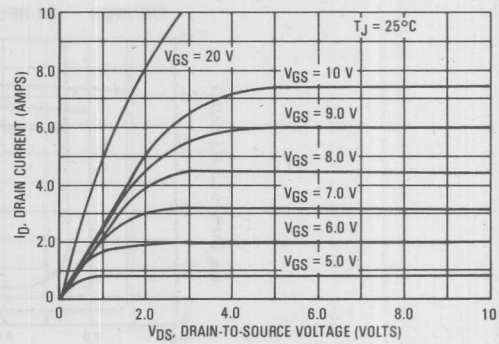


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

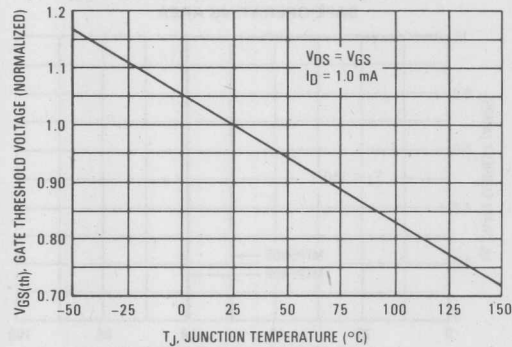


FIGURE 6 — TRANSFER CHARACTERISTICS

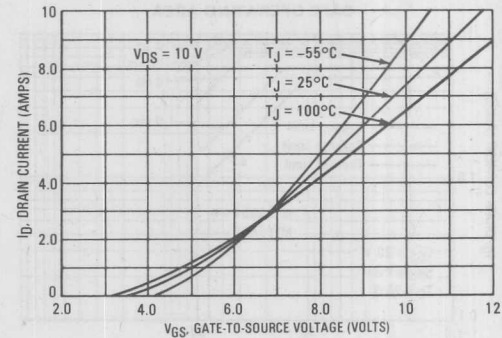


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

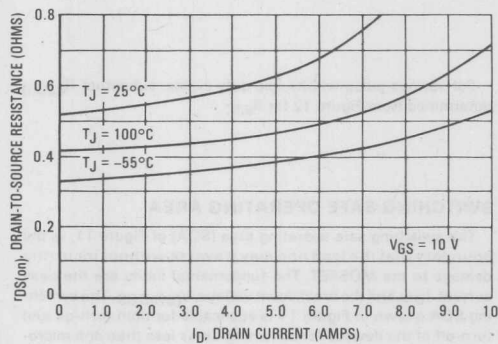
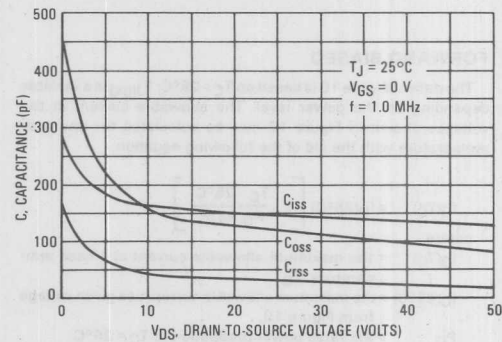


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — ON-REGION CHARACTERISTICS

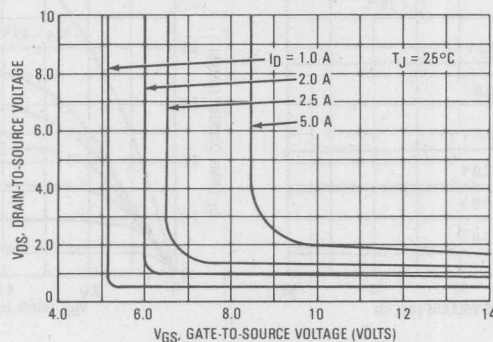


FIGURE 10 — MAXIMUM FORWARD BIASED SAFE OPERATING AREA

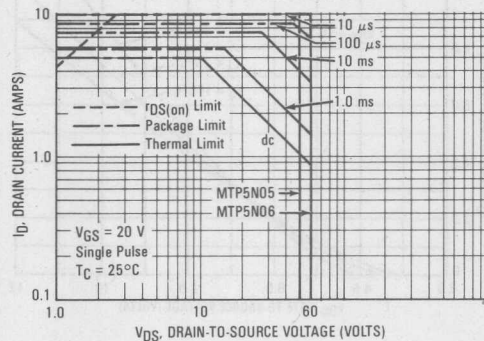
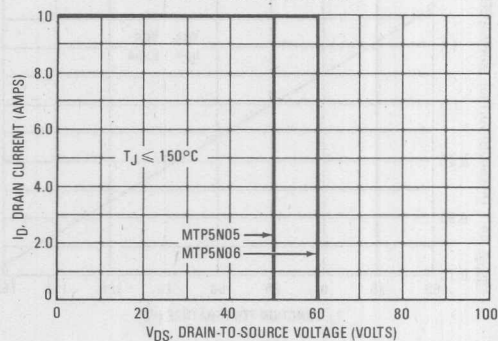


FIGURE 11 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 10 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 10 may be calculated for any case temperature with the aid of the following equation:

$$I_D(T_C) = I_D(25^\circ\text{C}) \left[1 - \frac{T_C - 25^\circ\text{C}}{P_D R_{\theta JC}} \right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C .

$I_D(25^\circ\text{C})$ = the maximum allowable current at a given voltage from Figure 10.

P_D = the rated power dissipation at $T_C = 25^\circ\text{C}$.

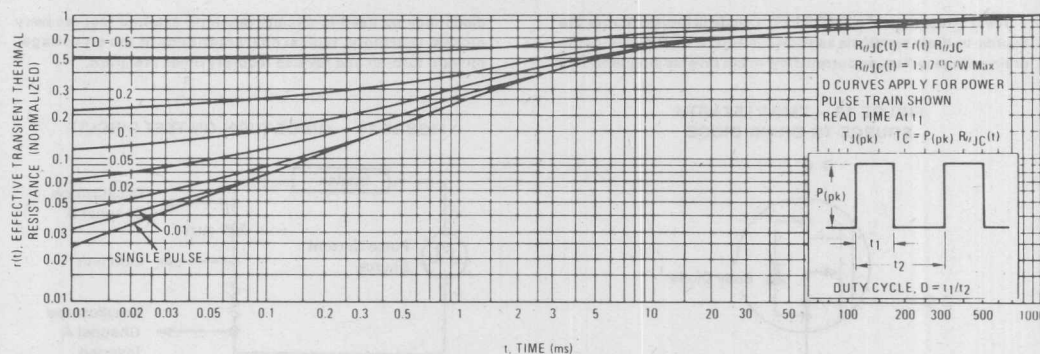
$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figure 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 11, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 11 is applicable for both turn-on and turn-off of the devices for switching times less than one micro-second.

FIGURE 12 — THERMAL RESPONSE



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 1.0 Amp. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ± 20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the

devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

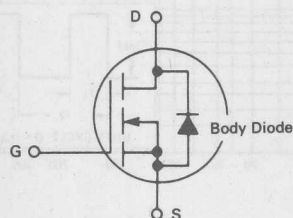
Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 13. Reversal of the drain voltage will cause current flow in the reverse direction. This

FIGURE 13 — TMOS FET WITH SOURCE-TO-DRAIN DIODE



diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 14 — DIODE TURN-ON TEST CIRCUIT

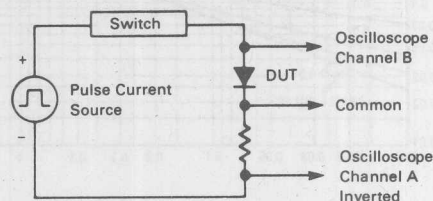


FIGURE 15 — DIODE TURN-ON WAVEFORMS

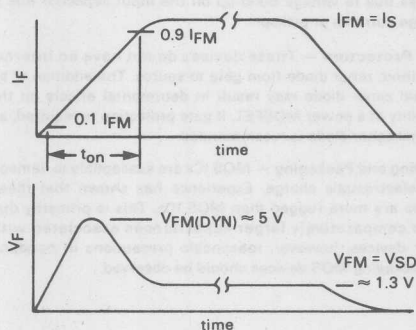


FIGURE 16 — REVERSE RECOVERY CHARACTERISTIC

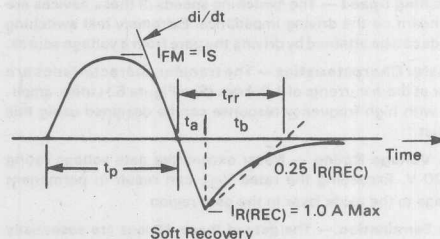
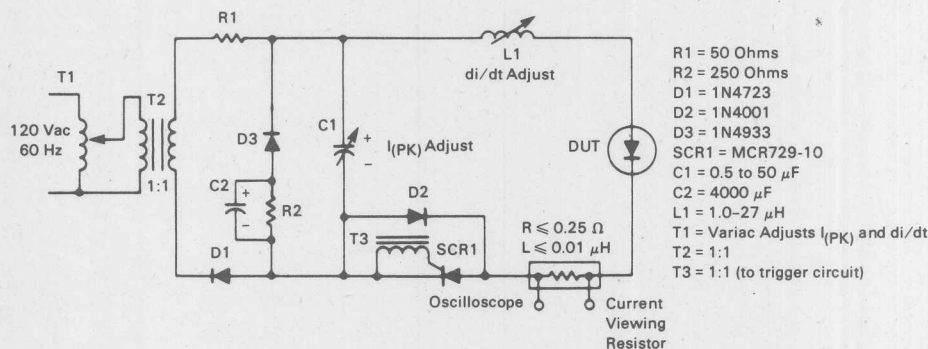


FIGURE 17 — JEDEC REVERSE RECOVERY CIRCUIT





MOTOROLA

**TIP47 TIP48
TIP49 TIP50**

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

... designed for line operated audio output amplifier, Switchmode⁽¹⁾ power supply drivers and other switching applications.

- 250 V to 400 V (Min) - $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Popular TO-220 Plastic Package
- TO-66 Leadform Available

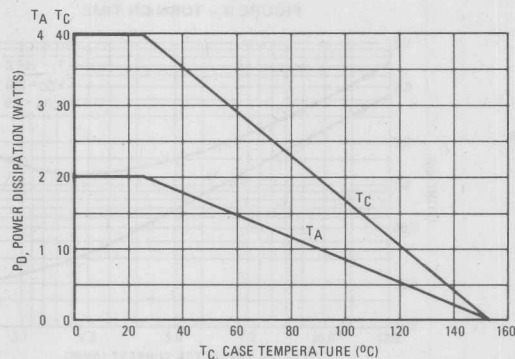
MAXIMUM RATINGS

Rating	Symbol	TIP47	TIP48	TIP49	TIP50	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	400	Vdc
Collector-Base Voltage	V_{CB}	350	400	450	500	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current—Continuous	I_C	1.0				Adc
Peak		2.0				
Base Current	I_B	0.6				Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	40				Watts
Derate above 25°C		0.32				W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.0				Watts
Derate above 25°C		0.016				W/ $^\circ\text{C}$
Unclamped Inducting Load Energy (See Figure 8)	E	20				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

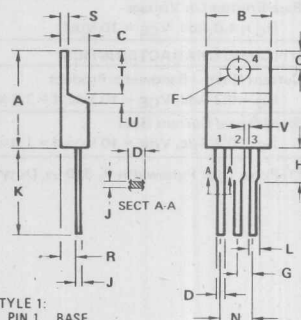
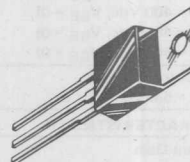
FIGURE 1 — POWER DERATING



1.0 AMPERE

POWER TRANSISTORS NPN SILICON

**250-300-350-400 VOLTS
40 WATTS**



STYLE 1:
PIN 1. BASE
PIN 2. COLLECTOR
PIN 3. EMITTER
PIN 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

**CASE 221A-02
TO-220AB**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 30\text{ mA}$, $I_B = 0$)	TIP47 TIP48 TIP49 TIP50	$V_{CE(sus)}$	250 300 350 400	— — — —	Vdc
Collector Cutoff Current ($V_{CE} = 150\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 200\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 250\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 300\text{ Vdc}$, $I_B = 0$)	TIP47 TIP48 TIP49 TIP50	I_{CEO}	— — — —	1.0 1.0 1.0 1.0	mA
Collector Cutoff Current ($V_{CE} = 350\text{ Vdc}$, $V_{BE} = 0$) ($V_{CE} = 400\text{ Vdc}$, $V_{BE} = 0$) ($V_{CE} = 450\text{ Vdc}$, $V_{BE} = 0$) ($V_{CE} = 500\text{ Vdc}$, $V_{BE} = 0$)	TIP47 TIP48 TIP49 TIP50	I_{CES}	— — — —	1.0 1.0 1.0 1.0	mA
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 0.3\text{ A}$, $V_{CE} = 10\text{ Vdc}$) ($I_C = 1.0\text{ A}$, $V_{CE} = 10\text{ Vdc}$)		h_{FE}	30 10	150 —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0\text{ A}$, $I_B = 0.2\text{ A}$)		$V_{CE(sat)}$	—	1.0	Vdc
Base-Emitter On Voltage ($I_C = 1.0\text{ A}$, $V_{CE} = 10\text{ Vdc}$)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product ($I_C = 0.2\text{ A}$, $V_{CE} = 10\text{ Vdc}$, $f = 2.0\text{ MHz}$)		f_T	10	—	MHz
Small-Signal Current Gain ($I_C = 0.2\text{ A}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ kHz}$)		h_{fe}	25	—	—

(1) Pulse Test: Pulsewidth $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

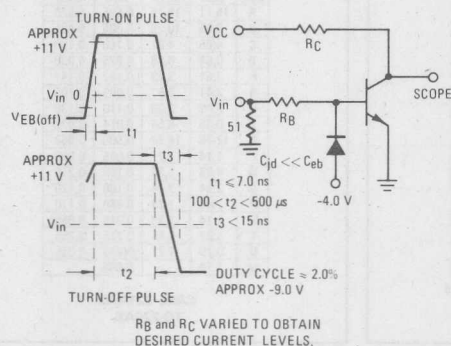


FIGURE 3 – TURN-ON TIME

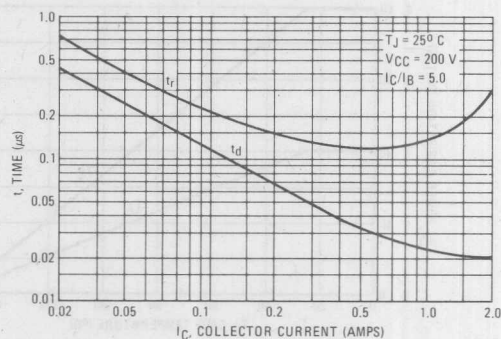


FIGURE 4 — THERMAL RESPONSE

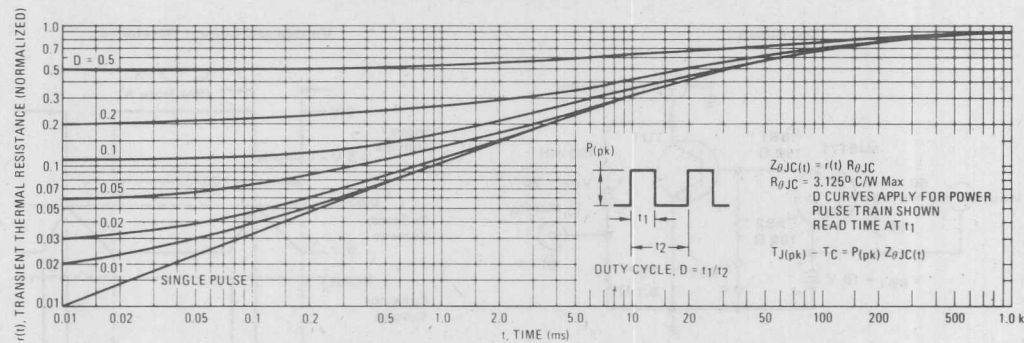
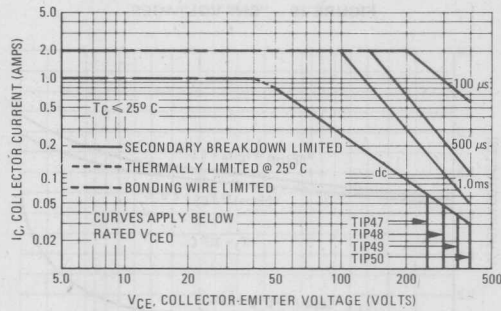


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ \text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ \text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — TURN-OFF TIME

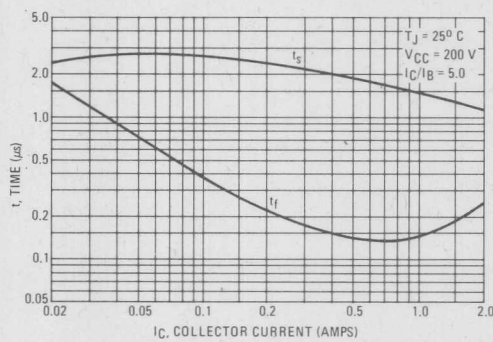


FIGURE 7 — TEMPERATURE COEFFICIENTS

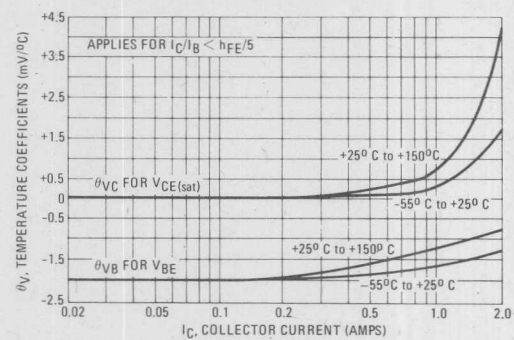
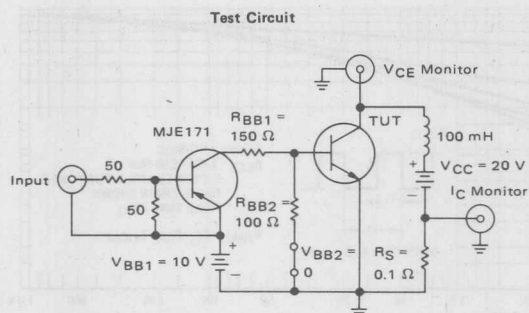


FIGURE 8 – INDUCTIVE LOAD SWITCHING



Note A: Input pulse width is increased until $I_{CM} = 0.63$ A.

Voltage and Current Waveforms

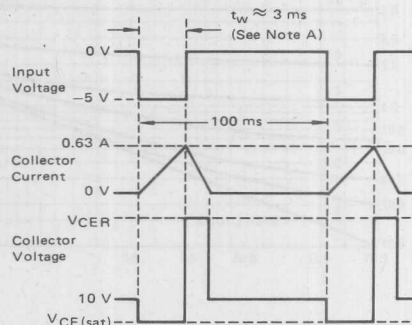


FIGURE 9 – DC CURRENT GAIN

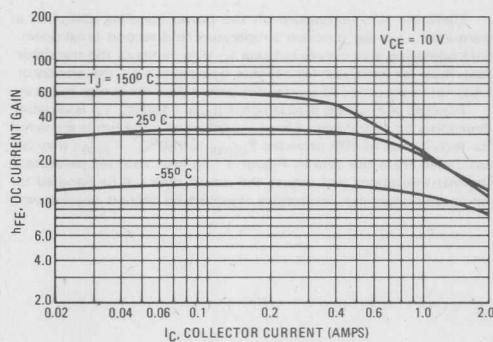
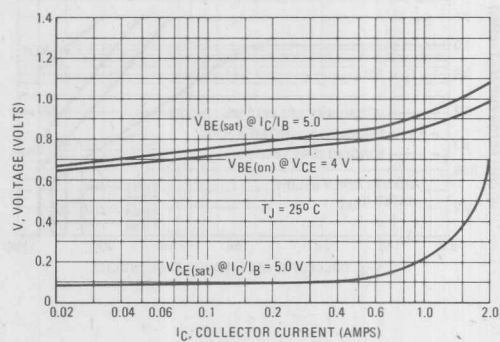


FIGURE 10 – "ON" VOLTAGES





NPN
2N3583
 thru 2N3585, 2N4240
 PNP
2N6420 thru 2N6423

**COMPLEMENTARY MEDIUM-POWER HIGH VOLTAGE
 POWER TRANSISTORS**

... designed for high-speed switching and linear amplifier applications for high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

- Collector-Emitter Sustaining Voltage —
 $V_{CE(sus)} = 175 \text{ to } 300 \text{ Vdc @ } I_C = 200 \text{ mAdc}$
- Second Breakdown Collector Current —
 $I_{S/B} = 350 \text{ mAdc @ } V_{CE} = 100 \text{ Vdc — NPN}$
 $= 150 \text{ mAdc @ } V_{CE} = 100 \text{ Vdc — PNP}$
- Usable DC Current Gain to 2.0 Adc

***MAXIMUM RATINGS**

Rating	Symbol	2N3583 2N6420	2N3584 2N6421	2N3585 2N6422	2N4240 2N6423	Unit
Collector-Emitter Voltage	V _{CEO}	175	250	300	300	V _{dc}
Collector-Base Voltage	V _{CB}	250	375	500	500	V _{dc}
Emitter-Base Voltage	V _{EB}	6.0				V _{dc}
Collector Current — Continuous — Peak	I _C	1.0 5.0	2.0 5.0			A _{dc}
Base Current	I _B	1.0				A _{dc}
Total Power Dissipation @ T _C = 25°C, Derate above 25°C	P _D	35 0.2				Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200				°C

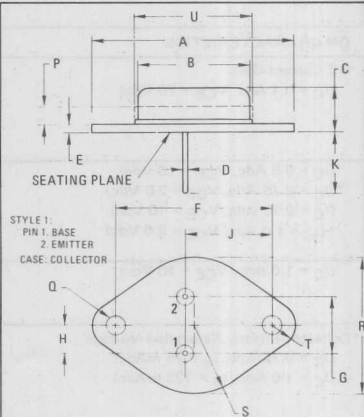
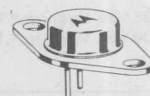
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.0	$^\circ\text{C/W}$

* Indicates JEDEC Registered Data

**1.0 AND 2.0 AMPERE
 POWER TRANSISTORS
 COMPLEMENTARY SILICON**

**250-500 VOLTS
 35 WATTS**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and Notes Apply.

CASE 80-02
 TO-66

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	NPN	PNP	Symbol	NPN		PNP		Unit
				Min	Max	Min	Max	
* OFF CHARACTERISTICS								
Collector-Emitter Sustaining Voltage (I _C = 200 mA _{Dc} , I _B = 0) NPN (I _C = 50 mA _{Dc} , I _B = 0) PNP	2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422 2N6423	V _{CE(sus)}	175 250 300 300	— — — —	175 250 300 300	— — — —	V _{dc}
Collector Cutoff Current (V _{CE} = 150 V _{dc} , I _B = 0)	2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422 2N6423	I _{CEO}	— — — —	10 5.0 5.0 5.0	— — — —	10 5.0 5.0 5.0	mA _{Dc}
Collector Cutoff Current (V _{CE} = 225 V _{dc} , V _{BE(off)} = 1.5 V _{dc}) (V _{CE} = 340 V _{dc} , V _{BE(off)} = 1.5 V _{dc}) (V _{CE} = 450 V _{dc} , V _{BE(off)} = 1.5 V _{dc}) (V _{CE} = 225 V _{dc} , V _{BE(off)} = 1.5 V _{dc} , T _C = 150°C) (V _{CE} = 300 V _{dc} , V _{BE(off)} = 1.5 V _{dc} , T _C = 150°C)	2N3583 2N3584 2N3585 2N4240 2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422 2N6423 2N6420 2N6421 2N6422 2N6423	I _{CEX}	— — — — — — — —	1.0 1.0 1.0 2.0 3.0 3.0 3.0 5.0	— — — — — — — —	1.0 1.0 1.0 2.0 3.0 3.0 3.0 5.0	mA _{Dc}
Emitter Cutoff Current (V _{BE} = 6.0 V _{dc} , I _C = 0)	2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422 2N6423	I _{EBO}	— — — —	5.0 0.5 0.5 0.5	— — — —	5.0 0.5 0.5 0.5	mA _{Dc}
ON CHARACTERISTICS								
DC Current Gain (I _C = 0.1 A _d , V _{CE} = 10 V _{dc})	2N3583* 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422 2N6423	h _{FE}	40 40 40 40	— — — —	40 40 40 40	— — — —	—
* (I _C = 0.5 A _d , V _{CE} = 10 V _{dc}) * (I _C = 0.75 A _d , V _{CE} = 2.0 V _{dc}) (I _C = 0.75 A _d , V _{CE} = 10 V _{dc}) * (I _C = 1.0 A _d , V _{CE} = 2.0 V _{dc})	2N3583 2N4240 2N4240 2N3584 2N3585	2N6420 2N6423 2N6423 2N6421 2N6422		40 10 30 8.0 8.0	200 100 150 80 80	40 10 30 8.0 8.0	200 100 150 80 80	
(I _C = 1.0 A _d , V _{CE} = 10 V _{dc})	2N3583* 2N3584 2N3585	2N6420 2N6421 2N6422		10 25 25	— 100 100	10 25 25	— 100 100	
* Collector-Emitter Saturation Voltage (I _C = 0.75 A _d , I _B = 75 mA _d) (I _C = 1.0 A _d , I _B = 125 mA _d)	2N4240 2N3583 2N3584 2N3585	2N6423 2N6420 2N6421 2N6422	V _{CE(sat)}	— — — —	1.0 5.0 0.75 0.75	— — — —	1.0 5.0 0.75 0.75	V _{dc}
* Base-Emitter Saturation Voltage (I _C = 0.75 A _d , I _B = 75 mA _d) (I _C = 1.0 A _d , I _B = 100 mA _d)	2N4240 2N3584 2N3585	2N6423 2N6421 2N6422	V _{BE(sat)}	— — —	1.8 1.4 1.4	— — —	1.8 1.4 1.4	V _{dc}
Base-Emitter On Voltage (I _C = 1.0 A _d , V _{CE} = 10 V _{dc})	2N3583* 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422 2N6423	V _{BE(on)}	— — — —	1.4 1.4 1.4 1.4	— — — —	1.4 1.4 1.4 1.4	V _{dc}

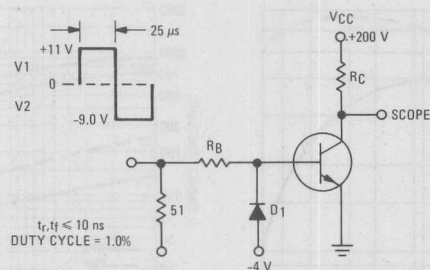
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	NPN	PNP	Symbol	NPN		PNP		Unit								
				Min	Max	Min	Max									
DYNAMIC CHARACTERISTICS																
*Current Gain – Bandwidth Product ⁽¹⁾ (I _C = 200 mAdc, V _{CE} = 10 Vdc, f _{test} = 5.0 MHz)	2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422 2N6423	f _T	10 15	— —	10 15	— —	MHz								
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz)	All		C _{Ob}	—	120	—	120	pF								
*Small-Signal Current Gain (I _C = 100 mAdc, V _{CE} = 30 Vdc, f = 1.0 kHz)	2N3583	2N6420	h _{fe}	25	350	25	350	—								
*SWITCHING CHARACTERISTICS																
Rise Time (V _{CC} = 200 Vdc, I _C = 1.0 Adc, R _L = 200 Ohms, I _{B1} = 100 mAdc) (V _{CC} = 200 Vdc, I _C = 0.75 Adc, R _L = 267 Ohms, I _{B1} = 75 mAdc)	2N3584 2N3585 2N4240	2N6421 2N6422 2N6423	t _r	— —	3.0 0.5	— —	3.0 0.5	μs								
Storage Time (V _{CC} = 200 Vdc, I _C = 1.0 Adc, I _{B1} = I _{B2} = 100 mAdc) (V _{CC} = 200 Vdc, I _C = 0.75 Adc, I _{B1} = I _{B2} = 75 mAdc)	2N3584 2N3585 2N4240	2N6421 2N6422 2N6423	t _s	— —	4.0 6.0	— —	4.0 6.0	μs								
Fall Time (V _{CC} = 200 Vdc, I _C = 1.0 Adc, I _{B1} = I _{B2} = 100 mAdc) (V _{CC} = 200 Vdc, I _C = 0.75 Adc, I _{B1} = I _{B2} = 75 mAdc)	2N3584 2N3585 2N4240	2N6421 2N6422 2N6423	t _f	— —	3.0 3.0	— —	3.0 3.0	μs								
Second Breakdown Collector Current (V _{CE} = 100 Vdc)									All	All	I _{s/b}	350	—	150	—	mAdc

*Indicates JEDEC Registered Data

(1) $f_T = |h_{fe}| \cdot f_{\text{test}}$

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:

MBD5300 USED ABOVE $I_B \approx 100\text{ mA}$

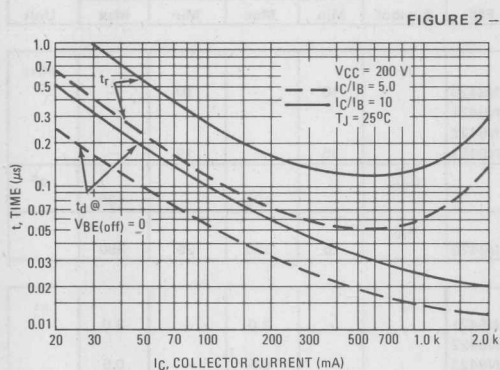
MSD6100 USED BELOW $I_B \approx 100\text{ mA}$

FOR t_d and t_r , D_1 IS DISCONNECTED AND $V_2 = 0$.

FOR PNP TEST CIRCUIT, REVERSE DIODE AND VOLTAGE POLARITIES.

2N3583 thru 2N3585 • 2N4240 – NPN
2N6420 thru 2N6423 – PNP

NPN
2N3583 thru 2N3585, 2N4240



PNP
2N6420 thru 2N6423

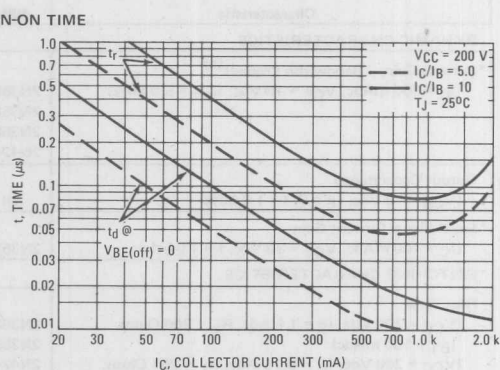


FIGURE 3 – TURN-OFF TIME

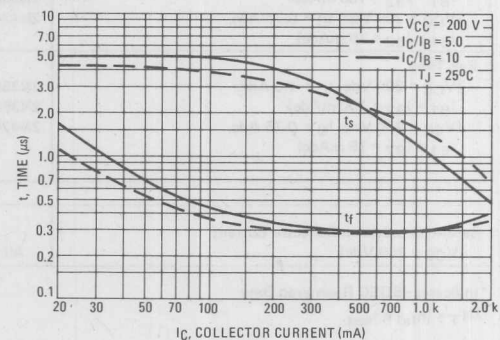
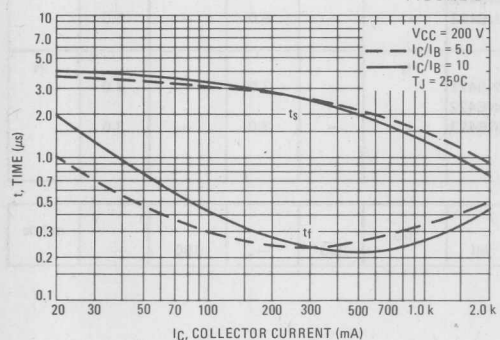


FIGURE 4 – CURRENT-GAIN – BANDWIDTH PRODUCT

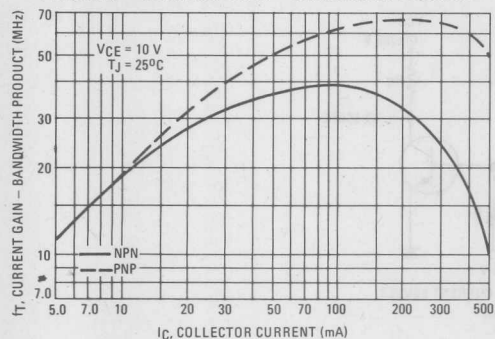


FIGURE 5 – CAPACITANCE

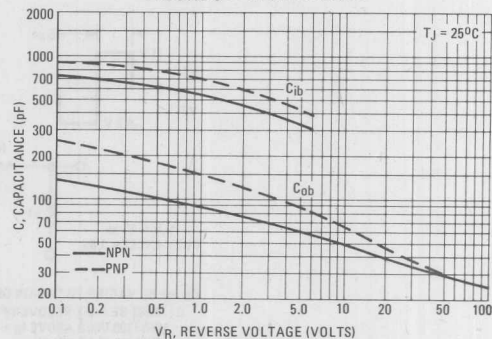
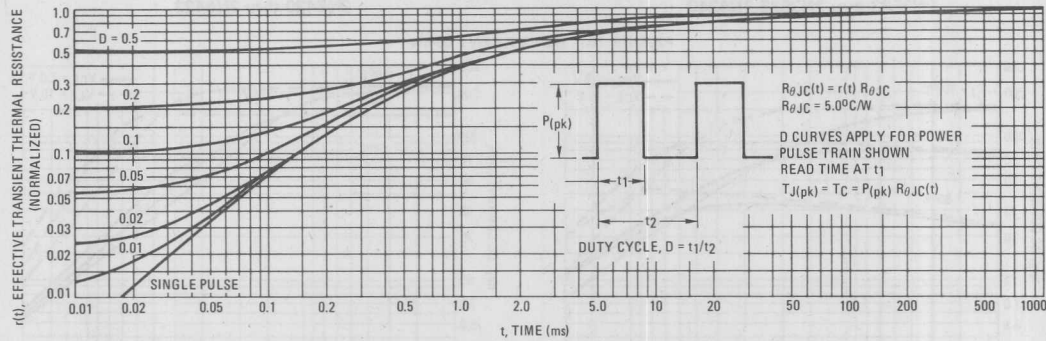


FIGURE 6 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 7 – 2N3583 thru 2N3585, 2N4240

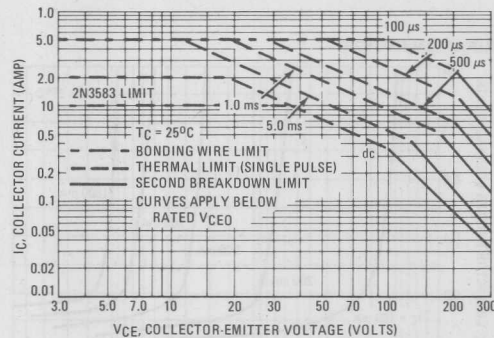


FIGURE 8 – 2N6420 thru 2N6423

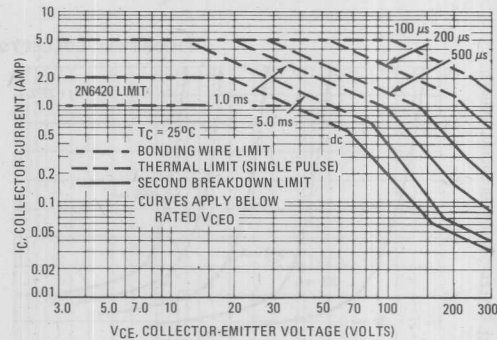
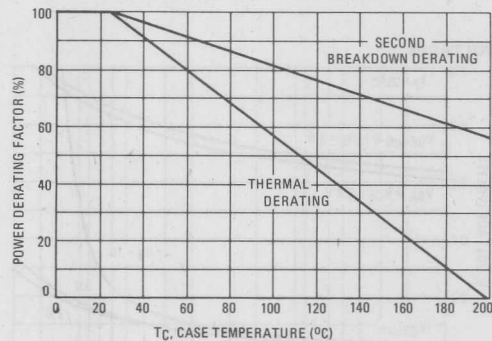


FIGURE 9 – POWER DERATING



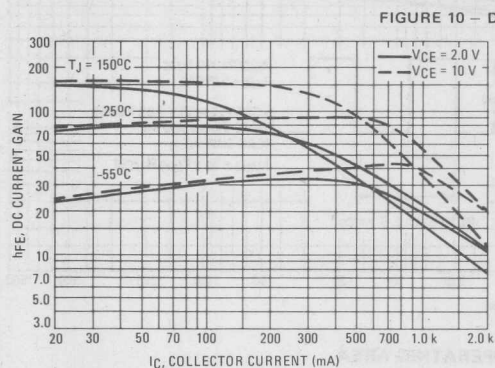
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 7 and 8 is based on $T_C = 25^\circ C$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 9.

$T_J(pk)$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 7 and 8 may be found at any case temperature by using the appropriate curve on Figure 9.

2N3583 thru 2N3585 • 2N4240 – NPN
2N6420 thru 2N6423 – PNP

NPN
2N3583 thru 2N3585, 2N4240



PNP
2N6420 thru 2N6423

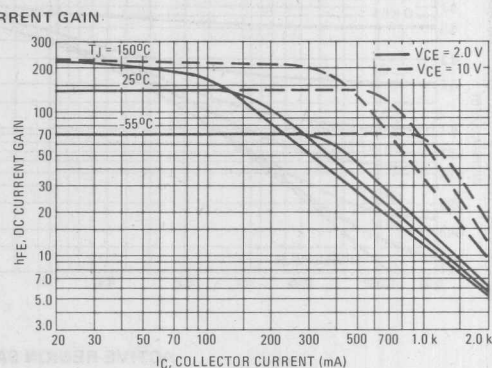


FIGURE 11 – COLLECTOR SATURATION REGION

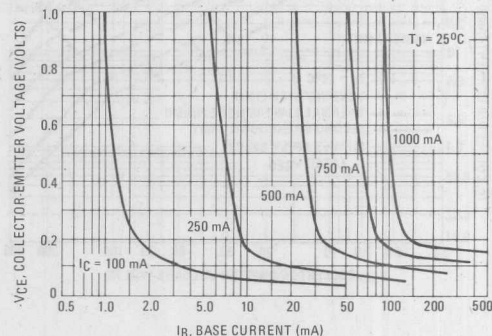
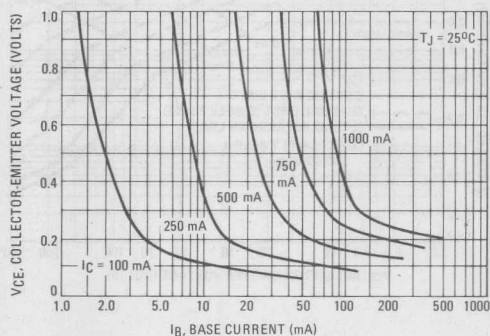
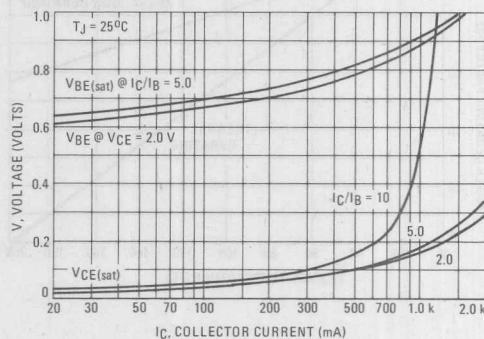
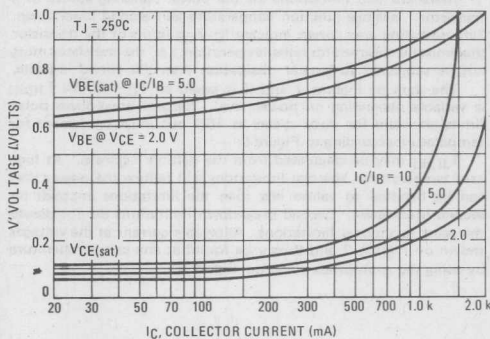


FIGURE 12 – "ON" VOLTAGES



NOTE: DC CURRENT LIMIT FOR 2N3583, 2N6420 is 1.0 Amp.

NPN
2N3583 thru 2N3585, 2N4240

PNP
2N6420 thru 2N6423

FIGURE 13 – TEMPERATURE COEFFICIENTS

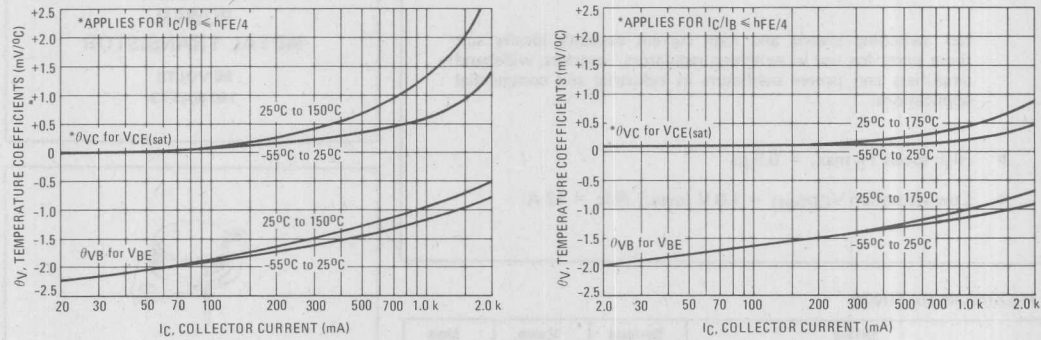


FIGURE 14 – COLLECTOR CUTOFF REGION

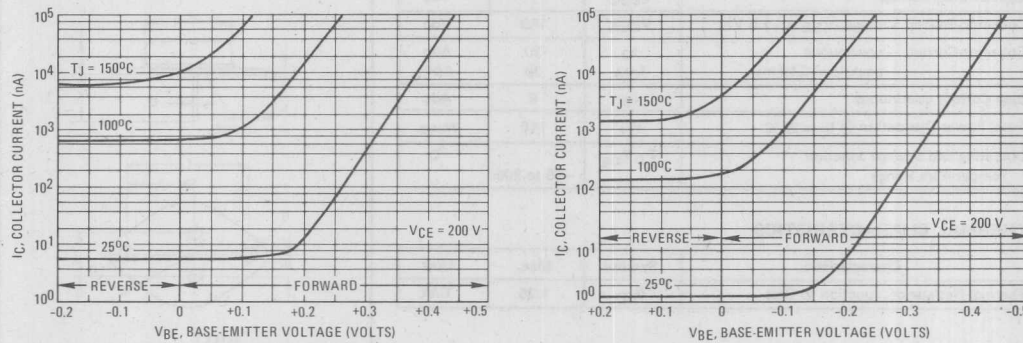
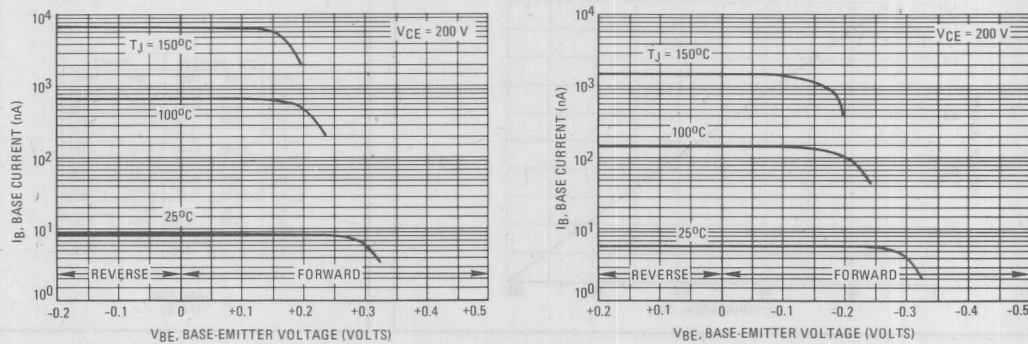


FIGURE 15 – BASE CUTOFF REGION



**MOTOROLA****2N5038****NPN SILICON POWER TRANSISTOR**

... fast switching speeds and high current capacity ideally suit these parts for use in switching regulators, inverters, wideband amplifiers and power oscillators in industrial and commercial applications.

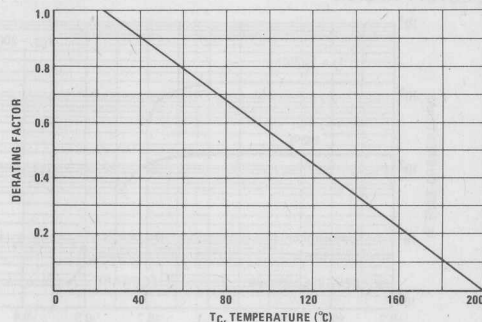
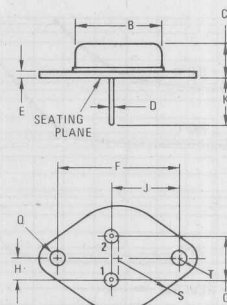
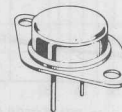
- High speed T_F max. = $0.5 \mu s$
- Low saturation $V_{CE(sat)} = 1.0 V$ (max.) @ $I_C = 12 A$

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	90	Vdc
Collector-Base Voltage	V_{CBO}	150	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5 V$)	V_{CEX}	150	Vdc
Collector-Current — continuous	I_C	20	Adc
— peak ($p_w \leq 10 ms$)	I_{CM}	30	Apk
Base-Current continuous	I_B	5	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	140	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.25	$^\circ C/W$

FIGURE 1 — POWER DERATING**20 AMPERES****NPN SILICON
POWER
METAL TRANSISTOR****90 VOLTS
140 WATTS**

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
----------------	--------	------	------	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 15\text{ mH}$) ($I_C = 200\text{ mA}$, $V_{BE} = -1.5\text{ V}$, $R_{BE} = 100\ \Omega$, $L = 2\text{ mH}$) ($I_C = 200\text{ mA}$, $R_{BE} = 50\ \Omega$, $L = 15\text{ mH}$)	$V_{CEO(sus)}$ $V_{CEX(sus)}$ $V_{CER(sus)}$	90 150 110		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 140\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 100\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	50 10		mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 70\text{ V}$)	I_{CEO}	20		mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7.0		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}	5.0		mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 28\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 45\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	5 0.9		Adc
Second Breakdown Energy ($V_{BE} = 4\text{ V}$, $R_{BE} = 20\ \Omega$) ($I_C = 12\text{ A}$, $L = 180\ \mu\text{H}$)	$E_{S/b}$	13		mJ

ON CHARACTERISTICS

DC Current Gain ($I_C = 2\text{ Adc}$, $V_{CE} = 5\text{ V}$) ($I_C = 12\text{ Adc}$, $V_{CE} = 5\text{ V}$)	h_{FE}	50 20	250 100	—
Collector-Emitter Saturation Voltage ($I_C = 12\text{ Adc}$, $I_B = 1.2\text{ A}$) ($I_C = 20\text{ Adc}$, $I_B = 5\text{ A}$)	$V_{CE(sat)}$		1.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 5\text{ A}$)	$V_{BE(sat)}$		3.3	Vdc

DYNAMIC CHARACTERISTICS

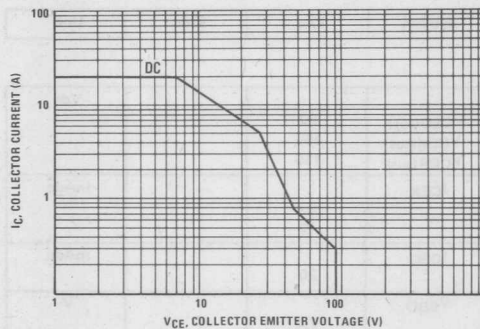
Forward Current Transfert Ratio ($V_{CE} = 10\text{ V}$, $I_C = 2\text{ A}$, $f = 5\text{ MHz}$)	$ h_{FE} $	12	—	
Output Capacitance ($V_{CB} = 10\text{ V}$, $f = 1\text{ MHz}$)		—	300	pF

SWITCHING CHARACTERISTICS (Resistive Load)

Rise Time	$(V_{CC} = 30\text{ Vdc}$, $I_C = 12\text{ A}$, $I_{B1} = 1.2\text{ A}$, $I_{B2} = 1.2\text{ A}$)	t_r	—	0.5	μs
Storage Time		t_s	—	1.5	
Fall Time		t_f	—	0.5	

(1) Pulse Test: Pulse Width = $300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

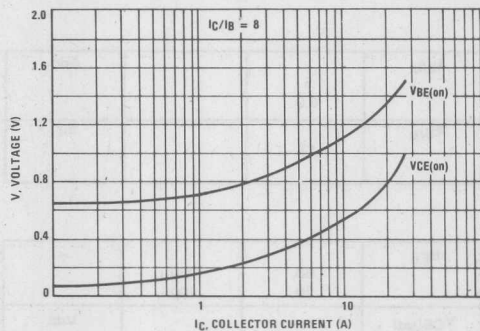


FIGURE 4 – DC CURRENT GAIN

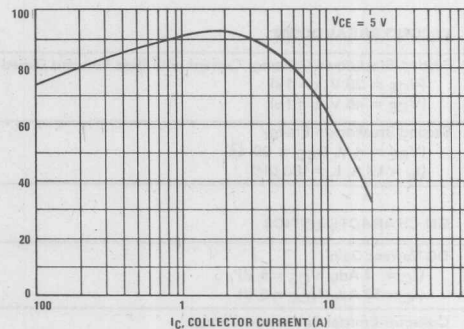


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

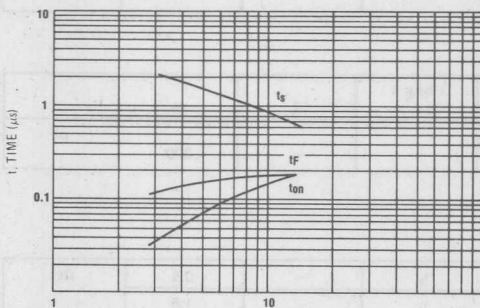
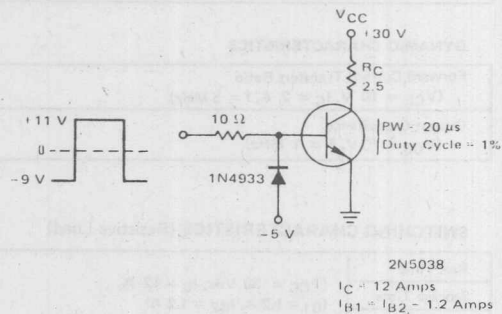


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT





MOTOROLA

2N5039

NPN SILICON POWER TRANSISTOR

... fast switching speeds and high current capacity ideally suit these parts for use in switching regulators, inverters, wideband amplifiers and power oscillators in industrial and commercial applications.

- High speed T_F max. = $0.5 \mu s$
- Low saturation $V_{CE(sat)} = 1.0 V$ (max.) @ $I_C = 10 A$

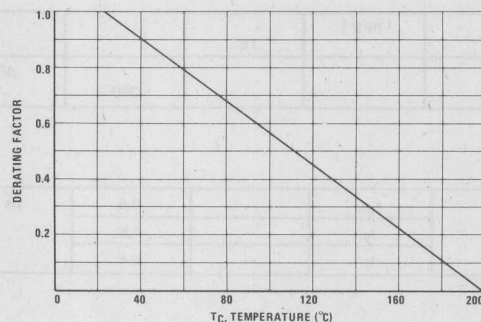
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	75	Vdc
Collector-Base Voltage	V_{CBO}	120	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5 V$)	V_{CEX}	120	Vdc
Collector-Current — continuous	I_C	20	Adc
— peak* ($p_w \leq 10 ms$)	I_{CM}	30	Apk
Base-Current continuous	I_B	5	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	140	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.25	$^\circ C/W$

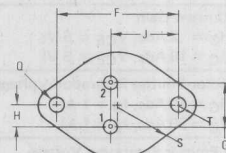
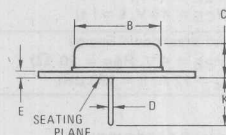
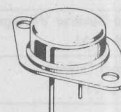
FIGURE 1 — POWER DERATING



20 AMPERES

NPN SILICON POWER METAL TRANSISTOR

**75 VOLTS
140 WATTS**



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
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G	10.67	11.18	0.420	0.440
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J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO 3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 15\text{ mH}$) ($I_C = 200\text{ mA}$, $V_{BE} = -1.5\text{ V}$, $R_{BE} = 100\ \Omega$, $L = 2\text{ mH}$) ($I_C = 200\text{ mA}$, $R_{BE} = 50\ \Omega$, $L = 15\text{ mH}$)	$V_{CEO(sus)}$ $V_{CEX(sus)}$ $V_{CER(sus)}$	75 120 95		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 140\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 100\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	50 10		mA _{dc}
Collector-Emitter Cutoff Current ($V_{CE} = 70\text{ V}$)	I_{CEO}	20		mA _{dc}
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7.0		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}	15		mA _{dc}

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 28\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 45\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	5 0.9		A _{dc}
Second Breakdown Energy ($V_{BE} = 4\text{ V}$, $R_{BE} = 20\ \Omega$) ($I_C = 12\text{ A}$, $L = 180\ \mu\text{H}$)	$E_{S/b}$	13		mJ

ON CHARACTERISTICS

DC Current Gain ($I_C = 2\text{ A}$, $V_{CE} = 5\text{ V}$) ($I_C = 10\text{ A}$, $V_{CE} = 5\text{ V}$)	h_{FE}	50 20	250 100	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 1\text{ A}$) ($I_C = 20\text{ A}$, $I_B = 1\text{ A}$)	$V_{CE(sat)}$		1.0 2.5	V _{dc}
Base-Emitter Saturation Voltage ($I_C = 20\text{ A}$, $I_B = 5\text{ A}$)	$V_{BE(sat)}$		3.3	V _{dc}

DYNAMIC CHARACTERISTICS

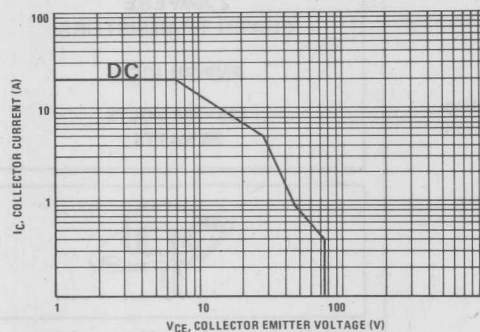
Forward Current Transfer Ratio ($V_{CE} = 10\text{ V}$, $I_C = 2\text{ A}$, $f = 5\text{ MHz}$)	$ h_{FE} $	12		
Output Capacitance ($V_{CB} = 10\text{ V}$, $F = 1\text{ MHz}$)			300	pF

SWITCHING CHARACTERISTICS (Resistive Load)

Rise Time	$(V_{CC} = 30\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{B1} = 1.0\text{ A}$, $I_{B2} = 1.0\text{ A}$)	t_{on}	—	0.5	μs
Storage Time		t_s	—	1.5	
Fall Time		t_f	—	0.5	

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 — "ON" VOLTAGES

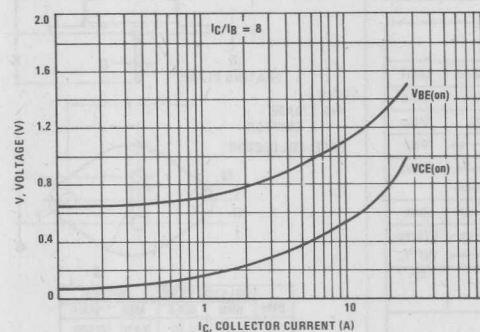


FIGURE 4 — DC CURRENT GAIN

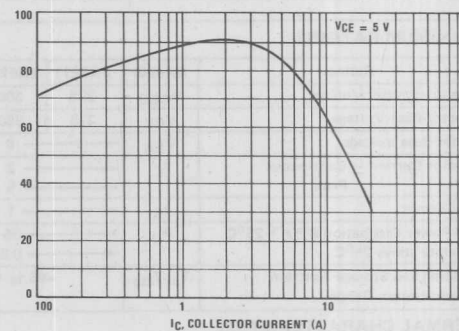


FIGURE 5 — RESISTIVE SWITCHING PERFORMANCE

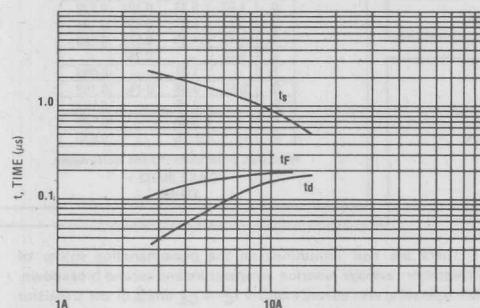
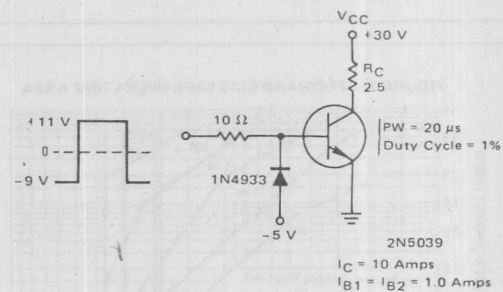


FIGURE 6 — SWITCHING TIMES TEST CIRCUIT



MEDIUM-POWER HIGH-VOLTAGE PNP POWER TRANSISTORS

... designed for high-speed switching and linear amplifier applications for high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

- Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 225 \text{ to } 350 \text{ Vdc @ } I_C = 200 \text{ mAdc}$
- Second Breakdown Collector Current –
 $I_{S/b} = 875 \text{ mAdc @ } V_{CE} = 40 \text{ Vdc}$
- $t_f = 0.6 \mu\text{s}$ Resistive Fall Time
- Usable DC Current Gain to 2.0 Adc

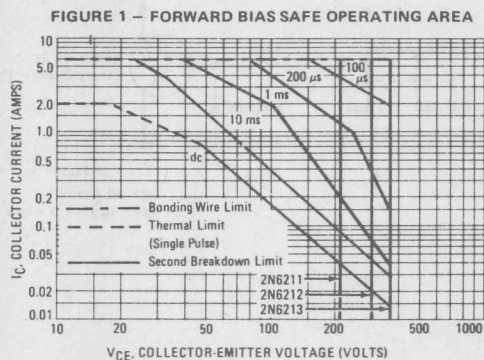
*MAXIMUM RATINGS

Rating	Symbol	2N6211	2N6212	2N6213	Unit
Collector-Emitter Voltage	V_{CEO}	225	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	350	400	Vdc
Emitter-Base Voltage	V_{EB}	6			Vdc
Collector Current – Continuous	I_C	2			Adc
Peak		5			
Base Current	I_B	1			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	35			Watts
Derate above 25°C		0.2			W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	$^\circ\text{C/W}$

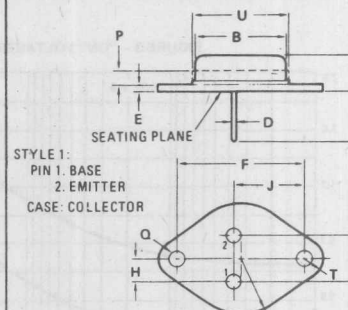
*Indicates JEDEC Registered Data.



2 AMPERE POWER TRANSISTORS

PNP SILICON

225–350 VOLTS
35 WATTS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-66

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 200$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See Figure 8).

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (1) ($I_C = 200\text{ mA}$, $I_B = 0$)	2N6211 2N6212 2N6213	$V_{CEO(sus)}$	225 300 350	— — —	Vdc
*Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $V_{BE} = -1.5\text{ V}$, $L = 10\text{ mH}$)	2N6211 2N6212 2N6213	$V_{CEX(sus)}$	275 350 400	— — —	Vdc
*Collector-Emitter Sustaining Voltage (1) ($I_C = 200\text{ mA}$, $I_B = 0$, $R_{BE} = 50\ \Omega$)	2N6211 2N6212 2N6213	$V_{CER(sus)}$	250 325 375	— — —	Vdc
*Emitter-Base Breakdown Voltage (1) ($I_E = 0.5\text{ mA}$, $I_C = 0$) ($I_E = 1.0\text{ mA}$, $I_C = 0$)	2N6212/13 2N6211	V_{EBO}	6.0 6.0	— —	Vdc
*Collector Cutoff Current ($V_{CE} = 250\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 25^\circ\text{C}$) ($T_C = 100^\circ\text{C}$) ($V_{CE} = 315\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 25^\circ\text{C}$) ($T_C = 100^\circ\text{C}$) ($V_{CE} = 360\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 25^\circ\text{C}$) ($T_C = 100^\circ\text{C}$)		I_{CEV}	— — — — — —	0.5 5.0 0.5 5.0 0.5 5.0	mAdc
Collector Cutoff Current ($V_{CE} = 150\text{ Vdc}$, $I_B = 0$)	All Types	I_{CEO}	—	5.0	mAdc
*Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	2N6211 2N6212 2N6213	I_{EBO}	— — —	1.0 0.5 0.5	mAdc
*ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 1.0\text{ Adc}$, $V_{CE} = 2.8\text{ Vdc}$) ($I_C = 1.0\text{ Adc}$, $V_{CE} = 3.2\text{ Vdc}$) ($I_C = 1.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	2N6211 2N6212 2N6213	h_{FE}	10 10 10	100 100 100	—
Collector-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 125\text{ mAdc}$)	2N6211 2N6212 2N6213	$V_{CE(sat)}$	— — —	1.4 1.6 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 125\text{ mAdc}$)	All Types	$V_{BE(sat)}$	—	1.4	Vdc
DYNAMIC CHARACTERISTICS					
*Current Gain—Bandwidth Product (2) ($I_C = 200\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 5.0\text{ MHz}$)		f_T	20	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$)		C_{ob}	—	220	pF
*SECOND BREAKDOWN					
*Second Breakdown Collector Current with Base Forward Biased $t = 1.0\text{ s}$ (non-repetitive) ($V_{CE} = 40\text{ Vdc}$)		$I_{S/b}$	0.875	—	Adc
*SWITCHING CHARACTERISTICS					
Rise Time	(V _{CC} = 200 Vdc, $I_C = 1.0\text{ Adc}$, $I_{B1} = I_{B2} = 0.125\text{ Adc}$)	t_r	—	0.6	μs
Storage Time		t_s	—	2.5	μs
Fall Time		t_f	—	0.6	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $< 300\ \mu\text{s}$, Duty Cycle $< 2.0\%$

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

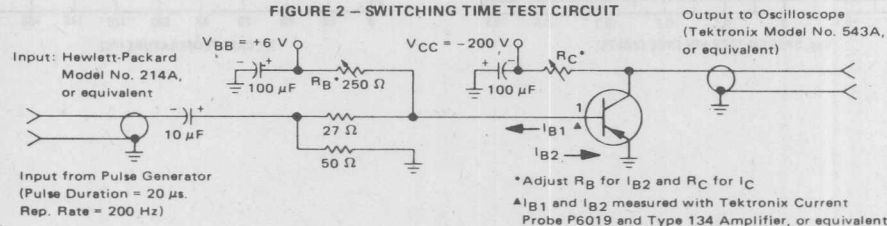


FIGURE 3 - DC CURRENT GAIN

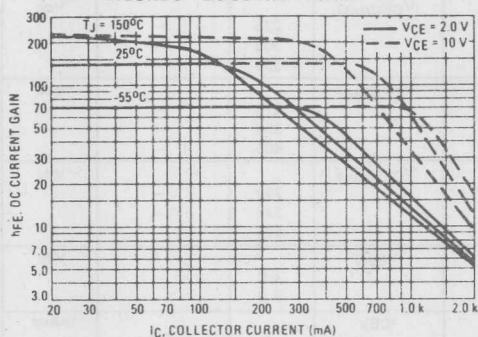


FIGURE 4 - COLLECTOR SATURATION REGION

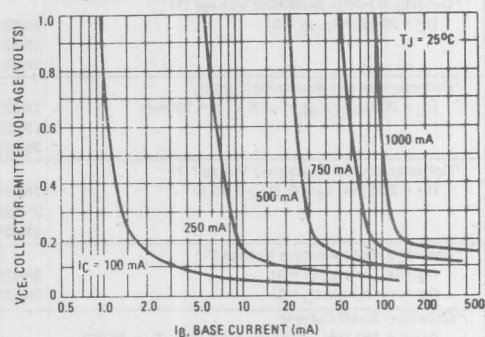


FIGURE 5 - COLLECTOR CUTOFF REGION

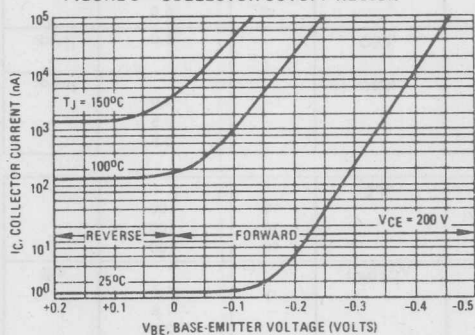


FIGURE 6 - TEMPERATURE COEFFICIENTS

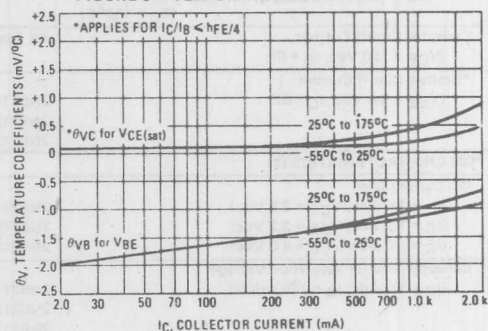


FIGURE 7 - BASE CUTOFF REGION

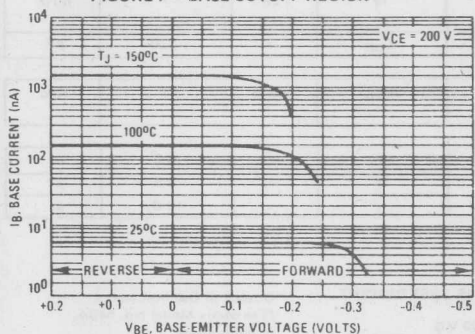


FIGURE 8 - POWER DERATING

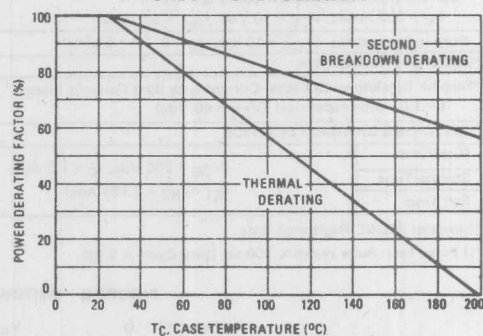


FIGURE 9 - CURRENT-GAIN-BANDWIDTH PRODUCT

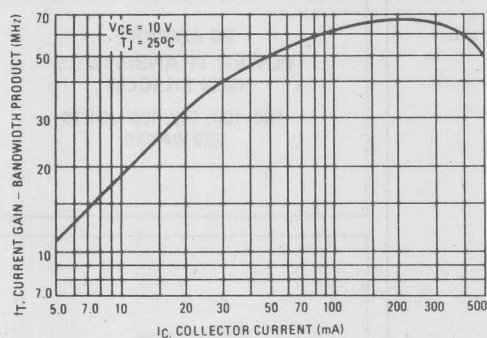


FIGURE 10 - TURN-ON TIME

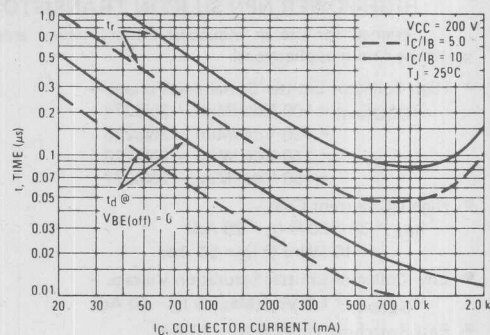


FIGURE 11 - TURN-OFF TIME

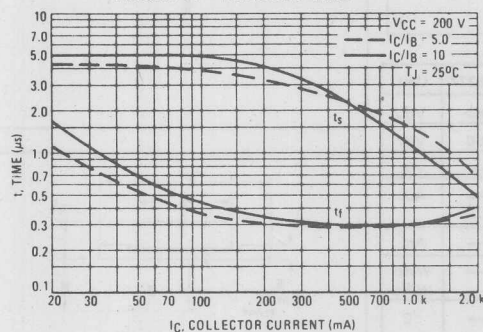


FIGURE 12 - CAPACITANCE

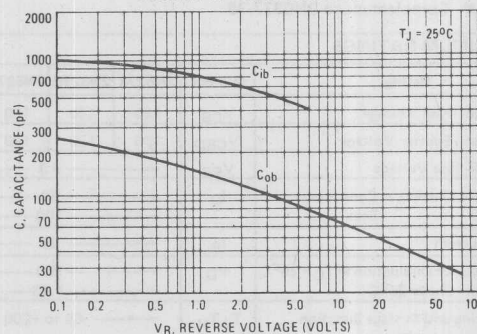
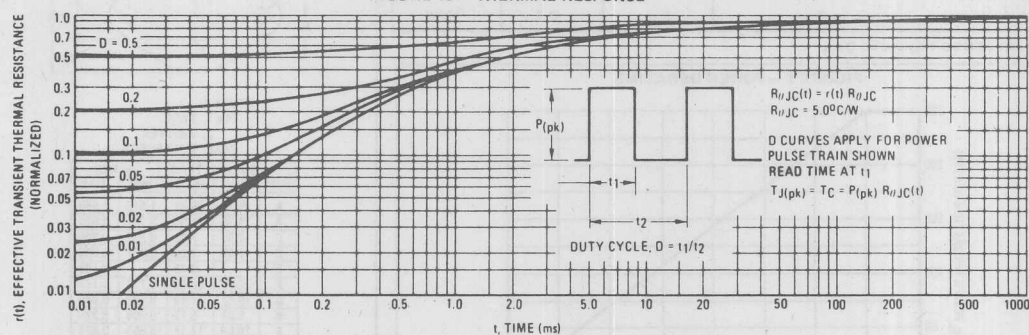


FIGURE 13 - THERMAL RESPONSE



HIGH-POWER NPN SILICON TRANSISTORS

... designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 100 \text{ Vdc (Min)} - 2N6274$
 $= 120 \text{ Vdc (Min)} - 2N6275$
 $= 140 \text{ Vdc (Min)} - 2N6276$
 $= 150 \text{ Vdc (Min)} - 2N6277$
- High DC Current Gain –
 $h_{FE} = 30-120 @ I_C = 20 \text{ Adc}$
 $= 10 \text{ (Min)} @ I_C = 50 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max)} @ I_C = 20 \text{ Adc}$
- Fast Switching Times @ $I_C = 20 \text{ Adc}$
 $t_r = 0.35 \mu\text{s (Max)}$
 $t_s = 0.8 \mu\text{s (Max)}$
 $t_f = 0.25 \mu\text{s (Max)}$
- Complement to 2N6377-79

*MAXIMUM RATINGS

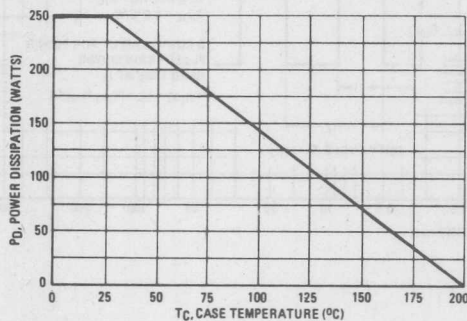
Rating	Symbol	2N6274	2N6275	2N6276	2N6277	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	6.0				Vdc
Collector Current – Continuous	I_C	50				Adc
Peak		100				
Base Current	I_B	20				Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250				Watts
Derate above 25°C		1.43				$\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C}/\text{W}$

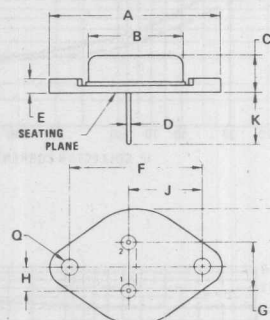
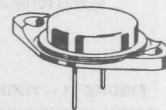
*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



50 AMPERE POWER TRANSISTORS NPN SILICON

100, 120, 140, 150 VOLTS
250 WATTS



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 50 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	100 120 140 150	— — — —	Vdc
Collector Cutoff Current ($V_{CE} = 50 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	50	μAdc
($V_{CE} = 60 \text{ Vdc}$, $I_B = 0$)		—	50	
($V_{CE} = 70 \text{ Vdc}$, $I_B = 0$)		—	50	
($V_{CE} = 75 \text{ Vdc}$, $I_B = 0$)		—	50	
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CB}$, $V_{EB(off)} = 1.5 \text{ Vdc}$)	I_{CEX}	—	10	μAdc
($V_{CE} = \text{Rated } V_{CB}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)		—	1.0	mAdc
Emitter Cutoff Current ($V_{BE} = 6.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	100	μAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 20 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 50 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	50 30 10	— 120 —	—
Collector-Emitter Saturation Voltage ($I_C = 20 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 10 \text{ Adc}$)	$V_{CE(sat)}$	— —	1.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 20 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 10 \text{ Adc}$)	$V_{BE(sat)}$	— —	1.8 3.5	Vdc
Base-Emitter On Voltage ($I_C = 20 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.8	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product (2) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{\text{test}} = 10 \text{ MHz}$)	f_T	30	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	—	600	pF

SWITCHING CHARACTERISTICS

Rise Time ($V_{CC} = 80 \text{ Vdc}$, $I_C = 20 \text{ Adc}$, $I_{B1} = 2.0 \text{ Adc}$, $V_{BE(off)} = 5.0 \text{ Vdc}$)	t_r	—	0.35	μs
Storage Time ($V_{CC} = 80 \text{ Vdc}$, $I_C = 20 \text{ Adc}$, $I_{B1} = I_{B2} = 2.0 \text{ Adc}$)	t_s	—	0.80	μs
Fall Time ($V_{CC} = 80 \text{ Vdc}$, $I_C = 20 \text{ Adc}$, $I_{B1} = I_{B2} = 2.0 \text{ Adc}$)	t_f	—	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.(2) $f_T = h_{fe} \cdot f_{\text{test}}$.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

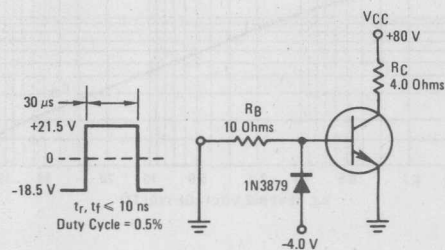
Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 — TURN-ON TIME

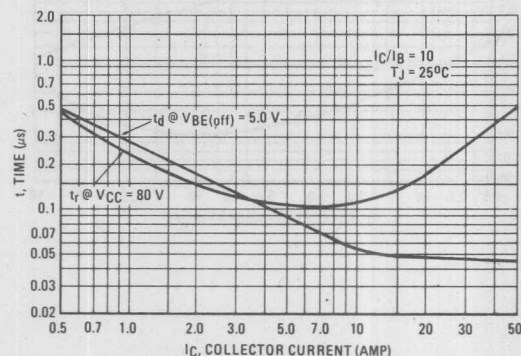


FIGURE 4 - THERMAL RESPONSE

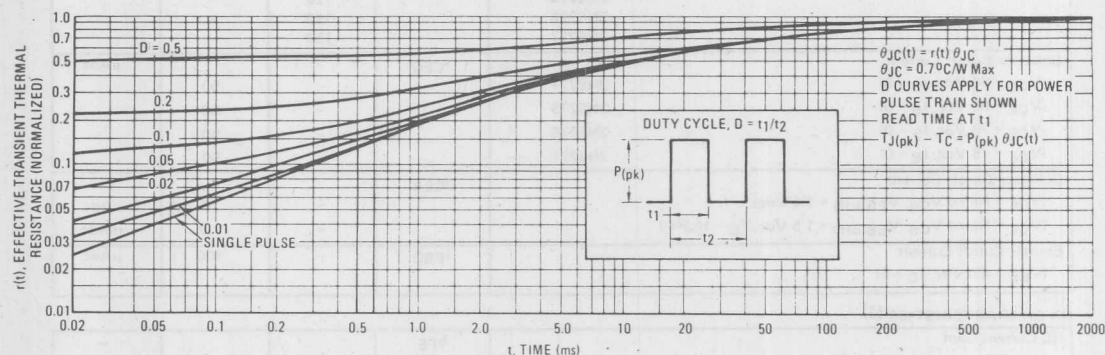
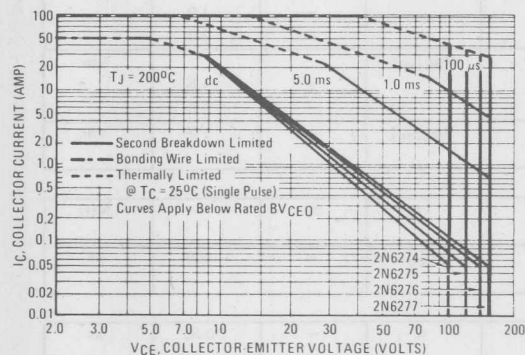


FIGURE 5 - ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 - TURN-OFF TIME

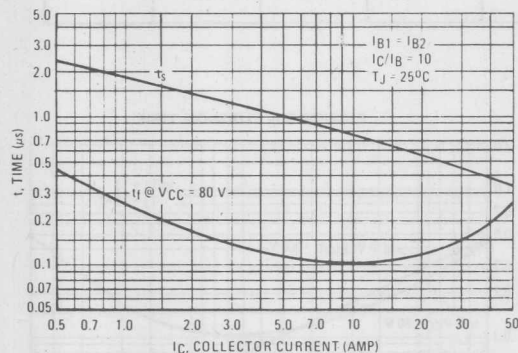


FIGURE 7 - CAPACITANCE

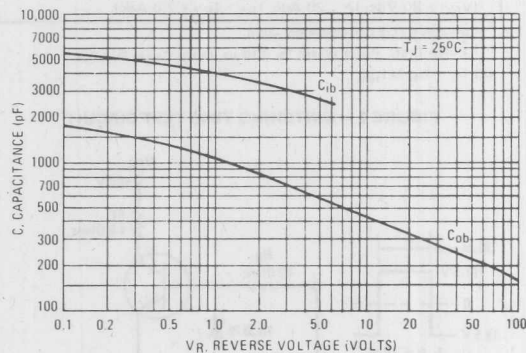


FIGURE 8 – DC CURRENT GAIN

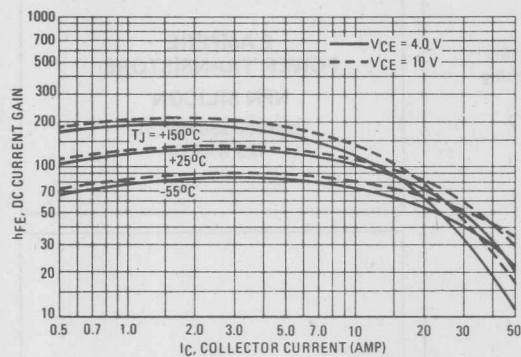


FIGURE 9 – COLLECTOR SATURATION REGION

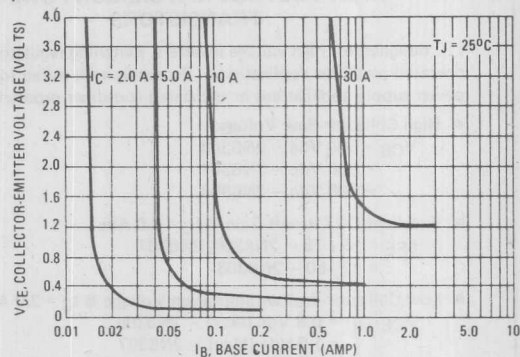


FIGURE 10 – "ON" VOLTAGES

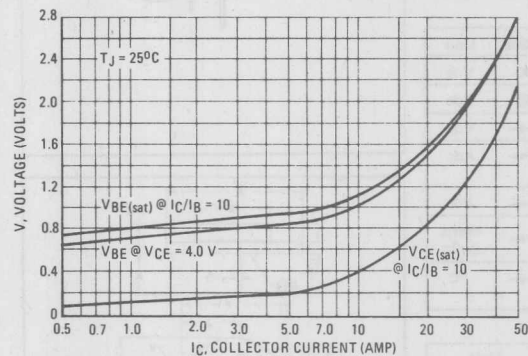


FIGURE 11 – TEMPERATURE COEFFICIENTS

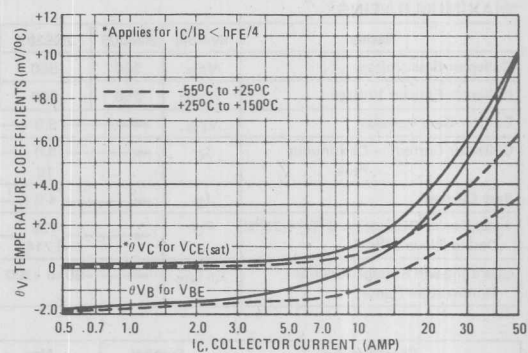


FIGURE 12 – COLLECTOR CUT-OFF REGION

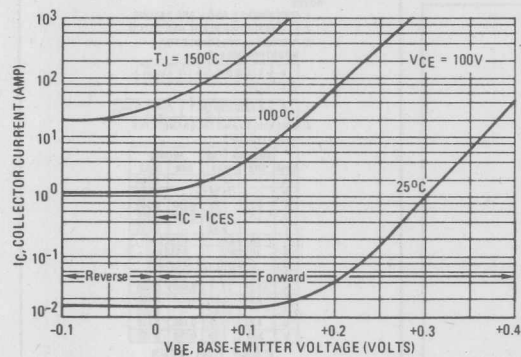
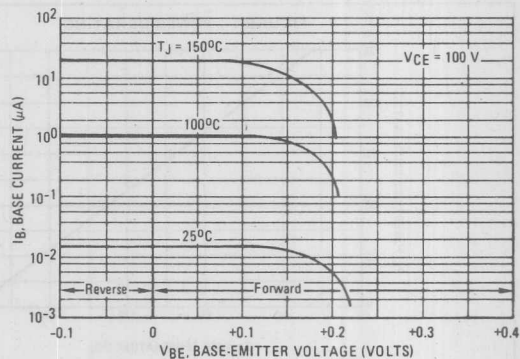


FIGURE 13 – BASE CUT-OFF REGION



**MOTOROLA**

2N6306
2N6307
2N6308

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

... designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications in associated consumer products.

- High Collector-Base Voltage —
 $V_{CB} = 500 \text{ Vdc} - 2N6306$
 $= 600 \text{ Vdc} - 2N6307$
 $= 700 \text{ Vdc} - 2N6308$
- Excellent DC Current Gain @ $I_C = 3.0 \text{ Adc}$
 $h_{FE} = 15 - 75 - 2N6306, 2N6307$
 $= 12 - 60 - 2N6308$
- Low Collector-Emitter Saturation Voltage @ $I_C = 3.0 \text{ Adc}$
 $V_{CE(sat)} = 0.8 \text{ Vdc (Max)} - 2N6306$
 $= 1.0 \text{ Vdc (Max)} - 2N6307$
 $= 1.5 \text{ Vdc (Max)} - 2N6308$
- Current Gain Bandwidth Product —
 $f_T = 5.0 \text{ MHz (Min)} @ I_C = 0.3 \text{ Adc}$

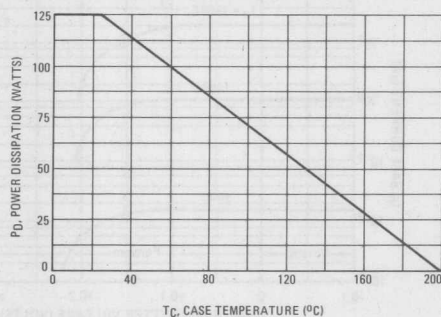
*MAXIMUM RATINGS

Rating	Symbol	2N6306	2N6307	2N6308	Unit
Collector-Base Voltage	V_{CB}	500	600	700	Vdc
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Emitter-Base Voltage	V_{EB}	8.0			Vdc
Collector Current — Continuous Peak	I_C	8.0 16			A dc
Base Current	I_B	4.0			A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	125 0.714			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			$^\circ\text{C}$

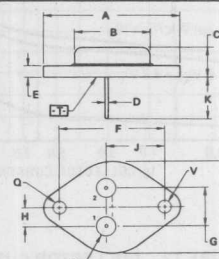
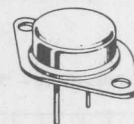
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.4	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING



**8 AMPERE
 POWER TRANSISTORS**
NPN SILICON
250-300-350 VOLTS
125 WATTS



NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\phi \pm 0.13 (0.005) \text{ T V } \phi$$

FOR LEADS:

$$\phi \pm 0.13 (0.005) \text{ T V } \phi \phi$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.09	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	250 300 350	— — —	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEO}$, $I_B = 0$)	I_{CEO}	—	0.5	mA
Collector Cutoff Current ($V_{CE} = 500\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 600\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 700\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 450\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 550\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 650\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	— — — — — —	0.5 0.5 0.5 2.5 2.5 2.5	mA
Emitter Cutoff Current ($V_{BE} = 8.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	mA
ON CHARACTERISTICS				
DC Current Gain (1) ($I_C = 3.0\text{ A}$, $V_{CE} = 5.0\text{ Vdc}$) ($I_C = 8.0\text{ A}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	15 12 4.0 3.0	75 60 — —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 3.0\text{ A}$, $I_B = 0.6\text{ A}$) ($I_C = 8.0\text{ A}$, $I_B = 2.0\text{ A}$) ($I_C = 8.0\text{ A}$, $I_B = 2.67\text{ A}$)	$V_{CE(sat)}$	— — — — —	0.8 1.0 1.5 5.0 5.0	Vdc
Base-Emitter Saturation Voltage (1) ($I_C = 8.0\text{ A}$, $I_B = 2.0\text{ A}$) ($I_C = 8.0\text{ A}$, $I_B = 2.67\text{ A}$)	$V_{BE(sat)}$	— —	2.3 2.5	Vdc
Base-Emitter On Voltage (1) ($I_C = 3.0\text{ A}$, $V_{CE} = 5.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.3 1.5	Vdc
Second Breakdown Energy (Figure 2) ($I_{C(pk)} = 3.0\text{ A}$, $L = 40\text{ mH}$, $R_{BE} = 3\text{ k}\Omega$, $V_{BB2} = 1.5\text{ Vdc}$)	$E_{s/b}$	—	180	mJ
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (2) ($I_C = 0.3\text{ A}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1.0\text{ MHz}$)	f_T	5.0	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	—	250	pF
SWITCHING CHARACTERISTICS				
Rise Time ($V_{CC} = 125\text{ Vdc}$, $I_C = 3.0\text{ A}$, $I_B = 0.6\text{ A}$)	t_r	—	0.6	μs
Storage Time (3) ($V_{CC} = 125\text{ Vdc}$, $I_C = 3.0\text{ A}$, $I_{B1} = 0.6\text{ A}$, $I_{B2} = 1.5\text{ A}$) Pulse Width = $25\text{ }\mu\text{s}$ Pulse Width = $5.0\text{ }\mu\text{s}$	t_s	— —	1.6 0.8	μs
Fall Time ($V_{CC} = 125\text{ Vdc}$, $I_C = 3.0\text{ A}$, $I_{B1} = 0.6\text{ A}$, $I_{B2} = 1.5\text{ A}$)	t_f	—	0.4	μs

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$; Duty Cycle = 2.0%(2) $f_T = |h_{fe}| \cdot f_{test}$ (3) "On" time is $25\text{ }\mu\text{s}$. t_s decreases with shorter pulse widths, being approximately 50% of the values shown at a $5.0\text{ }\mu\text{s}$ pulse width.

*Indicates JEDEC Registered Data.

FIGURE 2 – SECOND BREAKDOWN ENERGY TEST CIRCUIT AND WAVEFORMS

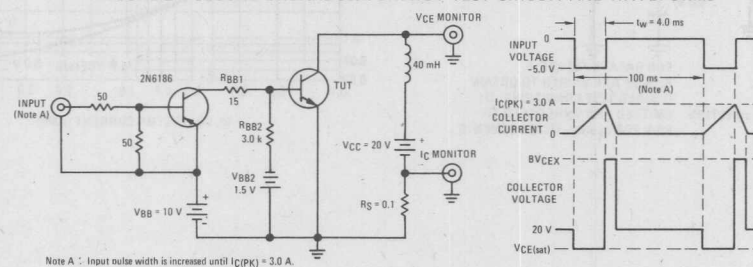


FIGURE 3 – THERMAL RESPONSE

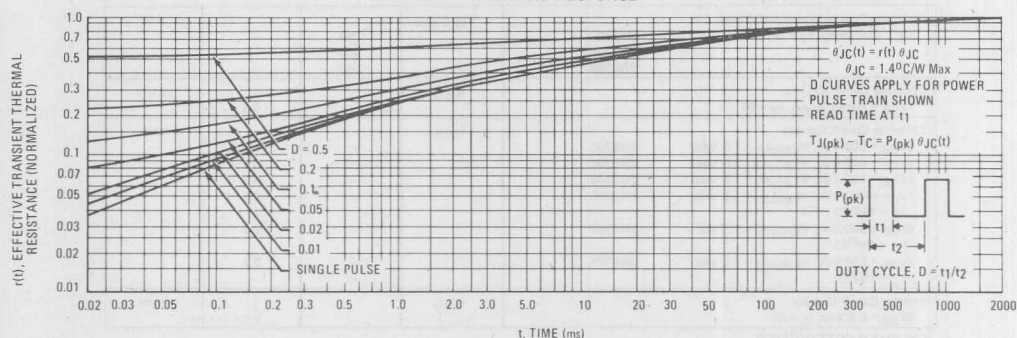
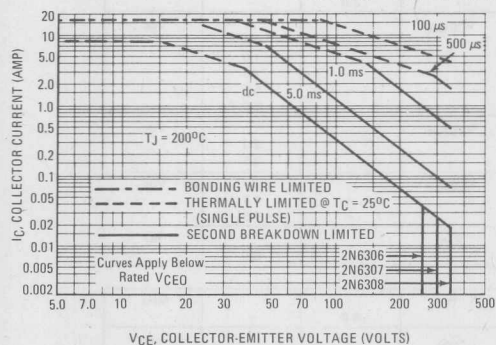


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 5 – SWITCHING TIMES TEST CIRCUIT

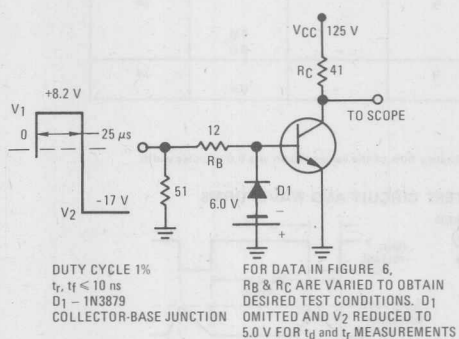


FIGURE 6 – TURN-ON AND TURN OFF TIMES

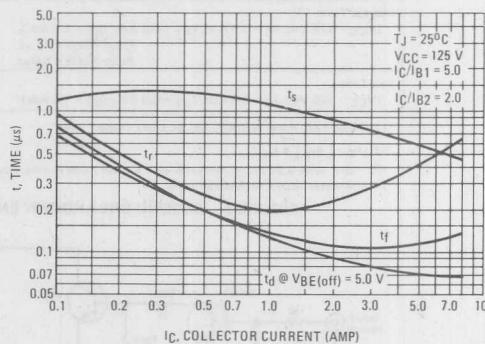


FIGURE 7 — DC CURRENT GAIN

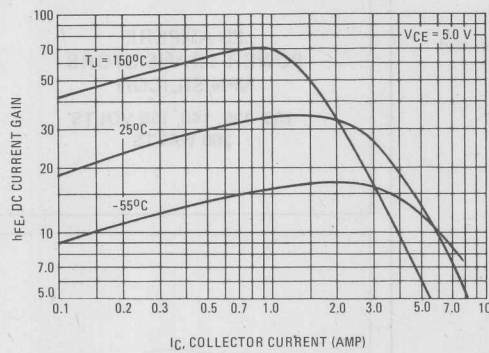


FIGURE 8 — COLLECTOR SATURATION REGION

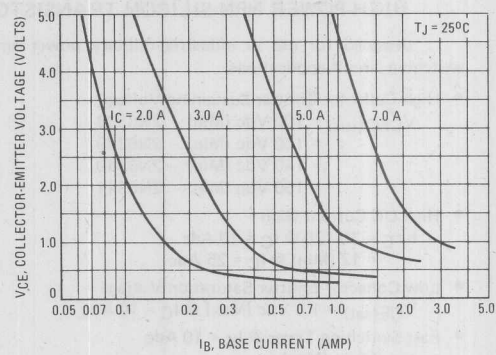


FIGURE 9 — "ON" VOLTAGES

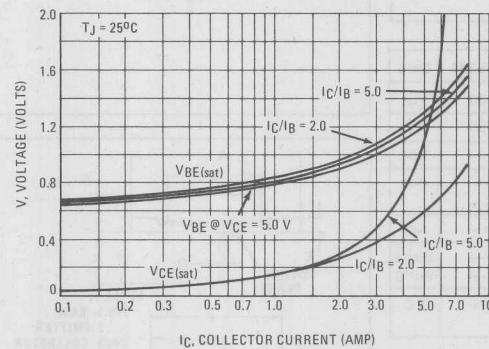


FIGURE 10 — TEMPERATURE COEFFICIENTS

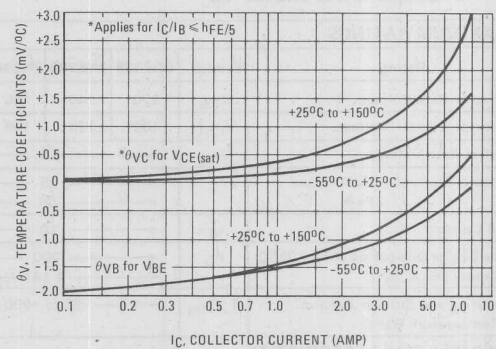


FIGURE 11 — COLLECTOR-CUTOFF REGION

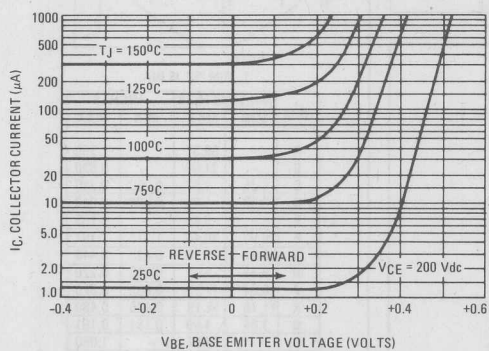
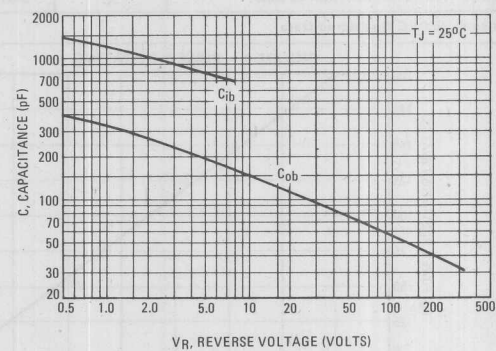


FIGURE 12 — CAPACITANCE



**MOTOROLA****2N6338
thru
2N6341****HIGH-POWER NPN SILICON TRANSISTORS**

... designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 100 \text{ Vdc (Min) – 2N6338}$
 $= 120 \text{ Vdc (Min) – 2N6339}$
 $= 140 \text{ Vdc (Min) – 2N6340}$
 $= 150 \text{ Vdc (Min) – 2N6341}$
- High DC Current Gain –
 $h_{FE} = 30-120 @ I_C = 10 \text{ Adc}$
 $= 12 \text{ (Min) } @ I_C = 25 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) } @ I_C = 10 \text{ Adc}$
- Fast Switching Times @ $I_C = 10 \text{ Adc}$
 $t_r = 0.3 \mu\text{s (Max)}$
 $t_s = 1.0 \mu\text{s (Max)}$
 $t_f = 0.25 \mu\text{s (Max)}$
- Complement to 2N6436–38

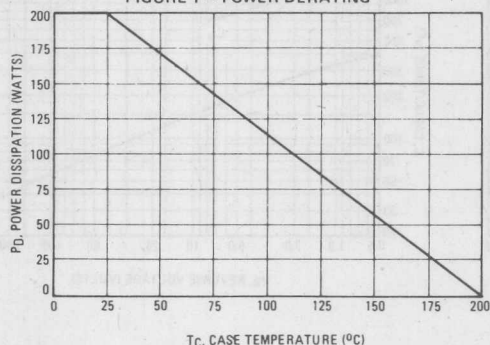
***MAXIMUM RATINGS**

Rating	Symbol	2N6338	2N6339	2N6340	2N6341	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	6.0				Vdc
Collector Current – Continuous Peak	I_C	25				Adc
		50				
Base Current	I_B	10				Adc
Total Device Dissipation @ $T_C = 25^{\circ}\text{C}$ Derate above 25°C	P_D	200				Watts W/ $^{\circ}\text{C}$
		1.14				
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200				$^{\circ}\text{C}$

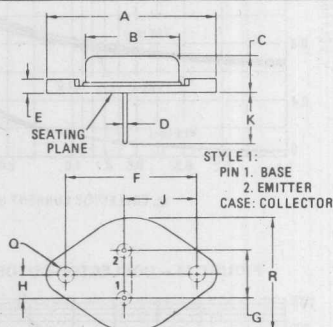
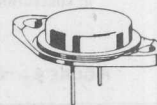
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^\circ\text{C/W}$

* Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING**25 AMPERE
POWER TRANSISTORS
NPN SILICON**

100, 120, 140, 150 VOLTS
200 WATTS



NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

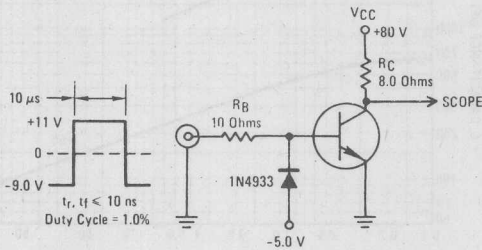
Collector connected to case.
CASE 11-01
(TO-3)

*ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 50\text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	100 120 140 150	—	Vdc
Collector Cutoff Current ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 60\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 70\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 75\text{ Vdc}$, $I_B = 0$)	I_{CEO}	— — — —	50 50 50 50	μAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CE}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CE}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^{\circ}\text{C}$)	I_{CEX}	—	10 1.0	μAdc mAdc
Collector Cutoff Current ($V_{CB} = \text{Rated } V_{CB}$, $I_E = 0$)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current ($V_{BE} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$) ($I_C = 25\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$)	h_{FE}	50 30 12	— 120 —	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 25\text{ Adc}$, $I_B = 2.5\text{ Adc}$)	$V_{CE(sat)}$	— —	1.0 1.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 25\text{ Adc}$, $I_B = 2.5\text{ Adc}$)	$V_{BE(sat)}$	— —	1.8 2.5	Vdc
Base-Emitter On Voltage ($I_C = 10\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (2) ($I_C = 1.0\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 10\text{ MHz}$)	f_T	40	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	—	300	pF
SWITCHING CHARACTERISTICS				
Rise Time ($V_{CC} \approx 80\text{ Vdc}$, $I_C = 10\text{ Adc}$, $I_{B1} = 1.0\text{ Adc}$, $V_{BE(off)} = 6.0\text{ Vdc}$)	t_r	—	0.3	μs
Storage Time ($V_{CC} \approx 80\text{ Vdc}$, $I_C = 10\text{ Adc}$, $I_{B1} = I_{B2} = 1.0\text{ Adc}$)	t_s	—	1.0	μs
Fall Time ($V_{CC} \approx 80\text{ Vdc}$, $I_C = 10\text{ Adc}$, $I_{B1} = I_{B2} = 1.0\text{ Adc}$)	t_f	—	0.25	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width $< 300\text{ }\mu\text{s}$, Duty Cycle $< 2.0\%$
(2) $f_T = h_{FE} \cdot f_{test}$

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 — TURN-ON TIME

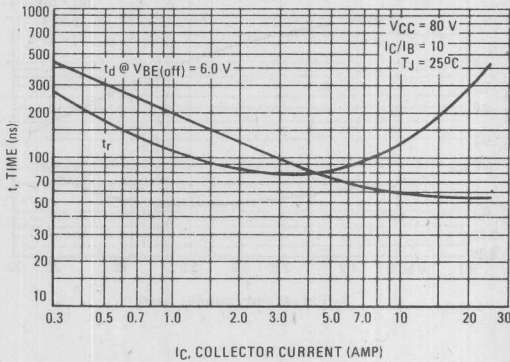


FIGURE 4 - THERMAL RESPONSE

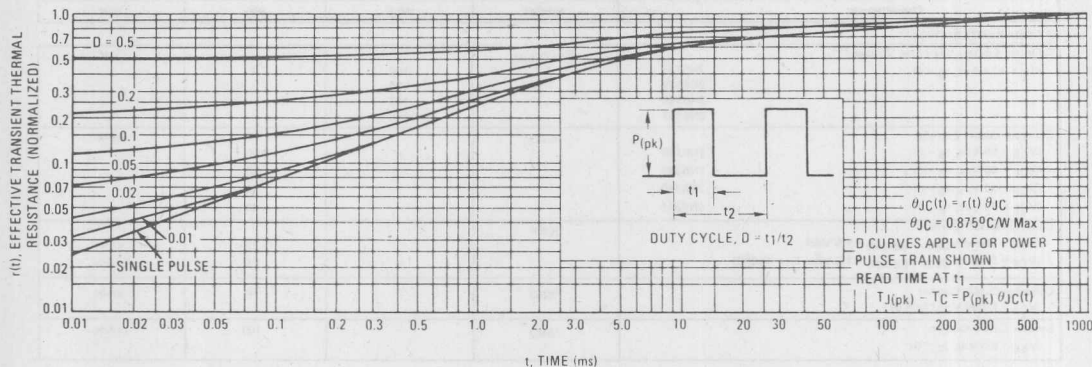
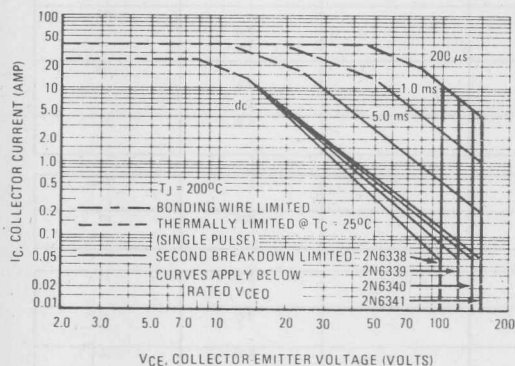


FIGURE 5 - ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 - TURN-OFF TIME

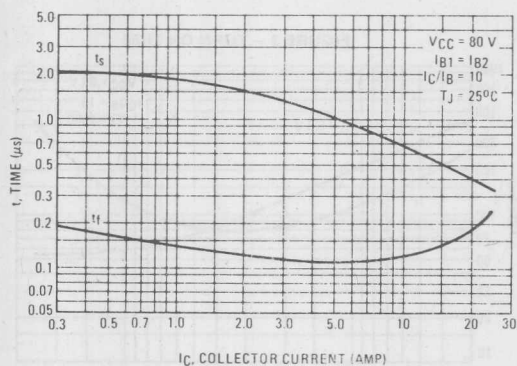


FIGURE 7 - CAPACITANCE

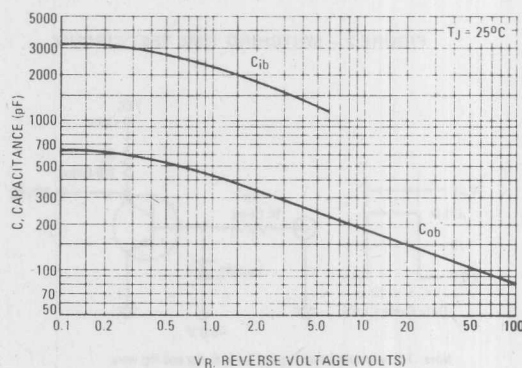


FIGURE 8 – DC CURRENT GAIN

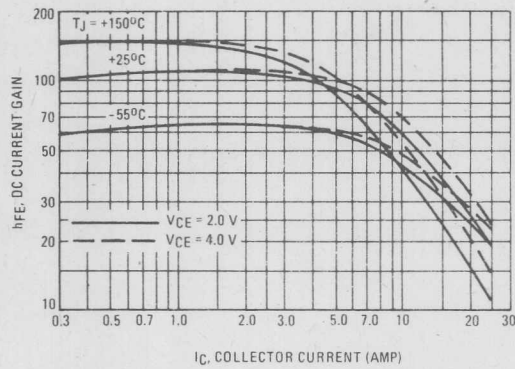


FIGURE 9 – COLLECTOR SATURATION REGION

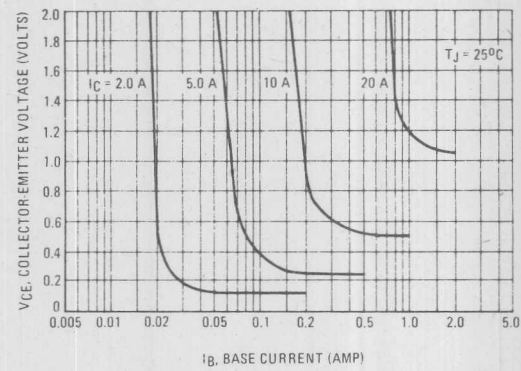


FIGURE 10 – "ON" VOLTAGES

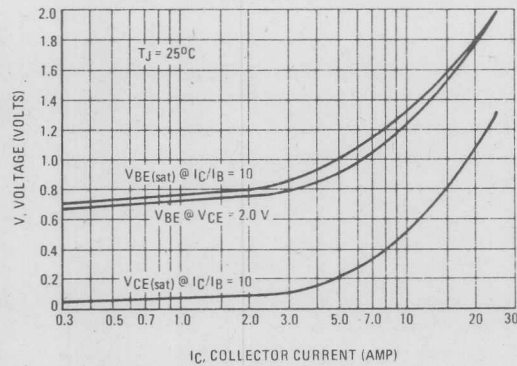


FIGURE 11 – TEMPERATURE COEFFICIENTS

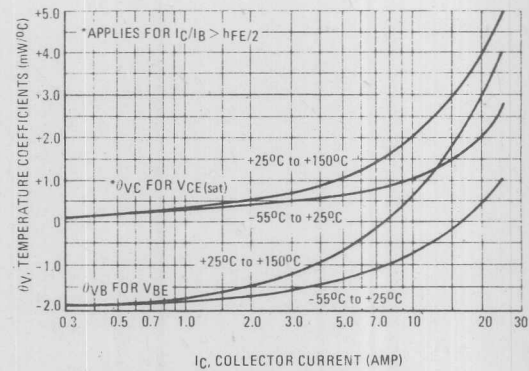


FIGURE 12 – COLLECTOR CUT-OFF REGION

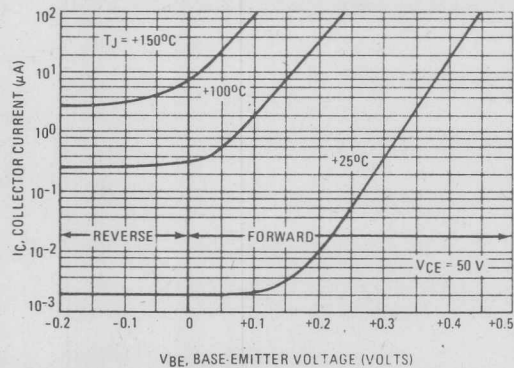


FIGURE 13 – BASE CUT-OFF REGION

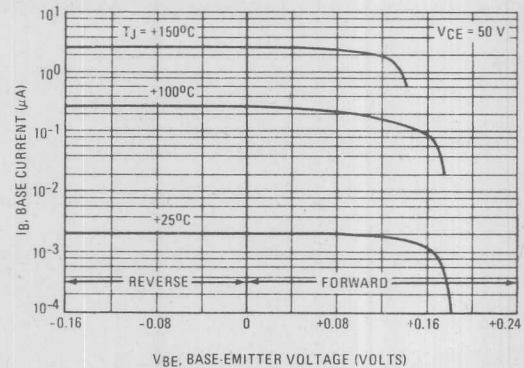


FIGURE 1 - COLLECTOR CURRENT

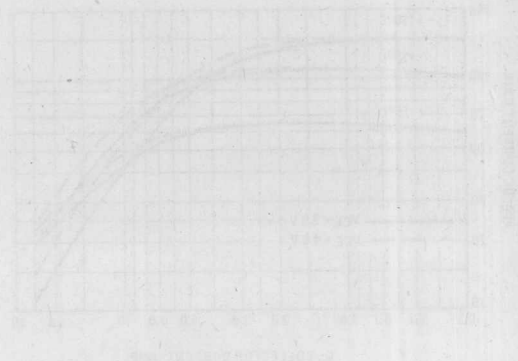


FIGURE 2 - COLLECTOR SATURATION CURRENT

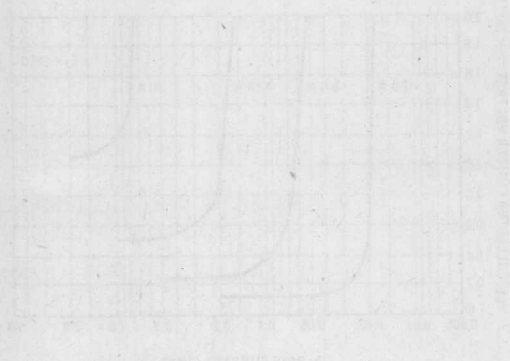


FIGURE 3 - VOLTAGE

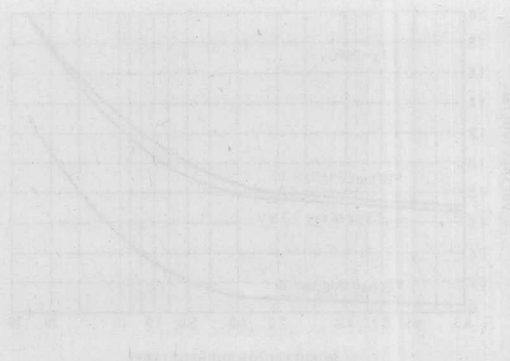


FIGURE 4 - TEMPERATURE COEFFICIENT

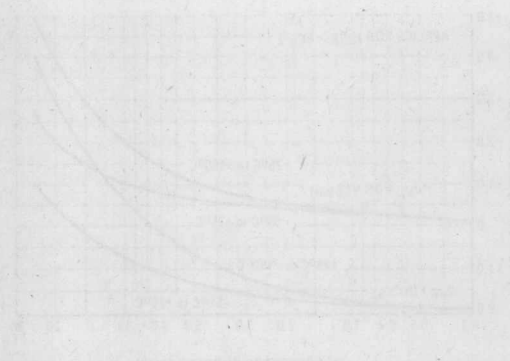


FIGURE 5 - COLLECTOR CURRENT

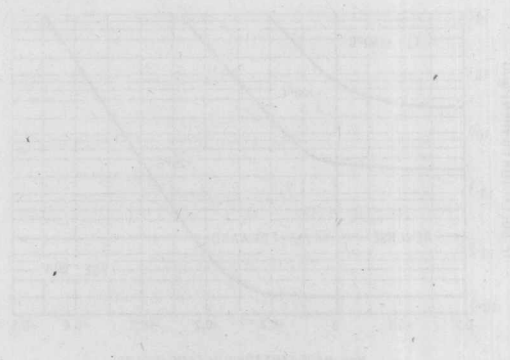


FIGURE 6 - BASE-EMITTER VOLTAGE

